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Design and Analysis of Low Power 7T SRAM 8x8 SRAM Memory Array with Quit Bit Line Technique

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Abstract— ***This paper presents the lowest power 8X8 SRAM array that is designed to store 128 bits. Absolute arrays are equipped with ancillary devices including SRAM cells, write driver circuits, revived circuits, address decoders, and sense amplifiers. This documentation is for an 8X8 SRAM array that utilizes 7T SRAM cells and is ranked according to total power consumption. Location and obstructions have a significant role in determining SRAM's overall efficacy. The suggested architecture for an 8x8 SRAM array is similar to existing 8x8 SRAM arrays that use conservative 6T SRAM cells, with the addition of a single NMOS transistor placed between two cross-coupled inverters. These designs reduce static power in support mode. The cadence simulation device is exercised at 90nm technology for manipulation. The proportional research is completed in a sequence of Read, Write Access time, Leakage power consumption, and absolute Leakage power consumption. Utilizing the Quiet Bitline approach, in which the voltage of bit lines remains as low as possible to attain high speed with low power while operating at a temperature of 270C, we have optimized leakage current and low power of an SRAM memory array. With the use of a low-power, quiet-bit line method, all bit lines are kept at low voltages at all times. This prevents wasteful full-swing charging on the bit line one-side driving scheme, which is utilized for write operations, and for read operations, that employ precharged, free-pulling techniques.***

***Keywords*: SRAM, 7T SRAM Cell, Cadence, CMOS, Leakage Power.**

I. INTRODUCTION

Memory, a fundamental component of every computer, drives the semiconductor market. Memory accounted for 27 percent of the global semiconductor industry market in 2020 (USD117 bn) and 28 percent of the market in 2021 (USD154 bn), as reported by WSTS (World Semiconductor Trade Statistics). The market for semiconductor memory is anticipated to exceed $730 billion by the end of 2024 [1]. Modern edge devices with support for IoT (Internet of Things) & AI (artificial intelligence) and must integrate memory into the CPU to meet the growing need for quick data processing. In order to construct energy- and performance-efficient algorithms, machine learning (ML) urgently need such hardware to conduct CIM (computation in memory). [2,3]. In the course of processing, memory stores information either permanently or temporarily. Access time and data retention are two crucial factors that influence the hierarchy of memory; faster memory will be located nearer to the processor unit. Classes for memories are shown in Figure 1. New nonvolatile memory cells including MRAM, PCM-RAM, FRAM, RRAM, and FLASH are desirable due to their enhanced performance, density, and retention time. [4–7]. However, the SRAM cell has emerged as a viable option for cache memory due to its lower latency and push-rule-based manufacturing [8]. SRAM performance and density have significantly increased due to technological scaling. Currently, 90 percent of transistors responsible for memory are present in a modern SoC. [9] But technological advancement is also creating a confluence of problems. SCE, or short channel effects [10] influence the efficacy and increase leakage current. As a result, a switch in transistor structure from planar to 3D-CMOS [11] and silicon on insulator (SOI) [12] technologies reduce junction leakage and SCE. Better conduction channel control is offered by a FinFET-SRAM cell. Therefore, FinFET is necessary for contemporary deep-submicron nodes. However, the SRAM cell stability is seriously threatened by the lower supply voltage. The power budget is also accelerated by leakage current. [13]. Additionally, variations in Vth (threshold voltage) have alarmingly increased the risk of non-erroneous SRAM cell operation [14]. Variations in the processes directly affect dependability[15]. In addition to the aforementioned problems, developing topics include SRAM soft faults and data security [16]. As a tradeoff for performance parameters, researchers have suggested a multitude of strategies for addressing these problems. [17–19]. Recent CIM developments also need dependable SRAM performance when several memory regions are accessed at once. Consequently, it is crucial to conduct a thorough analysis of SRAM limitations and cutting-edge solutions.

To store logic LSI's signature data, static random access memory (SRAM) has been widely employed. This is due to the SRAM array's quick operation and low standby power consumption. SRAM Cells also have the benefit of not requiring additional process costs during the manufacturing phase. Other memories like DRAM and Flash memories are unable to match these properties of SRAM. High performance, low power consumption, and low cost are anticipated from a well-designed SRAM cell & SRAM cell array. A non-destructive read operation and a dependable write operation must be provided by an SRAM cell in order for it to function properly. Engineers working on the process and design of SRAM cells have difficulties in ensuring data integrity in SRAM arrays due to the scaling of supply voltage and minimum transistor size. In a large SRAM array that can store billions of bits, this is a particularly challenging task. Device scaling presents a number of difficulties for VLSI (very large-scale integration) SRAM design. Leakage power consumption is on the rise as a result of today's designers' use of ultra-thin gate oxide and

extremely low threshold voltage. Read-and-write operations can degrade data stability, making fault tolerance an essential feature of SRAM for enhancing its dependability.

The tunneling gate leakage current increases exponentially with a low threshold voltage, while the sub-threshold leakage current increases exponentially with ultra-thin oxide. Dissipation of power due to leakage in a circuit is not linearly related to its surface area. The chip area is occupied about 50% by many processors' caches. Low voltage caches using 7T-SRAM cells have been developed.

The methods include Low power SRAM design, with an emphasis on minimizing voltage & capacitance, and swing. The primary capacitive components are the shards of memory bit lines, word lines, and data lines. There are two methods in the Quiet bit line technique, first for a read operation precharged free pulling scheme and second for a write operation, a one-side driving scheme. The term "Quiet" refers to maintaining a very low voltage on the bit line at all times. Read and write operations need to be improved, get this condition.

CMOS device characteristics are affected by temperature variations, causing integrated circuit performance to fluctuate. A circuit's propagation delay is proportional to the discharge current generated by active transistors. A set of device parameters determines the temperature-dependent efficacy of an integrated circuit. Variations in temperature have an effect on CMOS's threshold voltage, carrier mobility, and saturation velocity, all of which contribute to its low power and leakage current. Drain saturation current decreases with increasing supply voltages when a CMOS is heated. At low supply voltages, however, the drain current of a CMOS device shows an opposite trend, increasing with temperature. There is a bias voltage for which changes in device parameters have an influence on CMOS current that is counterbalanced when the temperature fluctuates. The ideal supply voltages (VDD = 0.7V) in 90 nm CMOS technology are greater than the nominal supply voltages necessary for temperature-insensitive circuit performance. Integrated circuits working at scaled supply voltages use little electricity at the expense of lower speed. The temperature may vary dramatically from one die region to the next due to needless application and a variety of circuitry at different portions of an integrated circuit. Furthermore, changes in the temperature of the environment can result in significant variations in the temperature of the die. I created a 7T Low Power SRAM Array Cell with temperature and leakage current variations. The low power method On SRAM arrays which are configured to minimize integrated circuit power consumption during read and write operations, quit bit lines are applied. The Memory array Cell is built with low power requirements and low leakage current in mind, ensuring complete circuit stability up to the necessary level. As a result, there is a decrease in overall power without Area and Delay overhead

II. SRAM ARCHITECTURE

The block diagram of a regular SRAM is seen in Figure.1. Both bit- and word-oriented structures are possible for SRAMs. While each address in a word-oriented memory typically takes up n bits (preferred values of n include 8, 16, 32, and 64), each address in a bit-oriented SRAM takes up a single bit. Y-address-bit-directed column decoders or column multiplexers (YMUXs) make it possible for two or more columns to share a single sense amplifier. The read-and-write operations of an SRAM cell should be secure and dependable. These two requirements impose constraints on SRAM cell transistor estimation. The transistor ratios in an SRAM cell need to be calculated for optimal reading and writing. The following lists the primary SRAM building squares.

1. SRAM cell.
2. Write Driver Circuit.
3. Pre-Charge Circuit.
4. Row decoder.
5. Sense Amplifier.

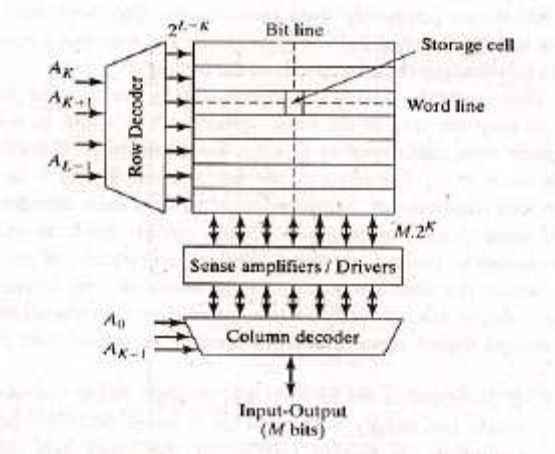

Fig. 1. SRAM Block diagram

III. 7T SRAM CELL

When it comes to CMOS memory applications, memory cells are often categorized as (1)Storage operation, (2) Number of constituent elementary devices, (3) Storage media, (4) Access mode, (5) Data forms, (6) Logic system, (7) Storage mode, (8) Featured operation modes (9) Toughness against radiation. In this work, memory cells are deployed in arrays, and every other memory circuit in the paper is designed to make use of the arrays' functionality. [10]. An array in RAM is a configuration of memory cells.

Write operation and read operation. This paper proposes the implementation of 7T SRAM which is better in terms of Q Arrays are useful because instead of having to separately store related information in dissimilar names as memory position. Each fundamental positioned to a collection is robotically accumulated in an adjacent memory position. The leakage current of the memory augment within capability which has extreme power will be addicted still in the support cycle. Many schemes are used to reduce power, here we try to save power to write and by power dissipation.

8-bit cells are used to store 8 bits at a time and produce one output at a time. Here 7T is used to store a single bit. Each BL and BLB is reviving maximum prior and following both read/write operations. Write operation is done when the center NMOS is OFF but here this NMOS is getting DT and ON, so it read at the same time and initially, it generates garbage value. The balance of data to be printed to node Q is functional to BLB and equivalent NMOS is twisted through declaring Word line DT maximum. BL and its access transistor do not take part in the write operation. During standby mode, both access transistors are kept off by applying a negative DT pulse. At the next positive pulse of the DT center, NMOS is ON and reads previously stored data.

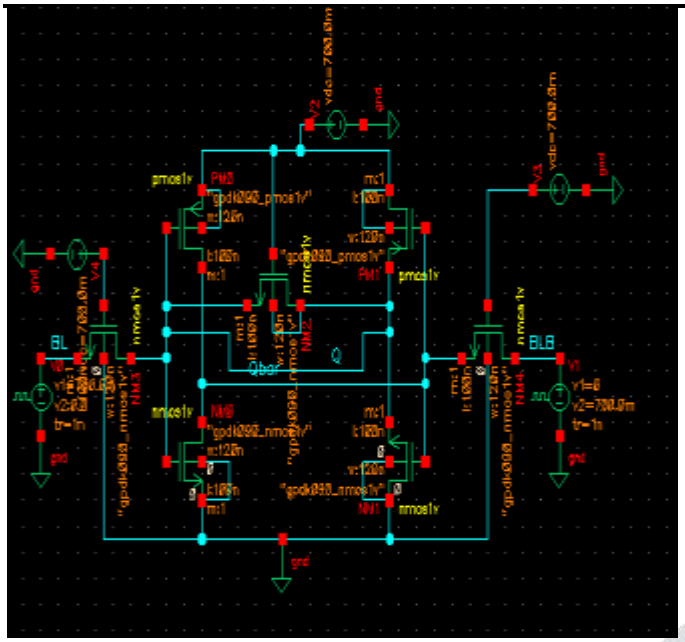

Fig. 2. Schematic of 7T SRAM Cell

Through read operation sense amplifier obtain BL and BLB, and read the data while word line DT is rotten. 3-to-8 Decoder is used to select to write one of all cells. In the 8x8-bit array, Read operations are back and forth between 8x8-bit cells. Both sense amplifiers 1 and 2 produce the data of ST1 and ST2 respectively at different pulse times.

IV. Precharge Circuit

In an SRAM array, the precharge circuit is the main component. The precharge circuit diagram is shown in Figure 3. There are three PMOS transistors in total. For revitalization, 2 larger transistors are used, and for balancing, one single transistor is used. Prior to read and write operations, the primary function of the precharge circuit is to charge both bit lines to VDD = 0.7V. The precharge circuit enables the bit lines to get a stimulating boost during each read/write operation. PMOS transistors have a measured thickness of 120nm and a length of 100nm. Each column in the archive only makes use of a single precharge circuit.

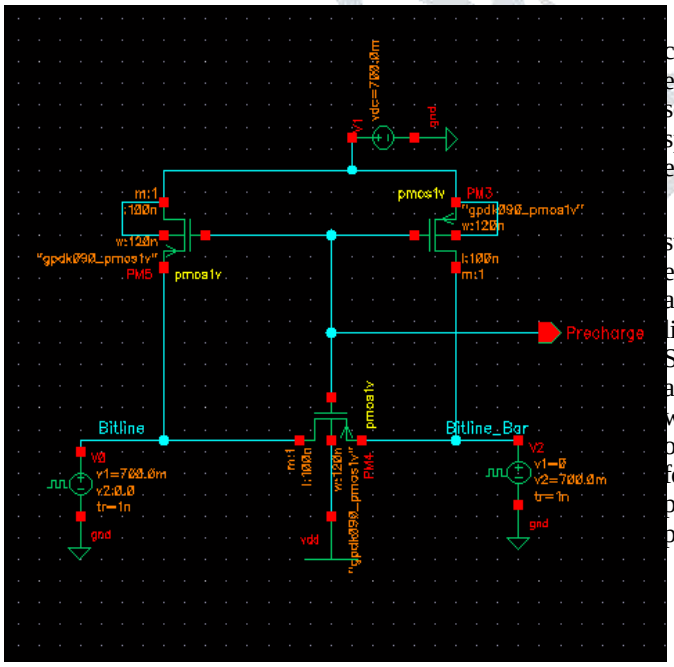

Fig. 3. Circuit Diagram of Precharge Circuit

V. Write Driver Circuit

The SRAM write driver may quickly discharge individual bit lines below the SRAM cell's write margin, serving as precharge. In most cases, the WE (Write Enable) signal allows the write driver to discharge the bit line completely from the precharge level all way down to the ground. It is not absolutely necessary for the correct execution of the writing process that the word line be enabled and writes drivers to be activated in quick succession. The write driver makes use of two load NMOS transistors to generate pair pass-transistor AND gates, which are made up of NMOS Q1, Q3, & Q2, and Q4 transistors. NMOS transistors Q1 and Q2 have their power source connected to the ground. When the write allow signal is present in inverters 1 and 2, input data will either activate Q1 or Q2 transistor. This will connect a strong '0' by allowing BL or BLB to fall from precharge level to ground level.

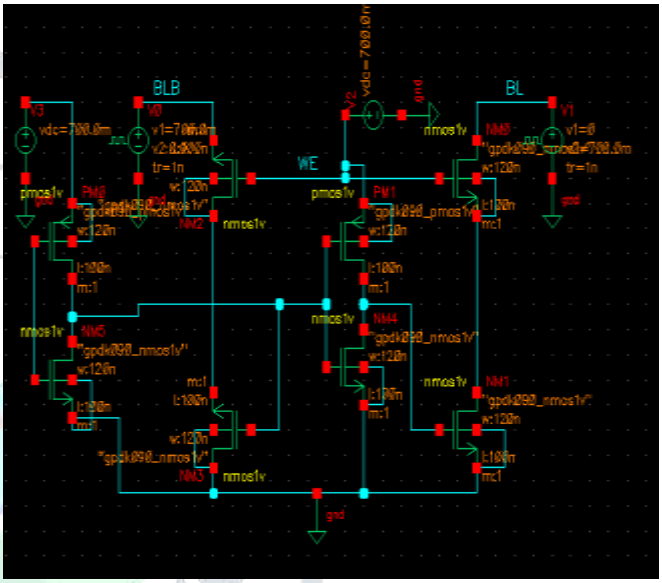

Fig. 4. Circuit Diagram of Write Driver Circuit

VI. Sense Amplifier

Input components like sense amplifiers, which are coupled to memory cells, are essential to the presentation and environmental tolerance of CMOS memories. The goal of a sense amplifier in our circuit is to give signals that meet the specifications of memory's driving peripheral route, hence enhancing memory's speed performance.

The sense amplifier is required to make an attempt in the surrounding environment of the circuit components. The elementary situation for the functioning of the sense circuit and amplifier may primarily be acquired from the operational limitations of the potential sense circuit. Figure 3 shows the Sense Amplifier Circuit, during read operation sense amplifier receives BL and BLB, and reads the data when the word line DT is off. 3-to-8 Decoder is used to select to write one of all cells. In 8x8 bit array Read operations are back and forth between 8x8-bit cells. Both sense amplifiers 1 and 2 produce the data of SA1 and SA2 respectively at different pulse times.

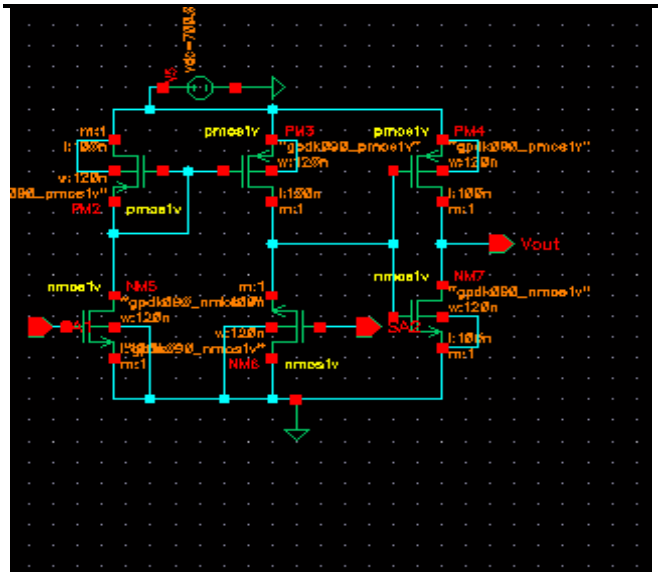

Fig. 5. Sense Amplifier

VII. 3:8 DECODER

Every address row is assigned a unique set of 2N lines by the 3:8 decoder. The output of the decoder is delivered into the SRAM array's word row. They choose the row in the SRAM array that is permitted to be utilized. The graphical representation of the row decoder that is being used can be seen in Figure 4. Decoders are an essential component of the SRAM design process because they are responsible for deciding where in the matrix of memory cells, which is laid out in a row-and-column arrangement, we will be working. This makes them an essential component of the SRAM design process. The Row decoder is constructed from a sequence of NAND gates, in its most basic form. N input from the user can decode up to N rows of information. Selecting the correct cell from the array of cells is another crucial function performed by the column decoder. A large number of words may be efficiently designed using a column decoder. The bit line wire length and diffusion cap of all the pass transistors linked to the word line are visible to the column decoder, making its design important. It relies on the idea of decoding the column address bit by bit. Typically, the last digit is what decides which column will be used. The first few bits of an address indicate the row, while the final few indicate the column. The 3:8-row decoder was employed, and its output was used to link the array's word line. Address decoding is employed in memory design to decode the provided address and activate the specified row or column. A specific WL and WE of an SRAM array are chosen using a row and a column decoder, respectively.

Figure 6 depicts a decoder diagram with 3 inputs (a, b, and c) and eight outputs (X0 - X7). The AND gate-based decoder is employed in this research. When using Table 1's outputs from the 3:8 decoder, select a specific WL and WE for the equivalent column & row of the SRAM collection.

TABLE I. DECODER THREE-TO-EIGHT AND OUTPUT SELECTION

Inputs			**Output Selection (As WL/WE Selection)**
A	B	C	
0	0	0	X0
0	0	1	X1
0	1	0	X2
0	1	1	X3
1	0	0	X4
1	0	1	X5
1	1	0	X6
1	1	1	X7

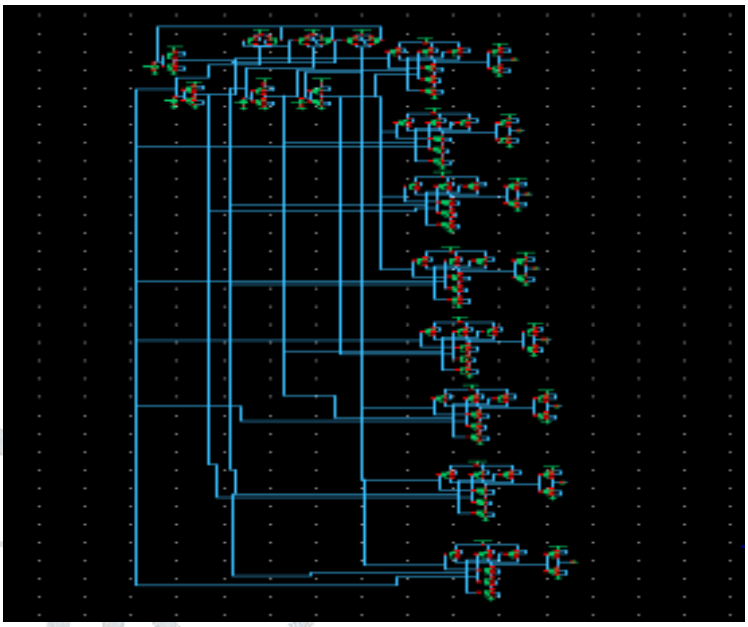

Fig. 6. 3:8 Decoder`

VIII. 8X8 MEMORY ARRAY ORGANIZATION

This 8X8-bit SRAM array employing 7T can store 16 bytes. These components include 8 precharge circuits, 8 write driver circuits, and 8 sensing amplifiers. The precise WL and WE signals of the write driver circuit are selected with the help of a column and row decoder. The design for an 8X8 SRAM array employing 7T SRAM cells is shown in Figure.7

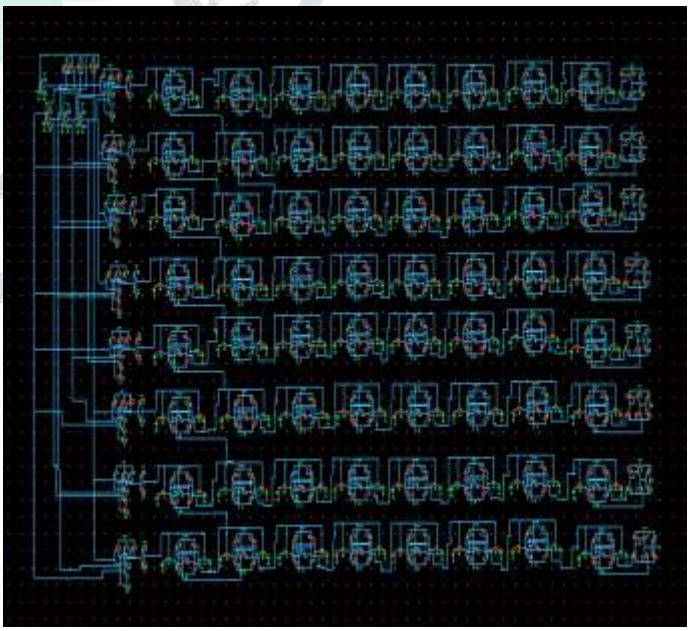

Fig. 7. 8x8 Memory Array

IX. LOW POWER QUIT BIT LINE TECHNIQUE

Power is used in SRAM for things like read/write address decoding, output driving, sense amplification, word line driving, multiplexing, bit line charging, and static current.

The bit lines' voltage is maintained at an absolute minimum via silence. The immediate benefit is the

elimination of bit-line charging and discharging electricity. The two distinct modes of operation are writing and reading. It is common to practice utilizing a one-sided drive scheme for writes to avoid bit-line overcharging during full-swing operations. This technique involves accessing a floating-point cell while simultaneously forcing a strong "0" signal into it. The pulling strategy is employed for the reading procedure. It works by first taking bits from bit lines, then activating word lines, then equalizing bit lines, and then amplifying sensation.

For a read operation, the bit line charge power can be substantially reduced if aggressive word line pulse control is utilized to restrict bit line fluctuation to between 100 and 200mV. Nevertheless, all bit lines are typically required to have full cycles during a write operation, primarily to facilitate a rapid cell reversal. For the write operation, only the side of the bit line or bit line bar that has a strong "0" signal forced into it is driven, while the other side is left floating. The charge needed for reading and writing is also done away with. A design with silent bit lines is the result of combining these two approaches.

X. Simulation Results and Discussion

The simulation of an 8x8-bit array of 7TSRAM cells in 90nm technology at a notional supply current of Vdd= 0.7 V was carried out employing a cadence tool. Read and write data into the cell, as well as the transient response of an 8x8 bit array utilizing a 7T SRAM cell, are shown in the figures below in appropriate order. The gate leakage is the only major mechanism at room temperature, which is 27 degrees Celsius.

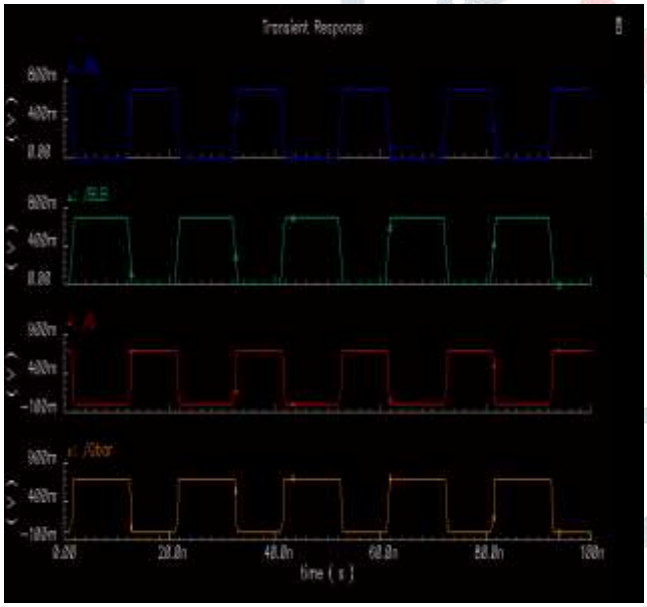

Fig. 8. 7T SRAM cell write waveform

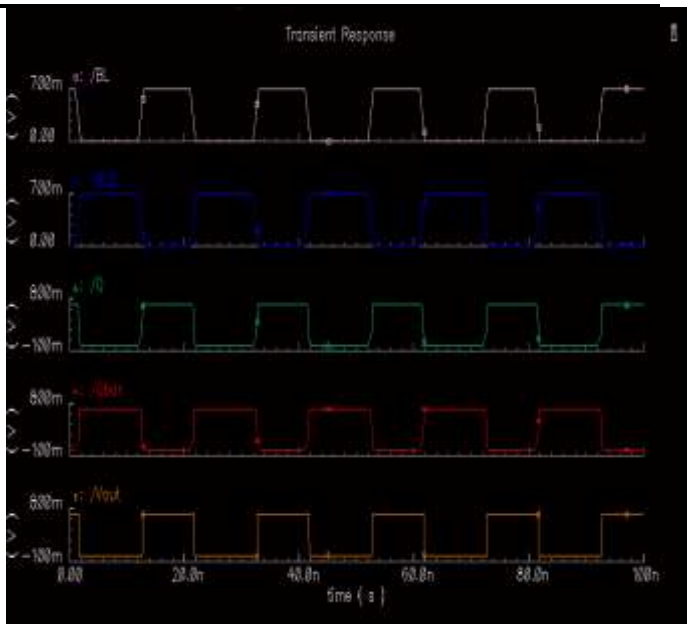

Fig. 9. Waveform read of a 7T SRAM cell

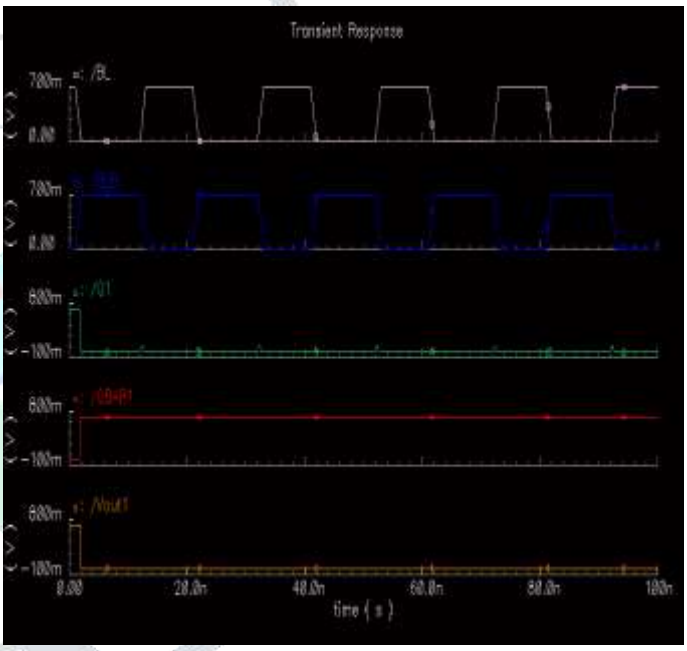

Fig. 10. SRAM cell transient response in an 8x8-bit array

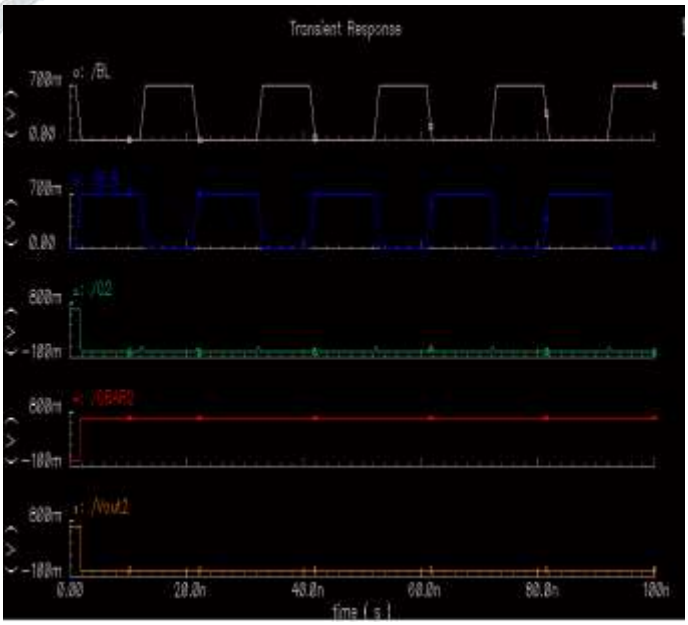

Fig. 11. Transient Response of 8X8 Bit Array using 7T SRAM cell

The resulting Summary of the 8x8 Array with 7T SRAM Cell is shown below in Table 1.

TABLE II. SIMULATED RESULT SUMMARY

S.no	Performance Parameter	8x8 Array with 7T SRAM Cell	8x8 Array with 7T SRAM Cell with Quit Bit line Technique
1.	Leakage Power	8.4nW	6.4nW
2.	Total Leakage Power Consumption	33.6nW	28.6nW
3.	Read Access time	21.1ns	18.8ns
4.	Write Access time	16.5ns	14.2ns
5.	The capacity of Array to store a bit	128 bits	128 bits

XI. CONCLUSION

Data storage is a need in all modern high-speed VLSI circuits. Nowadays, it's crucial that massive amounts of data be kept in one place and quickly accessed. Around two years, utmost storage capability which is virtually executed twice. A crucial design metric is the number of accumulated data bits per unit area, which measures the memory collection's region efficacy. Memory access time is an additional crucial performance criterion. The speed of the memory array is determined by access time. Intentionally low-power 8X8 SRAM array with 128-bit storage. The inclusion of the SRAM cell, precharge circuit, write driver circuit, address decoder, and sensing amplifier in the absolute array is intentional. In this study, a 7T SRAM cell-based 8X8 SRAM array is created and its overall power consumption is ranked. The suggested 8X8 SRAM array uses 7T SRAM cells, which use less power than the more often used 6T SRAM array. SRAM arrays are designed with a supply voltage of 0.7 V in consideration. Temporal reactions while reading and writing have been studied. Cadence is employed to design the low-power SRAM array, and the gods (generic process design kit) 90nm library is utilized for design. This study introduces the Quit Bitline approach as a means for designing a low-power, 8x8 SRAM array that is robust against temperature fluctuations. The technology used is 90 nm CMOS. CMOS drain current changes are caused by temperature-dependent device parameters, which are discovered.

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