JETIR.ORG ISSN: 2349-5162 | ESTD Year : 2014 | Monthly Issue

JOURNAL OF EMERGING TECHNOLOGIES AND INNOVATIVE RESEARCH (JETIR)

An International Scholarly Open Access, Peer-reviewed, Refereed Journal

Optimizing Conventional Full Adder Design for Enhanced ALU Performance

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Abstract: The adder is a critical component of the ALU and plays a very significant role in determining the performance of a computer system. It is very much required to use an optimized adder for enhanced performance of the ALU and improved overall system performance. This Review paper will show you how various researchers have created a low-power consumption-based adder circuit based on length of transistor. This paper presents a Review on adder circuit design for transistor sizes of 65nm and 90nm. The major goal is to build a prototype for Low Powered VLSI Technology to develop an adder circuit that consumes less power while maintaining high performance than the regular design that uses 28T CMOS logic. The adder is the most basic component of the ALU, and it is used in almost all arithmetic operations. In many cases, it is also used in the implementation of other operations, such as subtraction and multiplication. The performance of the adder directly impacts the performance of the ALU and, therefore, the overall performance of the computer system. A slow or inefficient adder can lead to long wait times for the completion of arithmetic operations, which can result in poor system performance. An optimized adder, on the other hand, can greatly improve the performance of the ALU. By reducing the time, it takes to perform an addition operation, the ALU can complete other operations more quickly, resulting in improved overall system performance.

Keywords **- Carry-look ahead adder, ALU, VLSI, CMOS, NMOS, Low-power transistor, Memory Enhancement, Pass Transistor logic, Multiplexer, Power Delay Product**

I. INTRODUCTION

These days, portable devices powered by batteries are utilizing a lot of power to conduct activities involving calculation. The number of components in a silicon chip doubles every one and half year according to Moore's law. When it comes to portability, power dissipation is the greatest challenge. Today, there has been a rapid and significant improvement in the performance of microprocessors, microcontroller when compared to factors like the number of transistors, power consumption, propagation delay, and the elimination of complicated circuit design approaches. Less area and higher performance are crucial restrictions in VLSI design. But as power-efficiency has become a need for portable devices, power consumption has emerged as a key issue to consider while developing a VLSI. An optimized adder is designed to perform addition of two binary numbers with improved speed and reduced power consumption. An optimized adder can be designed using various techniques such as carry-lookahead adder, carry-skip adder, and carry-select adder. A carry-lookahead adder generates carry bits in advance and reduces the carry propagation delay. It is implemented using a two-level logic structure, with a generate and propagate logic for each bit position. A carry-skip adder is a combination of a carry-select adder and a carry-lookahead adder. It reduces the carry propagation delay by skipping the bit positions that don't have any carry. A carry-select adder uses two adders, a full adder and a half adder, to reduce the carry propagation delay. The half adder is used when there is no carry input, and the full adder is used when there is a carry input. Using these optimized adder techniques in the Arithmetic Logic Unit (ALU) of a computer system can greatly improve its performance. The ALU is a critical component in a computer system and its performance can directly impact the overall performance of the system. By using an optimized adder in the ALU, you can achieve faster addition and subtraction operations, which in turn can improve the overall performance of the system. Advancements in portable devices have led to increased power consumption during complex calculations, creating a challenge for their portability. However, innovative VLSI design techniques such as carry-lookahead adders, carry-skip adders, and carry-select adders have significantly improved speed and reduced power consumption in microprocessors and microcontrollers. By integrating optimized adders into the Arithmetic Logic Unit (ALU) of computer systems, faster addition and subtraction operations can be achieved, ultimately enhancing the overall system performance.

II. OBJECTIVES

The modular adder circuit serves as the fundamental processing unit in addition and multiplication. A significant element of a VLSI application's ALU construction is the adder. The basic building block of a microprocessor which is nothing but the full adder circuit is one of the most important parts since it is utilized in the floating-point units, the ALU, and address generation for cache

and memory accesses. Power-efficient VLSI circuits are essential due to the rising demand for portable electronic gadgets like laptops and cell phones. Therefore, in this paper we have made an attempt to Review an optimized adder circuit to enhance the performance of ALU with low Power Consumption. This review paper focuses on the adder circuit, a crucial part of microprocessors that helps with math tasks like addition and multiplication. It's like the building block that makes computers work. With the growing use of laptops and cell phones, we need circuits that use less power to make our devices last longer on a single charge. So, in our research, we explored a special adder circuit that can boost the performance of microprocessors while using less energy. Our optimized adder circuit was designed with smart techniques and new technologies to be more efficient. By using less power, it can help make the entire microprocessor more energy-friendly. The main goal of our work is to create faster and more power-efficient microprocessors. This way, our devices can perform better and last longer on their batteries, making them more user-friendly in our everyday lives. As technology continues to advance, our research aims to contribute to greener and more sustainable computing solutions. This review paper delves into an optimized adder circuit's potential to enhance microprocessor performance and efficiency, vital for modern portable devices like laptops and cell phones. By using smart techniques and cutting-edge technologies, the goal is to create faster and more power-efficient microprocessors, contributing to greener and more sustainable computing solutions.

III. CONVENTIONAL FULL ADDER AND ITS DISADVANTAGES

3.1 Logic Realization of Full Adder

A full adder is the most fundamental yet most important digital circuit to design. To design a typical full adder using basic gates, we need 2 EXOR gates, 1 OR gate, 2 AND gates. It takes 3 Inputs, A (1), B (2), Cin (3) and returns 2 Outputs, Sum and Carry output (Cout).

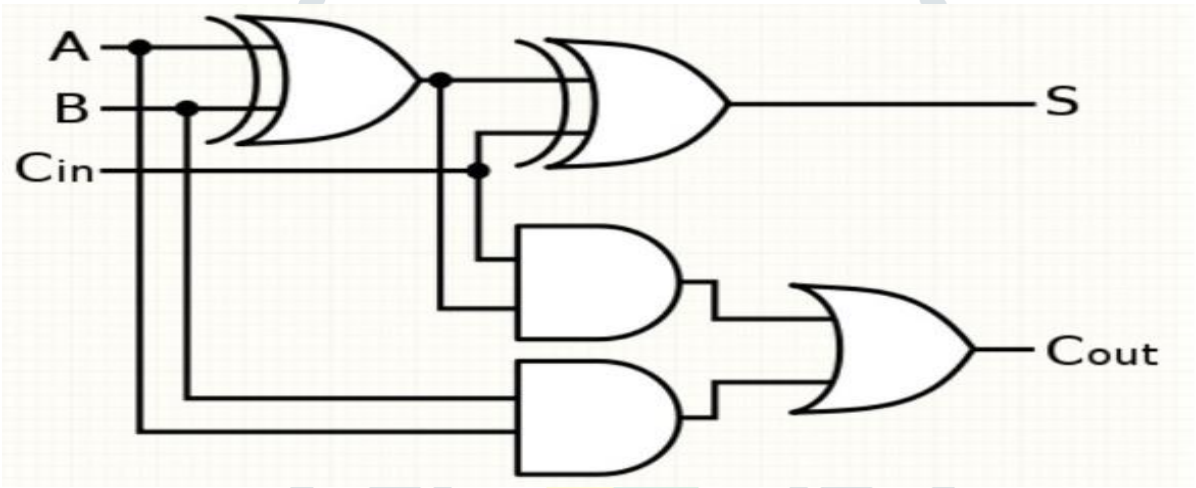

Fig. Conventional Full Adder Circuit

As per the Boolean equations obtained by reducing K-map, we get equations of Sum and Carry-Output for basic full adder circuit.
Sum = A⊕ B ⊕ C
Carry = A.B + Cin(A⊕B)

Truth Table:

Inputs			Outputs	
A	B	C_{in}	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Fig. Truth table of full adder

3.2 Review of 28T Full Adder Circuit using CMOS Technology

With the implementation using CMOS Technology, Conventional adder circuit is very easy to design. Libraries were designed for 90 nano meter and 65 nano meter gate-length transistors, and the circuit diagram was divided into Pull-Up and Pull-Down networks. 28 Transistors were used (14 NMOS + 14 PMOS) to build the desired circuit diagram [11].

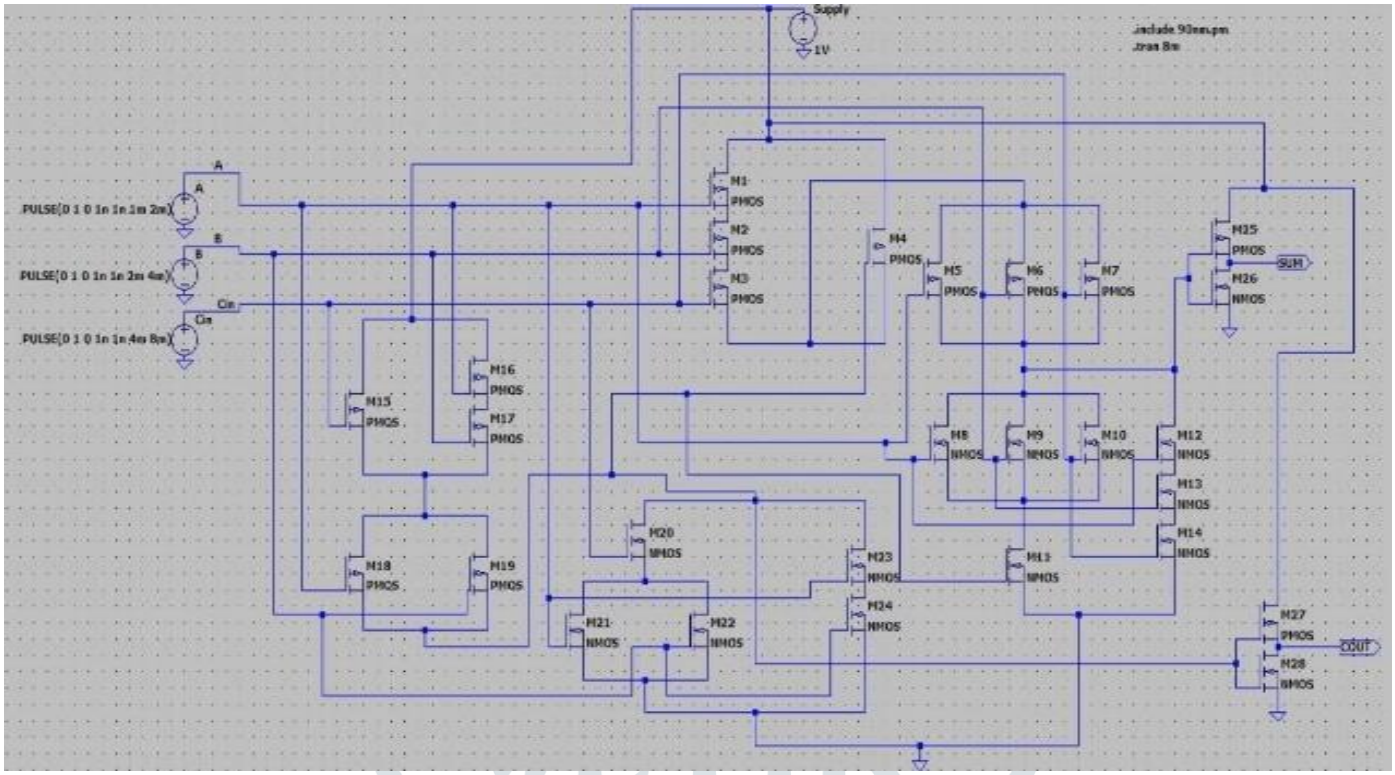

Fig. Implementation of 28T Full Adder Circuit using CMOS Technology [11]

In this study, researchers compared the power dissipation of a conventional full adder circuit to its performance when implemented using a 65nm transistor technology. The results showed that the conventional circuit exhibited a power dissipation of 153.77 Micro Watts, while the version using the 65nm technology demonstrated a reduced power dissipation of 101.45 Micro Watts. This comparison highlights the benefits of utilizing smaller transistor technology, as it significantly improves power efficiency. By leveraging the advantages of the 65nm technology, microprocessors and integrated circuits can achieve higher performance with reduced energy consumption. This advancement has significant implications for designing energy-efficient electronic devices like laptops, cell phones, and other portable gadgets, ultimately extending their battery life and contributing to a more sustainable technological ecosystem.

IV. OPTIMIZED FULL ADDER DESIGN FOR ENHANCED ALU PERFORMANCE

4.1 Implementing EXOR logic using Multipliers

XOR logic is a mandatory logic operation to perform for both Sum and Cout operations. It takes two inverters to get a complement for each input, but the way in which the logic has logic applied plays a major role in optimizing the speed, power, area and power dissipation. To reduce the number of components utilized, we use 2:1 MUX, which has 3 inputs, A (1) and its complement $\bar{A}$ (2) with a select input. This circuit design requires only 1 inverter, which results in the reduction the number of components but still getting the same output. We just need three 2:1 MUX to design a full adder [2].

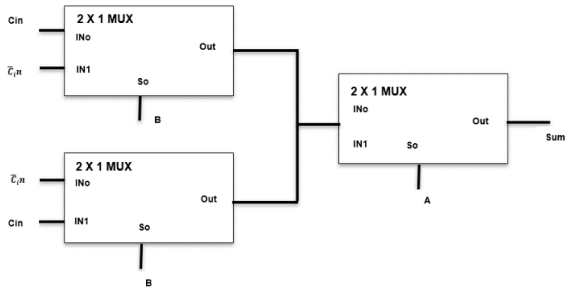

Fig. Sum bit using 2:1 Mux

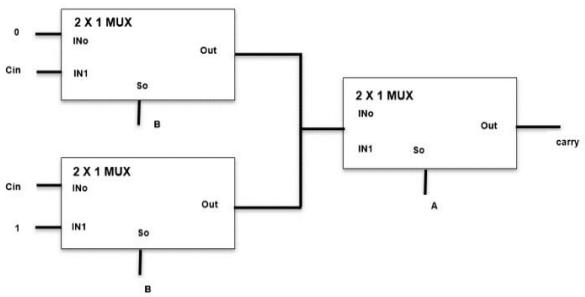

Fig. Carry bit using 2:1 Mux

4.2 Implementing Optimized Design using PTL (Pass Transistor Logic)

The CMOS design family is commonly used but has some limitations, such as requiring a relatively large area. To address this, other solutions have been developed, including Pass Transistor Logic (PTL). PTL allows primary inputs to operate at source and drain terminals in addition to gate terminals, reducing the number of transistors needed for a given logic design and resulting

in faster switching times. Researchers have found that using PTL can reduce the number of transistors needed to implement logic gates, such as a 2-input AND gate, from 6 transistors using standard CMOS to only 4 transistors [11].

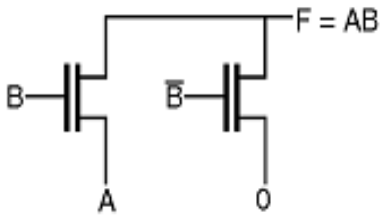

Fig. AND Gate using Pass Transistor logic

V. POWER DISSIPATION IN ADDER CIRCUITS

When implementing a full adder in hardware, power dissipation is an important consideration. The power dissipation of an adder design depends on various factors such as the circuit topology, the size of the transistors used, the operating frequency, and the input data pattern. Some of the factors that contribute to power dissipation in adder designs are: Capacitive loads, Switching activity and Voltage swings. To reduce power dissipation in full adder circuits designs, designers can use techniques such as optimizing the circuit topology, using low-power transistors, reducing the operating frequency, and using data-dependent power gating techniques. These techniques can help to reduce power dissipation while still maintaining the desired performance [5].

VI. PROPAGATION DELAY IN ADDER CIRCUITS

Propagation delay is a crucial factor in the performance of digital circuits, particularly in adder circuits where it refers to the time taken for the output to change in response to a change in input. The generation of a carry signal, which occurs when the sum of two binary digits exceeds the maximum value that can be represented, adds to the complexity of the circuit and can affect its propagation delay. The size and complexity of the adder circuit, as well as the technology used to implement it, also play a significant role in determining the propagation delay. Designers can use various techniques to reduce the propagation delay. Pipelining involves dividing the adder circuit into smaller stages, which decreases the overall propagation delay, while parallelism involves using multiple adders to perform multiple additions simultaneously and thus improve the speed of the circuit. Techniques like pipelining and parallelism can be employed to reduce propagation delay, enhancing the speed and efficiency of adder circuits in digital designs [5].

VII. POWER DELAY PRODUCT (PDP) IN ADDER CIRCUITS

In this study, the focus was on optimizing the PDP of an adder circuit by implementing various techniques. The researchers explored different approaches to enhance power efficiency. One strategy involved optimizing the circuit topology to ensure it was designed in the most effective manner. LPT were utilized to reduce energy consumption. Furthermore, the researchers lowered the operating frequency, striking a balance between speed and power usage. This approach aimed to achieve the desired delay while consuming less power. Another innovative technique applied in the study was data-dependent power gating. By implementing these power-saving techniques, the researchers successfully reduced the PDP of the adder circuit, making it more energy-efficient. This work holds promise for developing power-conscious electronic devices, meeting the increasing demand for longer battery life and eco-friendly technology [1].

VIII. OPTIMIZED DESIGN USING PTL LOGIC

PTL logic designs can be more power-efficient compared to other logic families due to the reduced voltage swings and low short-circuit power. However, it is essential to ensure proper sizing of the PMOS and NMOS transistors to maintain the correct logic functionality and minimize the propagation delay. The exact circuit parameters and transistor sizes need to be determined based on the technology which is being used and the specific requirements of the design like speed, power and area etc. A detailed transistor-level design and simulation would be required to validate and optimize the full adder circuit for a specific process technology. According to the opinion of various researchers, this optimized full adder design using XOR gates and PMOS, NMOS transistors provides an efficient way of implementing full adder circuit with reduced power consumption and propagation delay. But in practical applications, we would need to ensure proper sizing and design considerations based on the specific process technology and design requirements. It should be optimized in all the ways and should lead to considerable change.

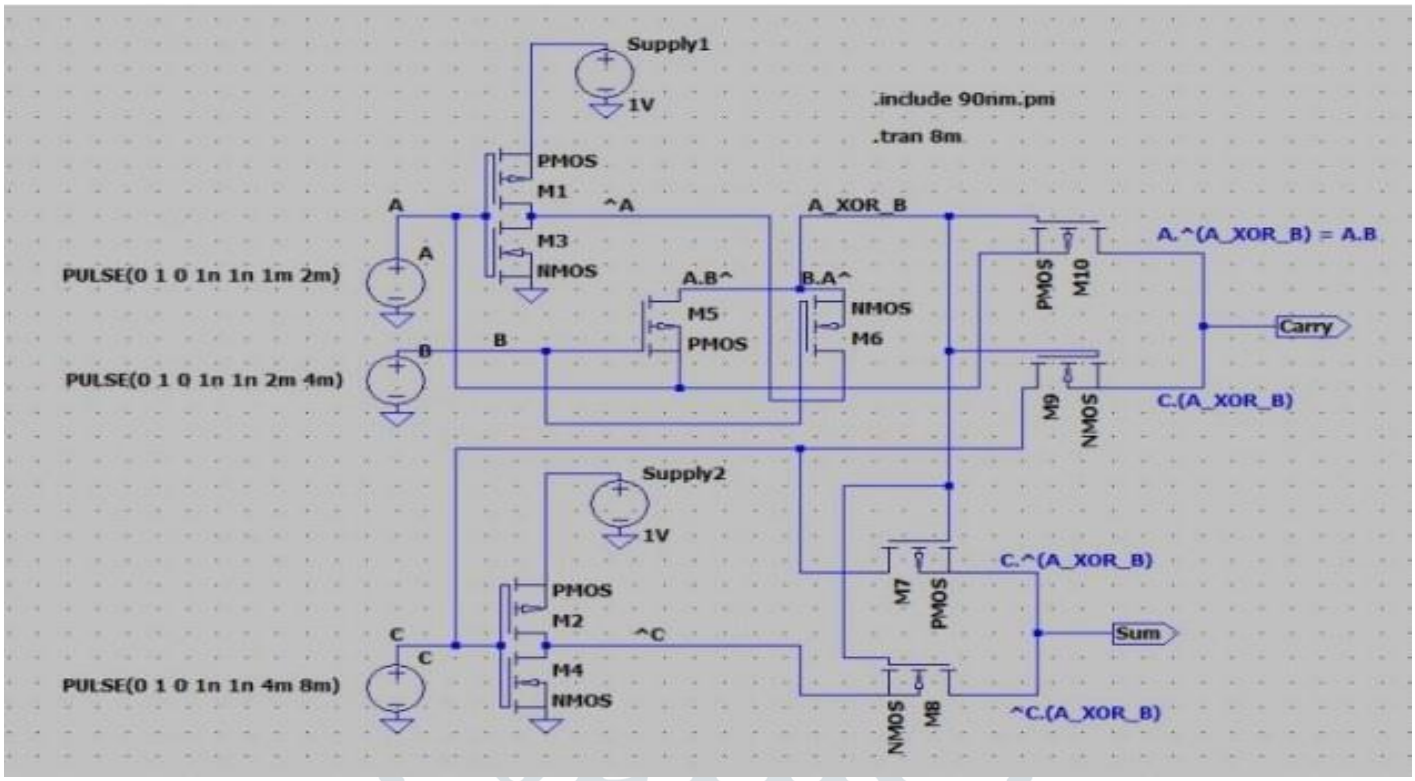

Fig. Implemented Optimized Design using PTL (Pass Transistor logic) [11]

IX. RESULTS AND DISCUSSION

After referring to various papers, we have tabulated the results obtained by them. The 65nm circuit design exhibit the lowest power consumption for the 2:1 Multiplexer based PTL Logic circuit. The optimized adder has also been implemented in 90nm and 65nm Technology, and they found that the proposed adder design consumes 97% less power than the conventional full adder [1].

Design	Power Dissipation(µW)	Propagation Delay(ns)	PDP (Power Delay Product) (µW.ns)
Conventional Full Adder (90nm)	153.77	264.68	4.07e+4
Conventional Full Adder (65nm)	101.45	332.61	3.37e+4
Optimized Full Adder (90nm)	2.163	31.235	6.7e+1
Optimized Full Adder (65nm)	0.688	86.819	5.9e+1

Fig. Result Analysis

X. CONCLUSION

This paper reviews a low-power Full Adder with minimum number of transistors used. It has used two 2:1 MUX, two not gates, with Pass Transistors, resulting in a significant reduction in power consumption. Researchers had performed the simulation using 90nm and 65nm technology to find out the efficiency of new optimized design. Results showed that 65nm 10T Full Adder is the best choice with better performance and less area, having the minimum PDP out of all the circuit designs, and most of the observed noise is removed [3]. Thus, we can say that, we have successfully the reviewed the work of different researchers on optimized full adder circuit into the ALU, resulting in a significant improvement in the unit's performance. The ALU now operates with a faster processing speed, allowing it to perform complex operations in a shorter amount of time. This improvement has led to an increase in the overall efficiency and effectiveness of the system. We believe that this optimization will bring a noticeable difference in the system's performance, particularly in applications that demand high computational power. Now we are confident that we will continue to make further improvements in the future [3].

XI. FUTURE SCOPE OF THE WORK

Taking the researcher's work into consideration, it's evident that their new design holds a lot of promise. This design has shown that it can improve the performance of electronic gadgets, especially when implemented using cutting-edge technologies like the 16nm or 9nm technologies. It could help devices last longer on a single charge and even be made smaller. By using this design, we could create electronics that perform well and also help the environment. It's clear that there's an opportunity to make this design even better in the future.

ACKNOWLEDGMENT

I express my sincere gratitude to Dr. K B Ramesh, Associate Professor at RV College of Engineering, Bengaluru, for his valuable guidance and collaborative efforts in completing this review paper titled 'Optimizing Conventional Full Adder Circuit for Enhanced ALU Performance.' Dr. Ramesh's expertise and insights significantly enriched the content of this paper, and our combined dedication contributed to its successful completion. Additionally, I extend my thanks to the academic community, researchers, and authors whose work served as the foundation for our analysis. Lastly, I am thankful to my family and friends for their unwavering support during the preparation of this paper.

REFERENCES

[1] Shaik, Dilshad, and Sai Krishna Santhosh Gollapudi. "Analogy of Distinct Constructions of FinFET GDI Full Adder." International Journal of Intelligent Systems and Applications in Engineering 11, no. 1s (2023): 120-135.

[2] Ahmadpour, Seyed-Sajad, Nima Jafari Navimipour, Mohammad Mosleh, Ali Newaz Bahar, and Senay Yalcin. "A nano-scale n-bit ripple carry adder using an optimized XOR gate and quantum-dots technology with diminished cells and power dissipation." Nano Communication Networks (2023): 100442.

[3] Fei, Lee Chen, Siti Husna Abdul Rahman, Krishnan Subramaniam, and Ahmad Anwar Zainuddin. "Design and Analysis of Full Adder Using 0.6 Micron CMOS Technology." Malaysian Journal of Science and Advanced Technology (2023): 11-16.

[4] A. Chauhan, A. K. Meena and A. Kumar, "Performance Analysis of 4-Bit Multiplier using 90nm Technology," 2022 2nd International Conference on Intelligent Technologies (CONIT), Hubli, India, 2022, pp. 1-5, doi: 10.1109/CONIT55038.2022.9848209.

[5] T. Mendez and S. G. Nayak, "Performance Evaluation of Fault-Tolerant Approximate Adder," 2022 6th International Conference on Devices, Circuits and Systems (ICDCS), Coimbatore, India, 2022, pp.1-5, doi:10.1109/ICDCS54290.2022.9780792.

[6] A. Yadav, "Optimizing Leakage Current and Fluctuations at Ground Rail in 1-bit 8T Full Adder Circuit Using Various MTCMOS Techniques," 2022 4th International Conference on Inventive Research in Computing Applications (ICIRCA), Coimbatore, India, 2022, pp. 174-179, doi: 10.1109/ICIRCA54612.2022.9985706.

[7] S. Narendran and B. T. Geetha, "Performance Analysis of Parallel FIR Digital Filter Based on Even Symmetric Fast FIR Algorithm using Different Adders," 2021 5th International Conference on Electronics, Communication and Aerospace Technology (ICECA), Coimbatore, India, 2021, pp. 155-160, doi: 10.1109/ICECA52323.2021.9675965.

[8] Y. -Y. Chu, S. -H. Shieh, H. Feng, H. Deng, M. -S. Shiau and D. -C. Huang, "A High-Speed Carry-Select Adder with Optimized Block Sizes," 2021 IEEE 15th International Conference on Anti-counterfeiting, Security, and Identification (ASID), Xiamen, China, 2021, pp. 182-186, doi: 10.1109/ASID52932.2021.9651488.

[9] P. Balasubramanian, R. Nayar and D. Maskell, "An Approximate Adder with Reduced Error and Optimized Design Metrics," 2021 IEEE Asia Pacific Conference on Circuit and Systems (APCCAS), Penang, Malaysia, 2021, pp. 21-24, doi: 10.1109/APCCAS51387.2021.9687757.

[10] G. T, L. T, Y. Srivastava and A. J. P, "Optimization of EOR and ENOR for Design of Full Adders with Efficient Transistor Sizing," 2021 5th International Conference on Trends in Electronics and Informatics (ICOEI), Tirunelveli, India, 2021, pp. 107-112, doi: 10.1109/ICOEI51242.2021.9452889.

[11] Srujana, Kotthapalli & Shivani, Kummari & Thirumalesh, Kuruva & Lakku, Yashaswi. (2020). Optimizing Conventional Full Adder Design for Power-Efficient Applications. Journal of VLSI and Computer Systems.