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Design a Low Power Flash Type ADC with different encoders for high speed applications

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Abstract

Analog to digital converters (ADC) are extremely important in today's environment. Flash type ADCs are the high speed among the available ADCs. In this paper, the design of Flash ADC structure uses a resistor string to generate reference voltages which are provided to each comparator for comparison with the input voltages. Comparator design is the crucial part of the Flash ADC architecture and used a Cascaded stages CMOS comparator, where each step contributes to boosting gain, sensitivity, and lowering noise of all kinds. One more important part in this ADC is Encoder design; here used a Wallace tree encoder and Heterogeneous encoder in this paper. The designed flash ADC consumes 9.280mW, 53.45ns delay and 11.583mw, 25.39 ns with respect to Wallace tree encoder and Heterogeneous encoder when operated in voltage of 1.2V. The design of A 4-bit flash ADC constructed with 180nm CMOS technology and the results are simulated.

Keywords: Flash type ADC; Comparator, Wallace tree and Heterogeneous encoder.

1. Introduction

Microelectronic devices and high-end instruments are becoming increasingly sophisticated and capable of performing a wide range of activities with high precision. In nature, real-world signals are analog signals from numerous sources and sensors have values that are constantly changing that can detect movement, temperature, sound, or light, and numerous digital systems monitor analogue signals from these transducers to communicate with their surroundings [4].Whereas Continuous signals are possible and offer an infinite count of possible voltage values, digital circuits only have two distinct states, a logic "1" (HIGH)/ a logic "0" (LOW). As a result, an electrical circuit capable of converting between the two domains of continually changing analog and discrete signals are required. Flash ADC is one such simple design utilized for converting continuous time changing signals to digital signals. Flash ADCs are mostly employed in high-speed applications and have a high power consumption. Satellite communication, data gathering, radar processing, and high-density disk storage are all applications for flash ADC.

2. Flash ADC architecture

In order to provide an equivalent output code for a specific n-bit resolution, parallel "Flash" A/D converters connect but space out a number of comparators with equal spacing and reference voltages produced by a number of precision resistors. The benefit of parallel converter also called flash converters, has to do with they are simple to develop and no timing clocks are necessary since a reference voltage is used to compare an analog voltage provided to the comparator inputs to [6].

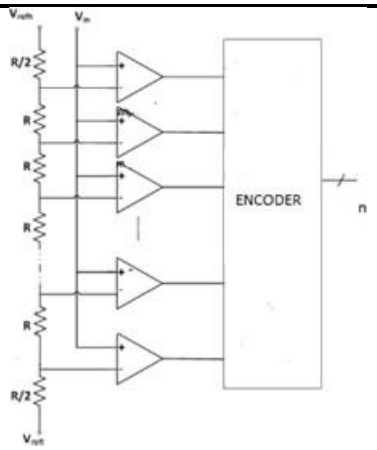

Fig.1. Flash ADC Architecture

N-bit flash ADC is made up of 2^N resistors, number of comparators are $2^N - 1$ and an encoder. At first, the input signal is fed to 2^N-1comparators where N is the resolution in the ADC. For a 4-Bit flash ADC, 16 resistors and 15 comparators are required [7]. Each comparator produced by the resistor strings used in a flash ADC is given a Vref. The resistor string circuit is employed for generate reference voltage which is used as one of the inputs to the comparator. Here reference voltage, which is produced from resistor ladder circuit as it descends from top to bottom because voltage decreases across the resistor. The voltage divider network arrangement yields V_{RF} using equivalent resistors. For example, the Vref level is certainly equal to half of the supply voltage or V/2, if the two resistors have equal values, or if R1 = R2. An analog comparator has two analog inputs that is applicable to contrast two distinct voltage levels' magnitudes include a positive and a negative input [8]. One of the comparator's inputs is given input voltage (V_{IN}) signal, and the other receives a reference voltage (V_{REF}). Two levels of voltages are compared at the comparator's input is made to choose one of two possible states for the comparator's digital logic output: "1" or a "0" [9]. The output of the comparator is the thermometer code. The thermometer code is then altered into binary code by the $2^N - 1$ to N encoder [10]. A combinational circuit known as an encoder transforms binary data from 2N input lines into N output lines, which represent the input's N bit code.

1.1. Comparator:

The schematic diagram of the comparator, which converts input voltage to logic 1/0, is the ADC architecture's most essential element. The voltage comparators evaluate the variation between the input and reference voltages. generated from the resistor string.

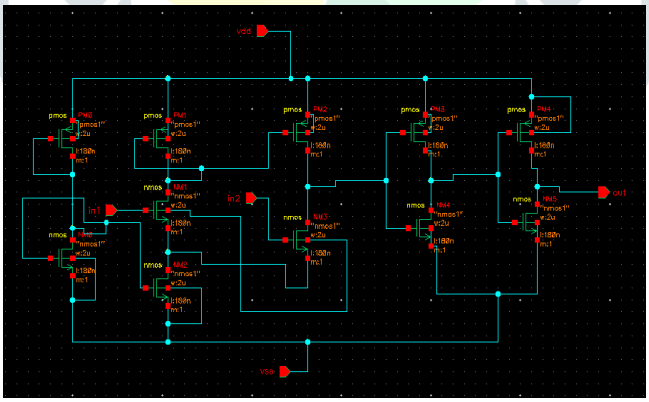

Figure .2. Schimatic Diagram of CMOS Comparator

There are plenty other comparators available, including discrete, RDC (Resistor Driving Comparator), open loop, differential, Domino logic, and pseudo dynamic latched comparators. However, for high-speed applications, Flash ADC needs a comparator with high sensitivity, gain, and low power consumption. A CMOS comparator with cascaded stages was employed here, and with each stage, both gain and sensitivity increased as the noise levels decreased. The output of the pre-amplifier stage, which is the first step, is fed into the decision stage's input. The decision-making stage is

followed by the post-amplifier stage. V_{REF}, the reference voltage is compared to V_{IN} that is used to the other input. The comparator output is "OFF" if the input voltage falls below the reference voltage ($V_{IN} < V_{REF}$), and "ON" if the input voltage exceeds the reference voltage ($V_{IN} > V_{REF}$). Result is, the comparator compares the two voltage levels and determines which is greater.

1.2. Wallace tree encoder:

This encoder block is essential to obtain the accurate the applied binary values analog input signal. It changes a sequence of 0s and 1s from comparators to binary format. The combinational circuit known as the encoder transforms binary information from 2N input lines are converted into N output lines, representing N bit code for the input. It is expected that there is only one active one input line at a time for straightforward encoders.

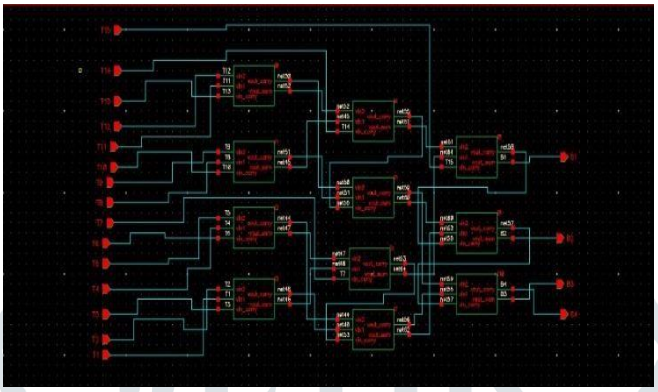

Fig.3. Schematic Diagram of Wallace tree encoder

This paper contains the encoder is carried out employing the Wallace tree design, which includes full adders. The equation gives the number of complete adder cells required to create an N bit encoder,

$$X_N = \sum_{i=1}^{N} (i-1)2^{(N-1)}$$

As a result of the quantity of ones and it is also referred to as a one's counter and provides binary output in compliance. This encoder turns comparator output into accurate binary output even when bubble faults are present. The Wallace tree encoder uses less electricity than a ROM-based encoder. Another benefit of this encoder is that the propagation delay is equal because all inputs pass through an equal amount of complete adders. It is also flexible and generates positive results for any settlement.

Full Adder:

Here designed a full adder with the help of 2:1 Multiplexers.

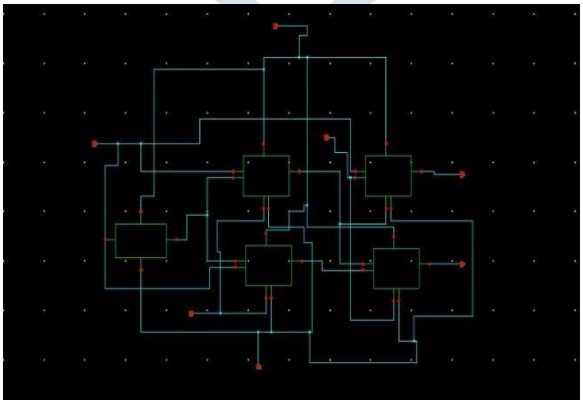

Fig.4. Schematic Diagram of Full Adder

1.2.1.1. Multiplexer:

A circuit called a multiplexer that combines 2^n input lines with only one output line. A multiplexer serves as a combinational circuit with a lot of inputs and one output. The output line receives and transmits binary data that is received based on the input lines. According to the selection line values, it will be connected to the output by one of these data inputs. In this project, a 2:1 multiplexer is used. In the 2:1 mux, there are only two inputs and a single output. Based on a variety of inputs which attend to the selection line S, It will be connected to the output from one of these two inputs. We know that multiplexer is also called a data selector. Here, the Multiplexer is designed with Modified GDI (Gate Diffusion Input) logic.

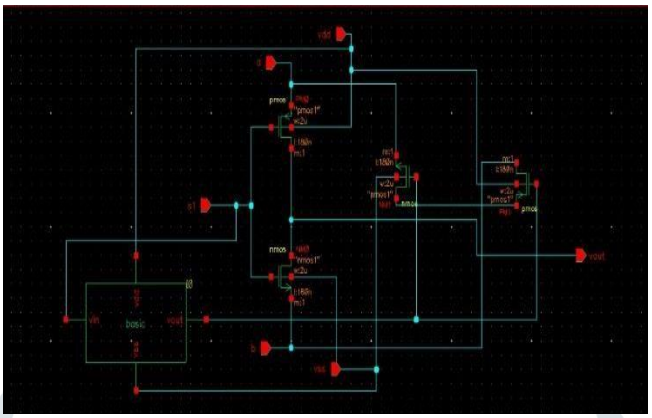

Fig.5. Multiplexer Schematic Diagram

1.3. Heterogeneous encoder

Any existing encoder, such as the Wallace tree encoder or the Fat tree encoder, can be used to construct a heterogeneous encoder. Seven multiplexers, two inverters, and four complete adders make up the heterogeneous encoder. Actually, we can't give input directly to the output in cadence virtuoso. So, two inverters used in the circuit. Wecan use buffer circuit in place of two inverters. Also, two cascaded inverters act as buffer circuit. The inputs to the encoder are 15 (T1 – T15) and it produces 4 outputs (B4-B1). This can tolerate bubble errors and allow the remaining signals to serve as inputs. The Wallace encoder is likewise without of bubble error, although circuit is complicated. As a result the heterogeneous encoder is simple to implement and usage a little power.

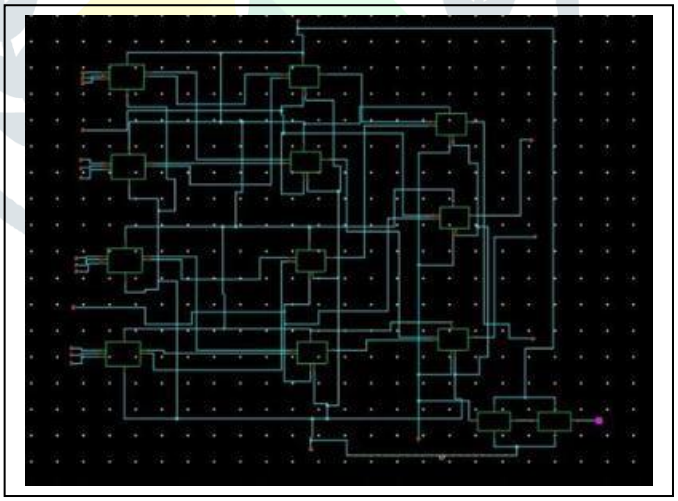

Fig.6. schematic diagram of heterogeneous encoder

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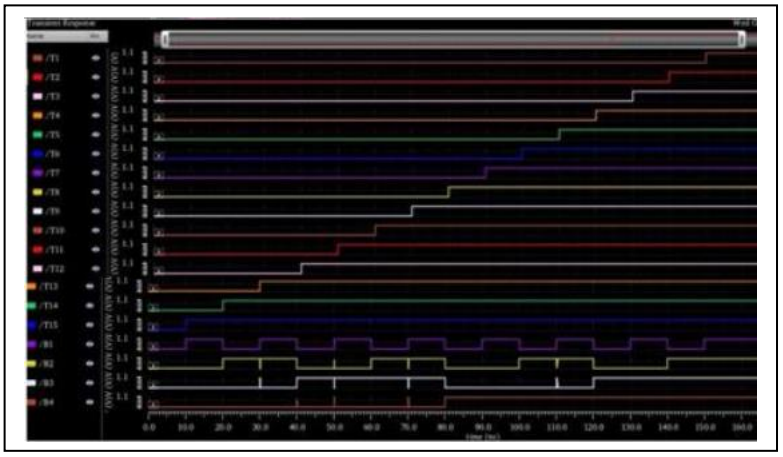

Fig.7. simulated waveforms of heterogeneous encoder

1.4. Flash ADC:

Finally Designed the Flash ADC architecture with a two-stage CMOS comparator and two types of encoders (Wallace Tree Encoder and heterogeneous encoder). The reference input voltage is sent to the inverting pins of comparators, even though analog the input signal is sent to the comparator's non-inverting pin. The comparator compares both inputs and outputs the results in the form of 1s and 0s. If the input voltage exceeds the reference voltage, then the output of the comparator is 1. If the input voltage is less than the reference voltage, then the output of the comparator is 0. The set of 1's & 0's is called thermometer code. Here one thermometer to binary code converter is needed. So, the Wallace Tree encoder is used for that conversion. The encoder output is in the form of binary and this output is called a digital output.

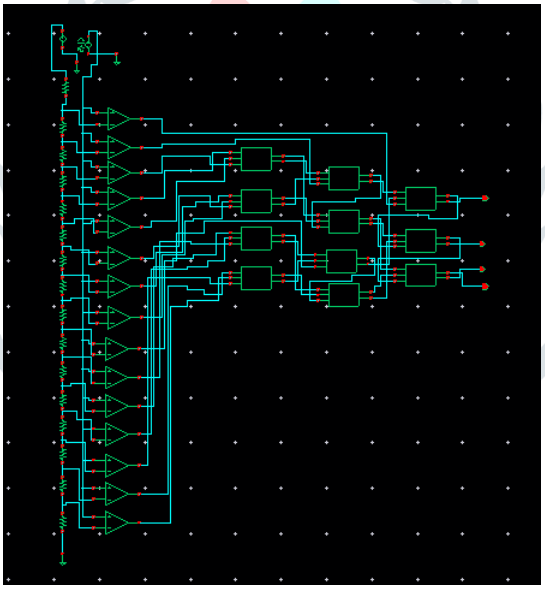

Fig.8. Schematic Diagram of Flash ADC

2. Results

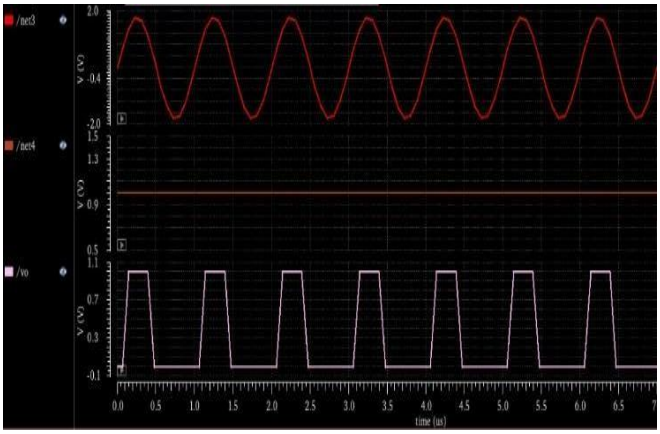

Fig.9. Simulation waveform of CMOS comparator

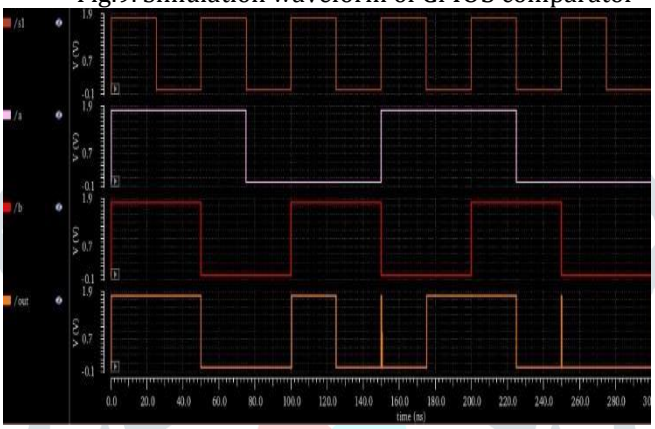

Fig.10. Multiplexer simulation result

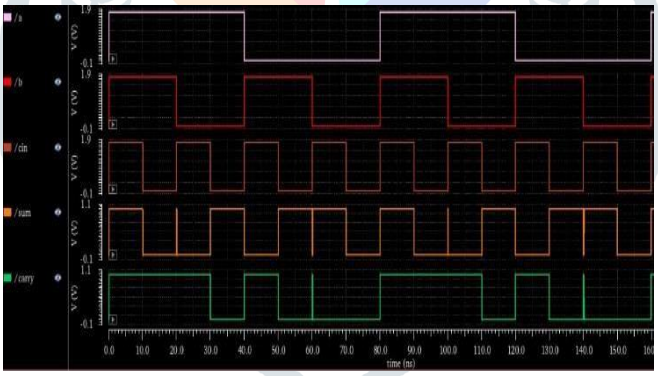

Fig.11. Full Adder Simulation result

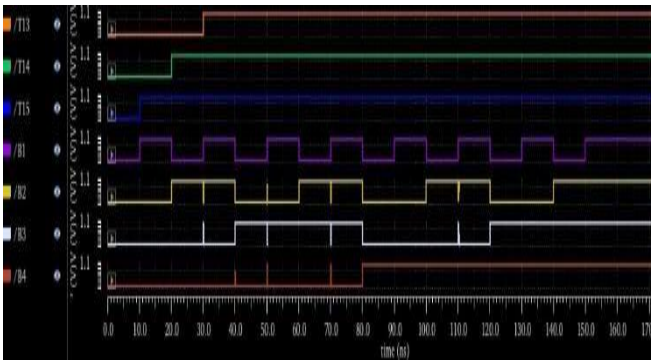

Fig.12. Simulation waveforms of Wallace Tree Encoder

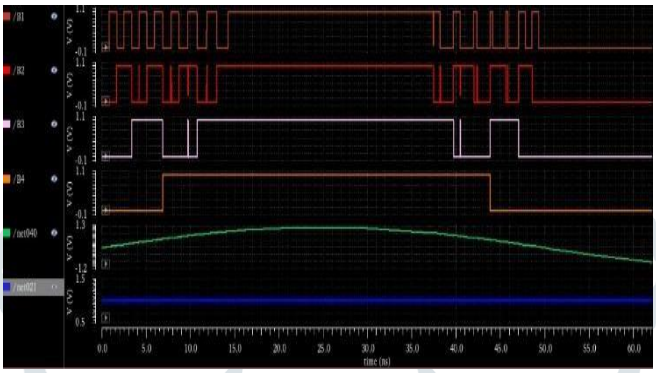

Fig.13. Simulation results of Flash ADC

Parameters	ADC with Wallace tree	ADC with Heterogeneous encoder
Vdd (V)	1.2	1.2
Technology	180nm	180nm
Resolution	4-bit	4-bit
Frequency	10 MHz	10 MHz
Delay	53.45 ns	25.39 ns
Power consumption	9.280 mW	11.583 mW

Table 1: Flash ADC Comparison

3. Conclusion

This paper designed a flash ADC with Wallace tree-based encoder or heterogeneous encoder, CMOS comparator with cascaded stages, and string of resistive ladder network. Designed circuit is 180nm CMOS technology was used to simulate. This ADC's has the significant advantages with low power usage and short latency. When this ADC designed with Wallace tree encoder, we observe the 9.280 mW power consumption, 53.45 ns delay and ADC with heterogeneous encoder design has 11.583 mW, 25.39 ns. Both circuits operated as input of 1.2V at a frequency of 10MHz. The Flash ADC created can be used in high-speed applications.

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