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Implementation of Power Efficient CMOS D Flip Flop using Leakage Reduction Technique

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***Abstract*—Leakage power is of paramount importance in CMOS technology. Power consumption may be reduced and the battery backup time extended by reducing the voltage supplied to the designated circuit when it is in standby mode.CMOS D flip-flops (FFs) have a rather high-power consumption, and digital systems may benefit considerably by optimizing their FFs' power usage. A power-efficient CMOS D FF (PECDTG) using Transmission gate is proposed. The suggested PECD FF only performs precharges when they are necessary thanks to their input-aware precharge approach. Energy efficiency is maintained without increasing the PECDTG FF's size by floating node analyses and transistor level optimisation. D type CMOS flip flop circuits use an adapted SVL approach to suppress signals and lower power consumption from leakage currents while the device is in standby mode. Further, the suggested layout requires fewer clocked transistors, cutting down on both dynamic power usage and leakage current. The proposed FF uses less power than a regular CMOS D-type flip-flop at 10% data activity and 0.7 V supply voltage thanks to the use of 90- nm CMOS technology.**

***Keywords*—CMOS, Leakage Power, D-Flip Flop (D-FF), Delay, Cadence, Current Leakage**

I. INTRODUCTION

As the process has advanced, digital systems' performance has significantly improved, and power consumption has turned into a severe limitation. Due to the meteoric rise of the Internet, IoT devices have also found widespread usage in the IoT. The Internet of Things (IoT) has several applications. Just a few examples include transportation, healthcare, and intelligent settings. These low-power components are used in devices that are powered by batteries or by themselves. Flip-flops (FFs) are key components that account for a sizeable amount of the total power. FFs often account for 50% or more of the total energy needed to run random logic operations. In most SoC devices, flip-flops (FF) account for more than half of the random-logic power because of the redundant transition of internal nodes that occurs when the input and output are in the same state.Therefore, reducing the amount of power that FFs require may substantially reduce the amount of energy that digital systems need. The transmission-gate flip-flop, often known as the TGFF, is the kind of FF that is used in current digital systems the majority of the time.

Flip-flops and other bi-stable devices are employed primarily as one-bit memory cells. The logic 1 and logic 0 are the two possible states of a flip-flop. [1] The flip flop requires an external pulse as input to enter one of its two stable states. This steady state is maintained at the output until another pulse is utilised to alter it. By providing valid inputs apart from the trigger, we can alter the flip-flop's output. Most sequential circuits, such as counters and shift registers, rely on flip flops to perform an essential function.The D input of a delay flip flop [2] will remember any bit pattern that is passed into it. This allows additional digital circuit components to analyse the data byte to figure out how to proceed in difficult scenarios. On the gate level of Fig. 1 are depicted D-type flip-flops with positive-edge triggers. This kind of FF is used as a short-term memory device. By eliminating the unexpected output and the circumstance that arises when S=R=1, the D-FF makes up for the basic shortcoming of the Set Reset FF. Since it can 'latch' and store data, Figure 1 depicts a D flip-flop, which is also known as a Data FF; however, since one of its advantages is delaying the processing of data, it is also sometimes called a Delay flip-flop. Both terms refer to the same piece of equipment.

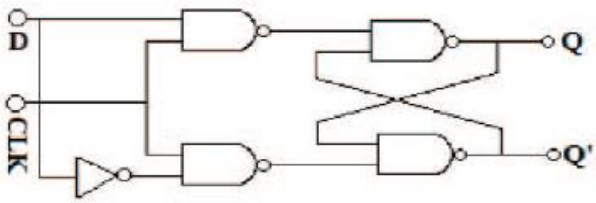

Fig. 1. D-type flip-flop gate diagram

Because the S=R=1 input combination leads to an ambiguous output, the simplest D Type FF [3] contains an inverter and a high-activation SR type to counteract the problem. The SR flip-flop's illegal and arbitrary states have been removed thanks to this improvement. D flip flops omit the S and R inputs and instead rely on a single D input to delay-multiply the clock pulse and transmit the input bit to the output.For devices like this, which rely on their power source or batteries, low-power design is of paramount importance [4][5][6][7]. Flip-flops (FFs) are fundamental building blocks of digital systems, contributing significantly to their overall performance [8][9]. As a result, digital systems may use much less energy if their FFs are made

more efficient. Power consumption in digital systems may be reduced using the voltage-scaling methodology, which has been shown to be an appealing strategy [10][11][12][13][14].

II. Conventional D type-CMOS Flip flop

In computers and many other electrical devices, flip-flops serve as the fundamental building component of digital electronics. The status of an electronic gadget is stored in a FF. The D FFs output is a replica of the input it receives. The letter D stands for "DATA" and stores the information found on the data line. In response to a clocking pulse, a logical state may be stored in a flip-flop electrical circuit for one or more data input signals. This can happen in conjunction with other states. Inverters can set and reset this D flip flop (FF). The get flip-flop may be put in motion with only one edge, whereas the DET flip-flop requires two. The clock's rising or falling edge may activate a single-edge triggered flip-flop, making it straightforward to manufacture. The TSPC D flip-flop architecture can be realized with only 5 transistors here. A 5-transistor TSPC D FF is seen in Fig. 2. Three NMOS and two PMOS transistors are used to construct this flip-flop. The modest number of transistors in this edge-triggered flip-flop allows it to occupy very little space. It decreases power consumption and uses just 5 transistors. By using just one phase of the clock, skew concerns are avoided and digital efficiency is increased in Clocked True Single-Phase (5T) FF. The reduction in required chip space and power consumption that results from removing skew [15] is substantial. The diagram for a 5T TSPC D-FF is shown in Figure 2. [16][17]

CLK and input D high deactivate P1 and N3 transistors, while the P2, N1, and N2 transistors are activated. The production rises dramatically. During the ON portion of the clock, the input value is converted into the output value.

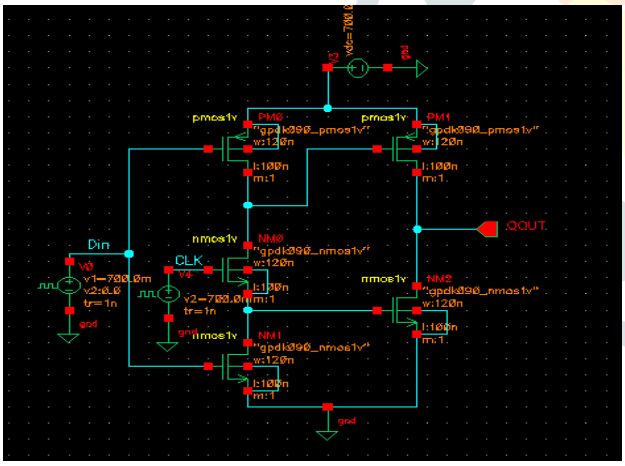

Fig. 2. CMOS D-Flip Flop

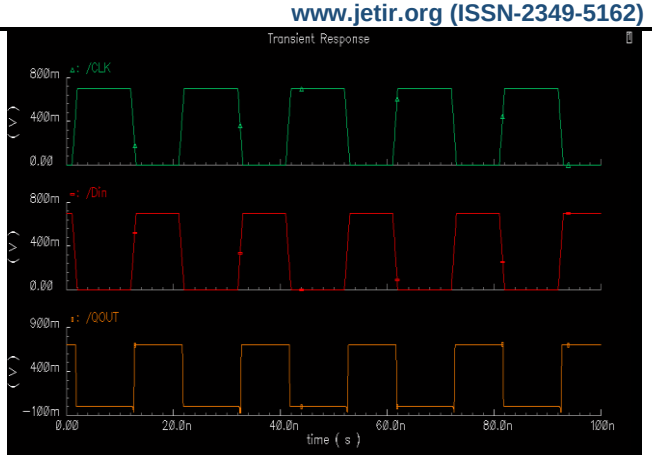

Fig. 3. CMOS D-Flip Flop Transient Response

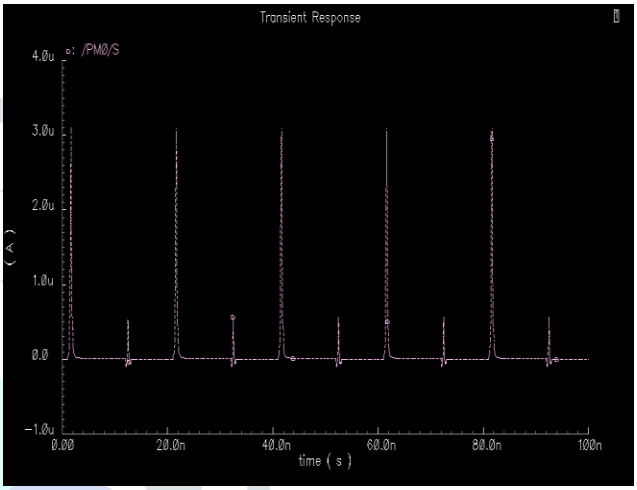

Fig. 4. Leakage Current of CMOS D-Flip Flop

III. Proposed Power-Efficient CMOS D FF (PECDTG) Using Transmission Gate

The power-efficient CMOS D FF (PECDTG) using Transmission gateis the FF that is utilized the most frequently in modern digital systems. The PECDTGschematic is depicted in Figure 5. The PECDTG is a near-threshold operation-capable, contention-free FF. To reduce FF's power usage, complementary clock signals should be used more selectively. The suggested PECDTGFF is free of contention and can operate at 0.7 supply voltages. In addition, in contrast to prior low-power FFs, the redundant precharge function has been entirely removed from the proposed FF, which has resulted in a further reduction in the amount of power that is required.

The transmission gates are furnished with clock pulses that mirror images of each other. When the clock pulse's leading edge comes, the TG-1's transistors, nmos and pmos, switch to the ON state and send the input signal via the gate. the TG-2, which also receives clock pulses that are fairly complementary to those received by the TG-1, stays in its OFF state since none of its transistors enters its active zone. The TG-3, which is subjected to the same clock pulses as the TG-2, also maintains its OFF state. The data is now transferred through TG-4, which has entered the ON state after receiving clock pulses identical to those of TG-1. The memory stage is now in play due to the fact that the input data is not directly sent to the output. D flip-flops' defining characteristic is their ability to hold onto the output of the preceding stage in the absence of a leading-edge clock pulse, a task performed by the device's "memory stage."

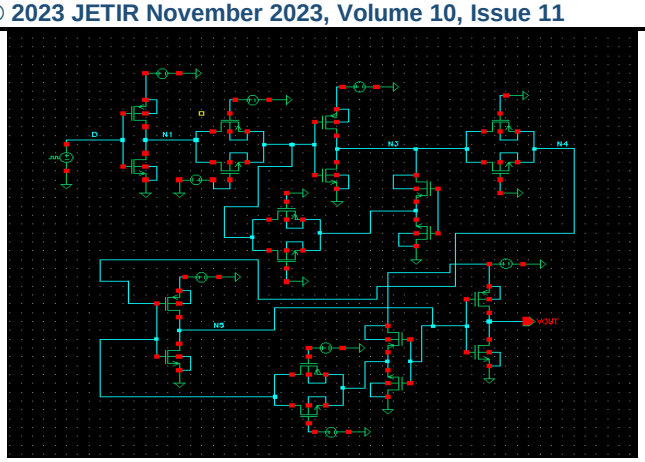

Fig. 5. Schematic ofpower-efficient CMOS D FF (PECDTG) using Transmission gate

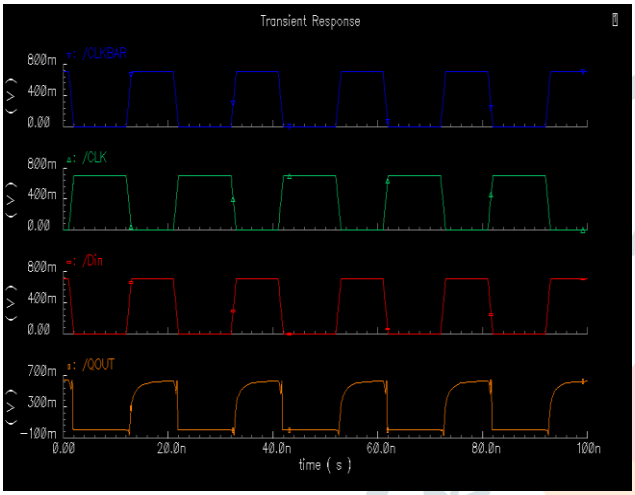

Fig. 6. Transient Response of power-efficient CMOS D FF (PECDTG) using Transmission gate

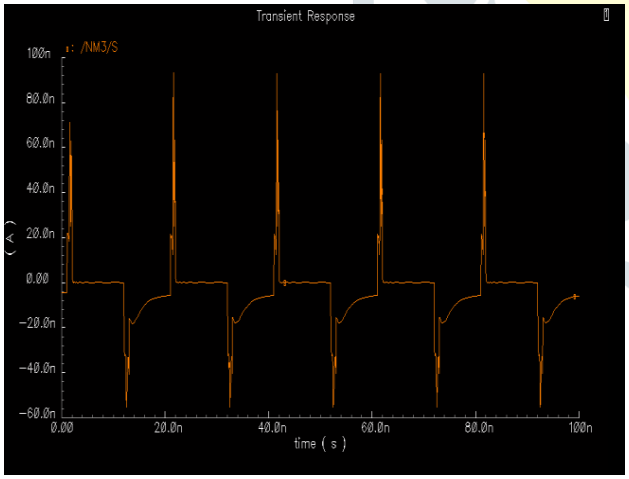

Fig. 7. Leakage Current of power-efficient CMOS D FF (PECDTG) using Transmission gate

IV. D-CMOS Flip Flop Leakage Reduction Methods

A. D type- CMOS Flip Flop with SVL Technique

Self-Voltage Level is an abbreviation for "Self-Voltage." During clock=0, the standby mode of operation for clocked devices like flip flops, the SVL approach is employed to limit leakage power.In the SVL method, pull-down and pull-up systems are implemented using NMOS and PMOS transistors connected in parallel. The clock signal's antipode, the gate of a pull-up transistor, is linked to the clock, and the gate of a pull-down transistor is connected to the clock. Controlling D-FF supply voltage using the clock signal, this method is able to significantly cut down on leakage power use. For this reason, "self-voltage level" is an appropriate moniker. Psw1 will be ON and Nsw1 will be OFF when clock = 1, clock bar = 0. We'll be hooking up the clocked circuit to Vdd.

When clock = 0, the circuit enters a power-saving standby mode and uses no further power. As a result, we may safely decrease the supply voltage when in standby mode and enjoy the benefits of lower power consumption and, in particular, lower leakage power (the amount of power that flows even when the transistors are turned off). Clocking in at 0 turns Nsw2 off.When employed as a pull-down, PMOS transistors produce a faulty logic zero—that is, they output Vth. The "virtual ground" node will receive a discrete voltage from the Psw2 PMOS transistor that has been connected as a pull-down rather than to ground. The pull-down clocked circuit's NMOS transistors' source terminal is connected to this virtual ground. A little positive voltage given to the source of an NMOS transistor will decrease its leakage current when the transistor is in the standby state. Similar to how Psw1 is OFF and Nsw1 is ON but produces faulty reasoning '1' when used for pull up, Psw1 is also OFF and Nsw1 is ON when used for pull up. In a timed circuit, the virtual supply [1] will have a voltage that is less than Vdd. This means that while the clock is at zero, the clocked circuit has the lowest possible leakage power.

SVL D-FF architecture is given in Figure 3. three NMOS (N1,N2,N3) and Two PMOS (P1 and P2) transistors construct the D flip-flop.

Case1: clock = 1(active mode)

Turn on Psw1, turn on Nsw2, turn off Psw2, and turn off Nsw1. For typical circuit functioning, connect Vdd and ground to the D-FF.

When D_in equals zero, it results in the activation of P1, N1, and N3, while P2 and N2 remain deactivated. Consequently, connecting Q to the ground is established, thereby setting Q equal to zero.

When D_in is equal to 1, the transistors P1 and N3 are in the OFF state, while the transistors N1, N2, and P2 are in the ON state. Additionally, the node Q is connected to the voltage source Vdd, resulting in Q being equal to 1.

- **Case2: clock = 0(standby mode)**

Both switches, Psw1 and Nsw2, are closed off (in the OFF state). By acting as a pull-up, Nsw1 supplies the D flip flop with a voltage between Vdd and Vth while the flop is active. The drop may be attributed to NMOS's resistant characteristic when used as a pull-up. The Psw2 switch is also active, but unlike the push-up switches, it supplies positive voltage rather than ground. In standby mode, the leakage power of the D-FF is reduced by a marginal extent due to the application of a virtual ground positive voltage that induces a tiny reverse bias on the NMOS transistors. In standby mode, the leakage power of PMOS transistors in a D flip flop is reduced by coupling them to a virtual supply [8].

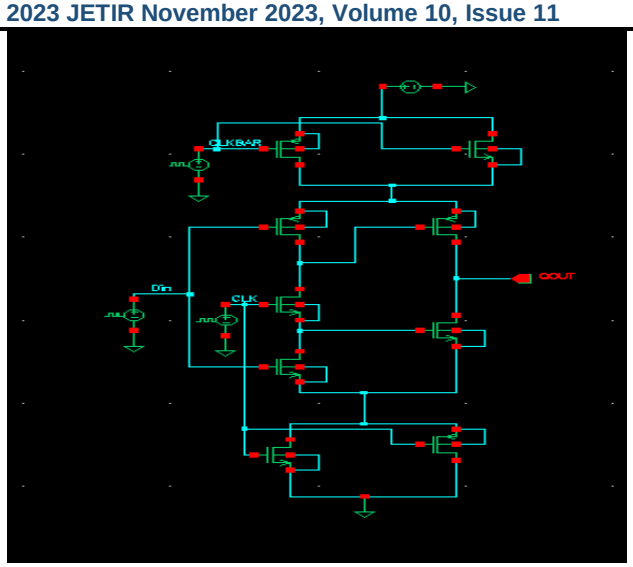

Fig. 8. D type CMOS Flip Flop SVL Logic Diagram

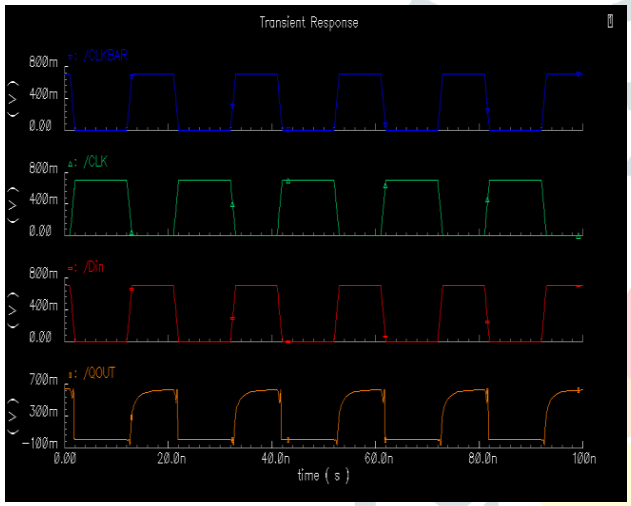

Fig. 9. Transient Response of D type –CMOS Flip Flop with SVL

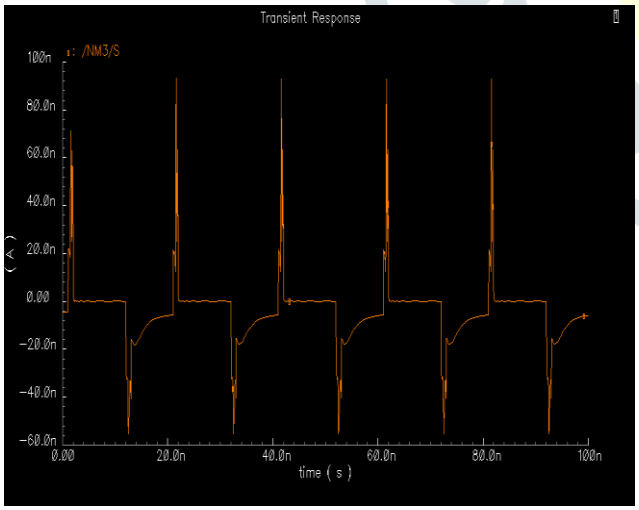

Fig. 10. Leakage Current of D-type CMOS Flip-Flops with SVL

B. D type- CMOS Flip Flop with Adapted SVL Technique

The development of a Delay FF that makes use of an Adapted SVL approach is seen in the accompanying figure, number 6. Five transistors, three NMOS (N1, N2, and N3) and two PMOS (P1 and P2), combine to create a CMOS Flip Flop of the D kind.

- **Case1: clock = 1(active mode)**

In this configuration, Psw1 and Nsw2 are both on, Psw2 and Psw3 are both off, and both Nsw1 and Nsw2 are off. For the D type -CMOS Flip Flop to function properly, it must be connected to both Vdd and ground.

By connecting Q to ground (representing a D_in=0 state) with P1,N1,N3 ON and P2,N2 OFF, we get Q = 0.

Q = 1 (connected to Vdd) if D_in = 1 (P2, N3 off, N1, N2, and P2 on), then P1, N3, and P2 off.

- **Case2: clock = 0(standby mode)**

All connections between Psw1 and Nsw3 are open. Nsw1, Nsw2 are both ON, but as pull-ups, they feed D flip-flop with a voltage of Vdd-Vth. Two NMOS transistors may be stacked to decrease the subthreshold leakage current. Similarly, Psw2 and Psw3 are both energised, but unlike Psw1, they function as pull-downs, supplying a positive voltage of a defined magnitude rather than zero.By gently reverse biassing the NMOS transistors of the D flip flop, this virtual ground positive voltage helps to lower leakage power [8] during standby. Flop the D's In the off state, Connecting PMOS transistors to a fictitious power source, which reduces leakage power. The leakage current and supply voltage in the enhanced SVL technique are reduced by stacking [7] NMOS transistors. Therefore, the static mode drastically reduces the power supply given to the fundamental FF circuit. Standby mode leakage power is minimised by the Improved SVL Technique because in static mode proportional to supply voltage and current. Not only does our design decrease leaking power, but also reduces the number of clocked [9] transistors, It helps the circuit run faster and reduce dynamic power usage a little bit more. We have applied this method to a D Flip Flop, but it is easily adaptable to any timed circuit in need of a static mode leakage power reduction.

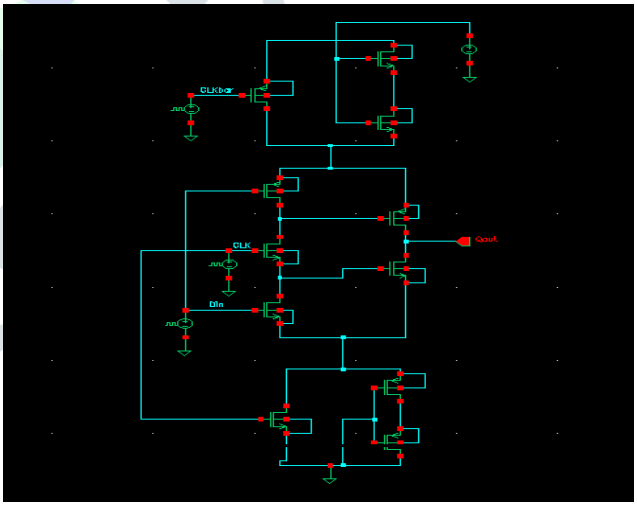

Fig. 11. Schematic of D type –CMOS Flip Flop with Adapted SVL

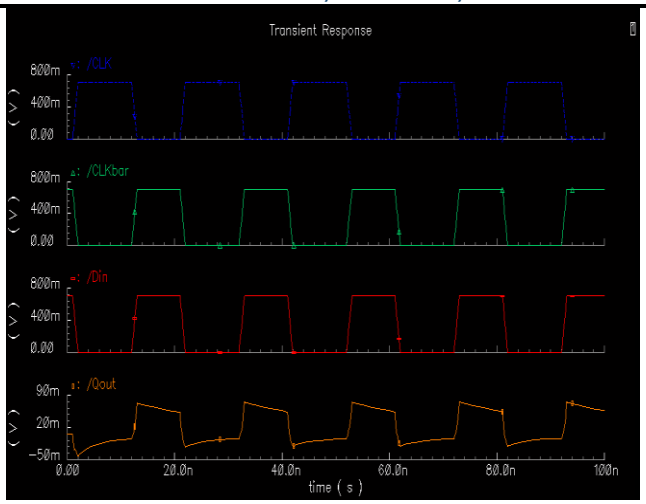

Fig. 12. Transient Response of CMOS D-Flip Flop with Adapted SVL

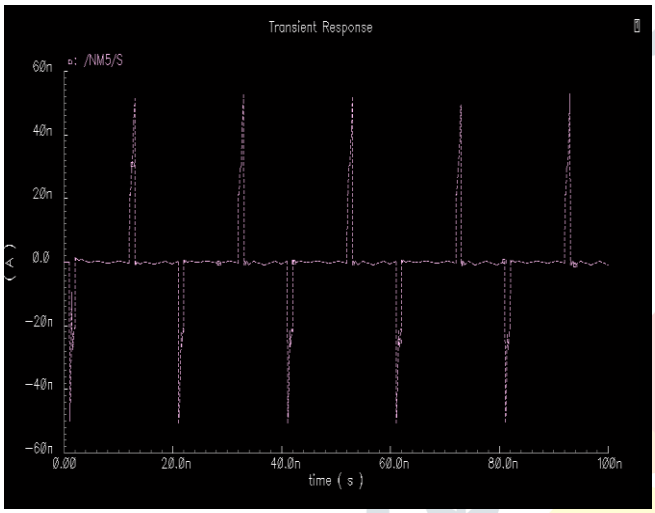

Fig. 13. Leakage Current of D type –CMOS Flip Flop with Adapted SVL

V. Simulation Result

Simulation of a CMOS D-Flip Flop and a power-efficient CMOS D FF (PECDTG) employing Transmission gate has been performed using the cadence tool at 90 nm with a Vdd = 0.7 V nominal supply voltage. Because gate leakage is the only significant mechanism at normal operating temperatures (around 27 °C), various circuits have been used to create power-efficient CMOS D FF (PECDTG), which reduces the maximum total leakage compared to the SVL technique and enhances the Leakage Current, leakage power, and Propagation Delay in D type -CMOS Flip Flops.

At 27 degrees Celsius, gate leakage is the sole dominant mechanism, and many methods have been developed to reduce power consumption without sacrificing performance in D-type CMOS flip-flops. Among these methods is the Adapted SVL technique, which, in addition to improving the parameters Leakage Current, leakage power, and Propagation Delay, also suppresses the maximum total leakage compared to SVL.

A. Leakage Power Analysis

Increases in leakage power, which occur when the length of a channel is shortened or a device is scaled down, are what keep electronics in a dormant state. Fig compares the leakage power of a traditional D-type CMOS FF with that of a power-efficient D-type CMOS Flip Flop (PECDTG) that makes use of a Transmission gate.Substrate injection effects and voltages below the threshold may both cause leakage current. The Schmitt trigger leakage power is defined as the amount of power that is lost during the trigger's operation.

$$P_{LEAK} = I_{LEAK} V_{dd}$$

D type -CMOS Flip Flop leakage power is denoted by P_LEAK, leakage current by I_LEAK, and power supply voltage by Vdd.

B. Propagation Delay

To lessen the need for a buffer and the energy needed to run it, CMOS D-Flip Flops are increasingly being employed. D type -CMOS Flip Flops excel due to their tunable threshold voltage, which may be set either higher than or lower than the voltage at which a buffer typically functions. Since a D type -CMOS Flip Flop's configurable low-voltage threshold allows it to function with more noise and voltage glitches than a buffer, it may be programmed to flip quicker than a buffer, reducing latency. Propagation delay refers to the amount of time it takes for a CMOS D-Flip Flop logic gate's output to change in response to a change in one or more inputs.

Power-efficient CMOS D FF (PECDTG) employing Transmission gate with D type -CMOS Flip Flop provides superior performance delay in 90nm and 45nanometer technology at supply voltage 0.7 V, as analyzed by means of a simulation. During a change in a signal, the through delay is calculated as:

$$Delay = 0.69 R_{eq} \times C_L$$

C_L is the load capacitance, and R_(eq) is the equivalent resistance of the feed through cell.

Table 1 illustrates the outcomes of comparing the methods used to implement a D type -CMOS Flip Flop with varying supply voltages.

TABLE I. Conclusions Based on Simulations

Performance Parameter	D type –CMOS Flip Flop	Power-Efficient CMOS D FF (PECDTG) Using Transmission Gate
Technology Employed	90nm	90nm
Voltage Supply	0.7V	0.7V
Leakage Power	12.1nW	8.4nW
Leakage Current	14.8nA	5.4nA
Propagation Delay	22ns	18ns

Table 2 shows the results of comparing the techniques used to implement a D type -CMOS Flip Flop with varying supply voltages.

TABLE II. Conclusion Based on Result Simulations

Performance Parameter	D type – CMOS Flip Flop	D type – CMOS Flip Flop with SVL	D type –CMOS Flip Flop with Adapted SVL
Technology Employed	90nm	90nm	90nm
Voltage Supply	0.7V	0.7V	0.7V
Leakage Power	12.1nW	4.4nW	2.3nW
Leakage Current	14.8nA	2.4nA	1.8nA
Propagation Delay	22ns	86ns	68ns

TABLE III. COMPARATIVE ANALYSIS WITH PREVIOUS RESULT

Performance Parameter	CMOS D FF [18]	Power-Efficient C(PECDTG) Using Transmission Gate
Technology Used	180nm	90nm
Low Power	1.54µW	8.4nW

VI. CONCLUSION

Because of the importance of minimizing power consumption in battery-powered circuits, we have set up a low-power, high-performance D-type CMOS Flip Flop using VLSI technology. Improve the circuit parameters leakage power, leakage current, and propagation delay in a D-type - CMOS Flip Flop and a power-efficient CMOS D FF (PECDTG) with a Transmission gate. During standby, the supply voltage to the designated circuit should have a lower value in order to reduce the amount of power that is being used and increase the amount of time that the battery backup has at its disposal. This research presents a comparative description of power-efficient CMOS D FF (PECDTG) using a Transmission gate. Vdd is the supply voltage, 0.35 V is the threshold, and 0.7 V is the input control voltage. To fully fulfill the PECDTG FF's promise for excellent energy efficiency without substantially increasing its footprint, floating node analysis and transistor level optimisations are also applied. A D-type CMOS flip-flop utilises more power than the planned FF, which employs 90-nm CMOS technology. With the Vdd supply voltage is 0.7 V, the Vth threshold is 0.35 V, and the Vcc input voltage is 0.7 V, this study provides a comparative analysis of SVL and Adapted SVL approaches based on minimum leakage power. The simulation results show that the adapted SVL approaches provide a higher quality D-type CMOS Flip Flop. The low-power communication systems use this D-type CMOS Flip Flop design.

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