Design and Performance Analysis of Low Power CRM USING CDF

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Abstract: - As a result of its ability to save energy, reversible logic has risen to prominence in recent years. Combinatorial circuits of various sorts, including a reversible de-multiplexer (RDM), reversible encoder (RE), reversible multiplexer (RM), and reversible decoder (RD) are implemented here. With the use of CMOS logic, the authors of this study provide novel 2:1 and 4:1 CMOS Based Reversible Multiplexer techniques to implementing the processor component and revised architecture. New 90 nm technology-based 2:1 and 4:1 CBRM are studied in this article. The software Cadence is used to do the simulations. However, designing low-power, energy-efficient Reversible MUX circuits employing COMS-based DG FINFET (CBDF) technology is a considerable difficulty. This research demonstrates the underlying logic structure and circuit working of the CMOS and CBDF devices used to construct a CMOS Reversible MUX circuit. CMOS Based Reversible Multiplexer/Exchanger (CBRM) is constructed at the transistor level using CMOS and CBDF. CBRM performance is analyzed and compared to that of CBDF simulations run using the cadence tool in 90nm technology. Better mobility and transistor scaling may be achieved with the use of CRM using CBDF approaches, which results in reduced leakage current and power.

Key Words: CMOS, CMOS Reversible MUX, DG FINFET, Leakage Power, Cadence.

1.Introduction

Efforts to reduce silicon area, increase hardware throughput, and decrease power consumption are driving changes in mobile operating systems [1-3]. The sub-threshold Swing (SS) and leakage current of multi-gate transistors, such as double-gate FinFETs, are both less than those of Standard CMOS [4]. For tasks like video processing, filtering, and the Fast Fourier Transform, adders play a large role in these complex arithmetic circuits [5–6], and their ability to utilize minimal power and energy has a substantial impact on how well any system is implemented in DSP-based processors performs. It is possible to minimize power usage by adjusting the supply voltage and operation frequency. However, waiting makes for safer driving and improved performance [7-9]. There have been a number of different designs for full adders throughout the years, and they all have their advantages and disadvantages. The full adder becomes the focal point of efficient structures like the carry choose, carry skip, carry look ahead, and

traditional adders [10, 11]. It is also crucial to extend and enhance the Full adder's functionality at very low voltages.

High-speed performance in computing and other areas of use, including the processing, calculation, and analysis of any signal, has led to the widespread adoption of digital CMOS circuits. Compared to other logic families, CMOS logic is favored because of its high performance, low static power consumption, and excellent logic levels and noise margins. Because we need to process signals more quickly, there is a strong demand for these circuits, and that need is only likely to grow in the near future. The greater the number of transistors on a chip, the quicker the computer can do calculations. Nevertheless, this gain in performance is accompanied with an increase in the amount of energy and power that are being dissipated [12]. Higher levels of energy and power dissipation have a number of drawbacks, the most significant of which is that they force circuits to need more costly packaging and expanding cooling equipment, which reduces their dependability and also drives up costs. Higher clock frequencies and on-chip integration are necessary to meet the need for quicker calculations, but the increased energy and power consumption of these high-performance circuits presents a significant design difficulty [13]. To reach Tera Instructions per Second (TIPS), high-end microprocessors need billions of transistors per board and clock speeds of more than 30 GHz. At this pace, the circuit is expected to use thousands of watts of electricity. The performance of circuits is negatively impacted when there is such a high density of power dissipation because it raises reliability problems such as hot carrier, thermal stress, and electromigration. More power from the battery will be required by larger power dissipation circuits to meet the increasing need for low-power processors or low-battery consumption chips [14-16]. For battery-operated digital devices like notebooks, laptops, tablets, and the like, having a low power consumption is of paramount importance since it results in longer battery life.

2.Literature Survey

A TSG gate-based NxN reversible multiplier was suggested by Himanshu Thapliyal and Srinivas [17]. Partial products are generated in parallel with a delay using a TSG gate in a reversible multiplier, and the sum is reduced to log2N steps. They have also used this reversible multiplier to develop a 4x4 architecture. To reach the total result, Nidhi Pokhriyal et al. [18] developed a Vedic 8x8 multiplier with compressors of 4: 3, 5: 3, 6: 3, and 7: 3. By merging the teachings of the Vedic sutras Urdhwa Triyakbhyam with modern compression techniques, a powerful but energy-efficient multiplier architecture has been developed. In 180 nm technology, the cadence tool was used for the synthesis and analysis. Maryam Ehsanpour and her colleagues [19] designed a reversible 4-bit binary multiplier circuit that makes use of a Modified Full Adder (MFA). They did this with the goal of minimizing the amount of complexity introduced by the hardware. Additionally, they demonstrated that the constructed reversible circuits are capable of functioning as a reversible full adder, with just a minimal number of garbage outputs and constant inputs required. This was accomplished by reversing the inputs and outputs of the adder. Arithmetic circuits were designed by Madhusmita Mahapatro et al. [20] using reversible logic gates as its building blocks. They were able to model and synthesise arithmetic circuits by using technology with a resolution of 0.25

micrometres. Adders, both complete and partial, may be built with reversibility in mind throughout the construction process. Combining the reversible full adders and half adders allowed for the development of a 4-bit binary parallel adder as well as a 4x4 multiplier circuit. A reversible multiplier circuit was developed by Anindita Banerjee and Anirban Pathak [21] by the use of the NCT gate (also known as NOT, CNOT, and Toffoli). All partial products are generated and then added using a binary tree network, which is the basis of this method. Circuits for producing reversible partial products and for performing parallel addition are developed. This design minimizes the system's quantum cost, gate count, and the amount of useless outputs. For single-precision floating-point multiplication, Jenath and Nagrajan [22] developed a reversible approach. Multipliers are created using Peres gates. The multiplier's operands are split into three 8-bit sub-operands. Nine 8x8-bit multipliers are used to produce a 24x24-bit reversible multiplier. The quantum cost, latency, and garbage outputs are all taken into account during the construction of an efficient multiplier. The Xilinx 9.1 simulation tool is used for simulation once the VHDL code has been written for the design. For signed multiplication, Kartikeya Bhardwaj and Bharat M. Despande [23] presented a Kalgorithm, an enhanced version of Booth's Recoding Algorithm. An efficient multiplier architecture is also suggested to be used in the implementation of this method. They built a 4-bit reversible multiplier, both fault-tolerant and non-fault-tolerant, using Booth's Recoding method. They have utilised this technique to investigate issues including quantum cost, constant inputs, gate count, and analysis of garbage data. When compared to standard approaches, this one reduces the quantum cost by 33%. Face recognition using LBP was the topic of a paper by Pradip Panchal et al. [24]. To create locally improved LBP, we first segment faces into smaller areas to extract features from. When all of the local histograms are added together, we get the GLBP picture. Face brightness and expression changes are used to evaluate the effectiveness of this method. They obtained an 80% recognition rate using this strategy. To recognise faces, Bilel Ameur et al. [25] presented a work. In order to extract features, Gabor wavelets, and LBP are used. The pattern vector is scaled down using the dimension reduction method.

3.Implementation and Operation of 2:1 CMOS-Based Reversible MUX Logic (CBRF)

An analogy that may help explain how a quantum computer works is that of a network (or collection of networks) of quantum logic gates, each of which executes a simple unitary operation on a qubit (or many qubits). A reversible logic gate is a non-destructive circuit or gate that may be used in either direction. When given two input vectors, a reversible logic circuit may produce two distinct output vectors.

When there is exactly the same number of inputs as there are outputs (n = k), we say that the logic gate in question is reversible. Since the input vector can be uniquely retrieved from the output vector, we declare the gate to be reversible when the logic of the input gate and the output gate are identical. You'll need a set of reversible logic gates to build a logical circuit that can operate in either direction. This is the terminology for a reversible logic gate with inputs of size n by k:

Input Vector

$$I_V = (I_{i,j}, I_{i+2,j}, I_{i+3,j} \ldots \ldots \ldots I_{k-1}, I_{k,j}) \tag{1.1}$$

Output Vector

$$O_V = (O_{i,j}, O_{i+2,j}, O_{i+3,j} \ldots \ldots \ldots O_{k-1,j}, O_{k,j}) \tag{1.2}$$

For each Particular Vector $I_V = O_V$

A reversible circuit is one that can be easily reversed by applying the same inputs to the same set of outputs. We can see this in Figure 1.
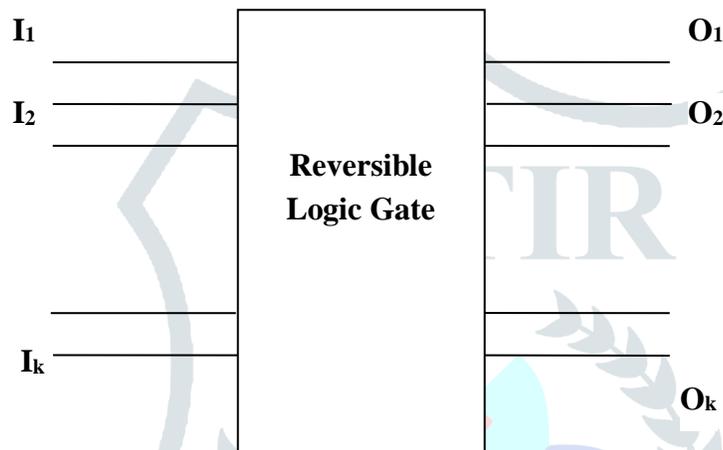

Figure 1.: A gate with K input and Output is called K*K gate

The reversible logic being as a more alternative and traditional approach for irreversible logic gate circuits. Since reversible logic computing does not erase or lose information or data in the logical operation.

One of the simplest reversible logic gates is the NOT gate, sometimes known as a 1x1 gate. A typical 2x2 gate is the controlled-NOT (CNOT) gate. On a 3x3 grid, some of the reversible logic gates that may be used are the TR, FG, PG, and TG gates. Reversible gates with a ratio of 1:1 have zero quantum cost, but those with a ratio of 2:2 have one. To get the most performance out of any reversible gate, all you need are 11 NOT gates (inverters) and 22 Feynman gates. FG gate, also known as CNOT gate, and reversible gates like V and V+ are all examples of such gates. V and V+ Quantum Gates have characteristics defined by the following equation.

$$V \times V = \text{NOT} \tag{1.3}$$

$$V \times V^+ = V^+ \times V = I \tag{1.4}$$

$$V^+ \times V^+ = \text{NOT} \tag{1.5}$$

Counting the number of V gates, V+ gates, and CNOT gates is one technique to determine the quantum cost of a reversible gate. In addition to the NOT gate, figure 1.2 also shows the Controlled NOT gate.
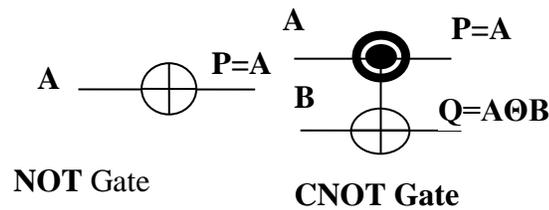
Figure 2: 1x1 NOT Gate and NOR Flip-Flop (CNOT) Combinational Circuit

(I) Garbage Input/output- Garbage output is a key characteristic of a reverse gate. Garbage input is an input to a gate that isn't utilised as input to another gate or as the principal output of the gate. This includes any and all inputs. The term "garbage" refers to the outputs of a gate that are not used in any way. Every single load of waste results in a significant financial penalty being incurred. In the context of computing using reversible logic, if we wish to find the exclusive or relationship between two variables, then this circuit will look like the one shown in Figure 3. It is necessary for this operation to generate one additional output in order for the logic circuit to be reversible; this undesirable output, denoted by the notation "P = A," is sometimes referred to as garbage.
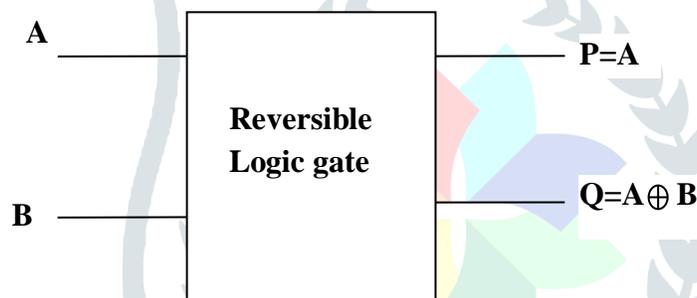

Figure 3: A Garbage input/output reversible logic gate.

(ii) Quantum Cost- The input side of the circuit's constants, which are either zeroed out or set to one. The "Gate Count" indicates how many non-destructive logic gates are needed to do the task. A common measure of computational hardware complexity is the number of "elementary logic gates" (NOT, AND, and EXOR gates) required to perform the desired set of operations.

(iii) Critical Path- The Delay may be determined using the critical route and reversible logic. The most indirect route achieves the intended result.

(iv) Gate Count- The sole function realised by a reversible circuit is the reversible one.

(v) Transistor Count- The sum of the transistors used in logic gates and the transistors needed to create a reversible gate.

Many types of reversible gates have been described in published works. Feynman Gate (FG) is the most prevalent, followed by Fredkin Gate (FRG), Peres Gate (PG), Toffoli Gate (TG), and Khan Gate (NG). There is currently no published quantum implementation of all of these gates. So far, nanotechnology has only been able to produce PG, FG, TG, and FRG.
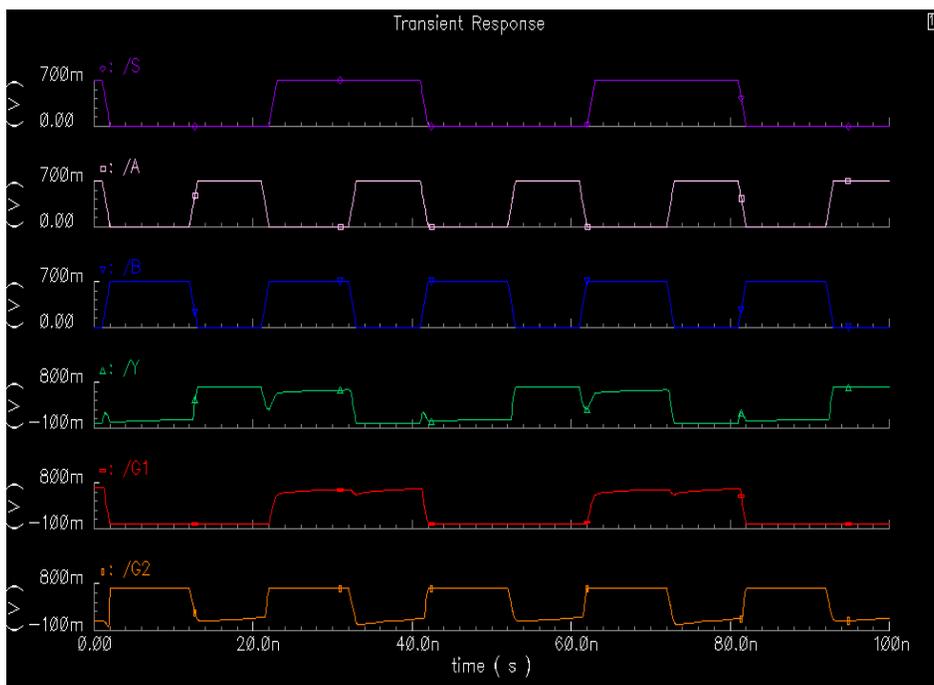
4. Proposed CMOS Based Reversible Multiplexer (CBRM)

The proposed design of CBRM design required the smaller number of transistors and the design implementation of the complex design of large logic gate circuitry. This is the most fundamental approach for every design of logic gate is the using pass transistor logic gate concept.

The proposed 2:1 CBRM is realized using CMOS (i.e. PMOS and NMOS). 2:1 CBRM producing two garbage bits i.e. G1 and G2. Specify S, A, and B as the inputs. The message bits are selected by the input S and sent on to the output Y. The proposed 2:1 CBRM's schematic is shown in Fig. 4, and the proposed 2:1 CBRM's transient response is depicted in Fig. 5.

Fig:4 Schematic of Proposed 2:1 CBRM

Fig: 5 Transient Response of proposed 2:1 CBRM

CMOS (including PMOS and NMOS) is used to implement the planned 2:1 CBRM. Two trash bits (G1 and G2) are generated by a 2:1 reversible MUX. These are the inputs: S, A, and B. The message bits are sent to the output Y based on the selection input S. DC A ratio of 2 to 1 Figure 6 depicts the reversible MUX, while Figure 7 displays the waveform of the leakage current.
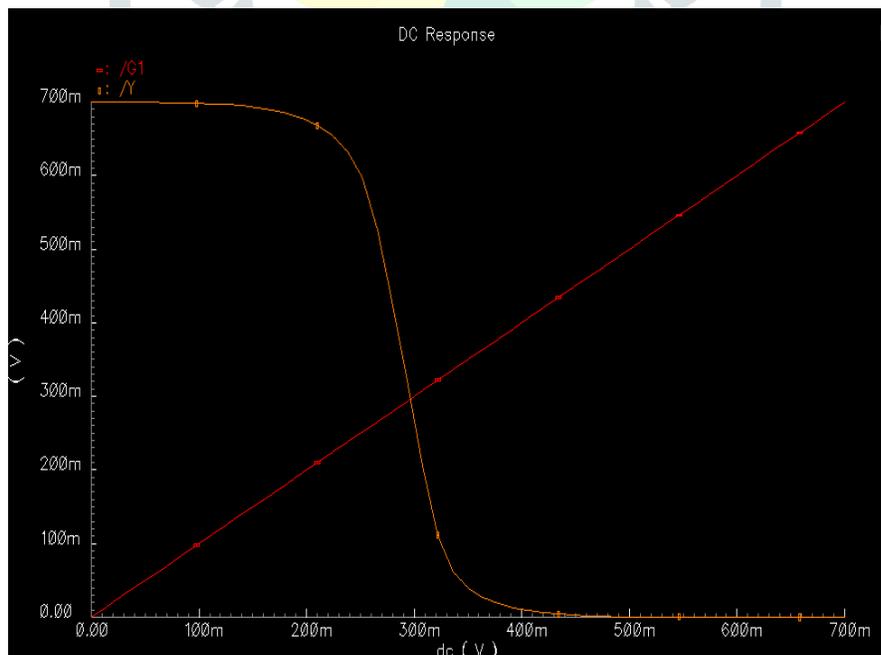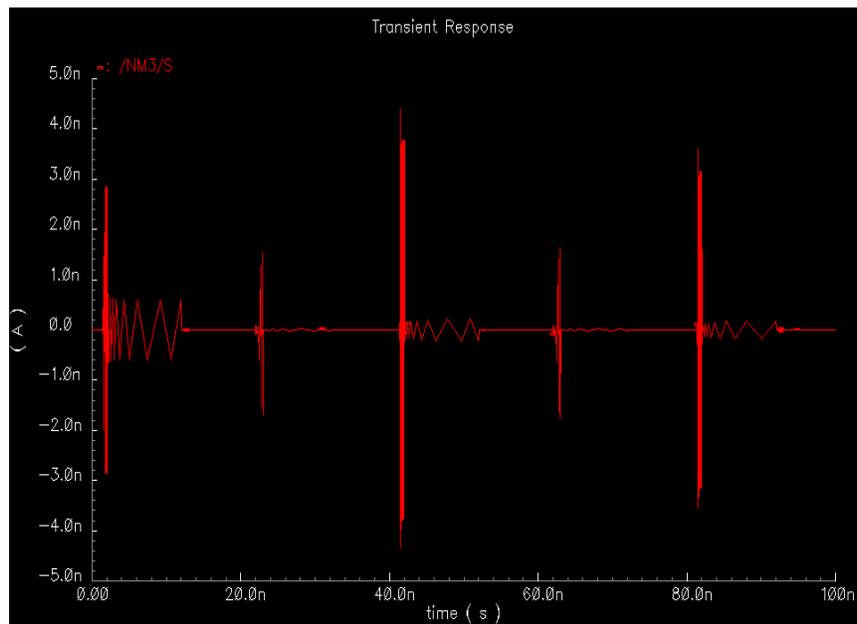

Fig: 6 DC Response of proposed 2:1 CBRM

Fig: 7 LC Waveform of proposed 2:1 CBRM

5.CBRM Using CMOS-Based DG FINFET (CBDF) Technique

Connected on a CMOS-based reversible multiplexer (CBRM) is a COMS-based DG FINFET (CBDF) system. Here, the CDF's front and back gate's autonomous decision-making controls may be put to good use in order to generate execution and reduce control utilisation. Parallel transistors may be combined in non-obvious ways using self-deciding entrance control. Connecting the source and drain terminals of two transistors in parallel creates a parallel transistor match. To reduce short-channel effects and spilling current, a second gate is placed in the opposite direction of the conventional gateway in CBDF, which has been expected. Short gate (SG) mode involves connecting the gates of two transistors; independent gate (IG) mode uses two independent digital signals to drive the gates; low power and ideal power mode involves connecting the back gate to a fixed voltage to better regulate spillage; and crossover method mode combines the low power and self-deciding gate modes. Constant efforts to shrink bulk CMOS have revealed basic material problems. Significant challenges arise when attempting to shrink mass CMOS to 45 nm gate lengths, including short channel effects, optimum current, gate dielectric leakage, and device-to-device variation. However, CBDF-based designs allow for better management of short-channel effects, lower leakage, and increased yield in 45nm processes. This improves the ability of CBDF-based designs to conquer scale issues. Figure 8 depicts the CBDF coupled to the CRM schematic. Figure 9 displays the waveform of CRM's output when the CBDF technique is used.
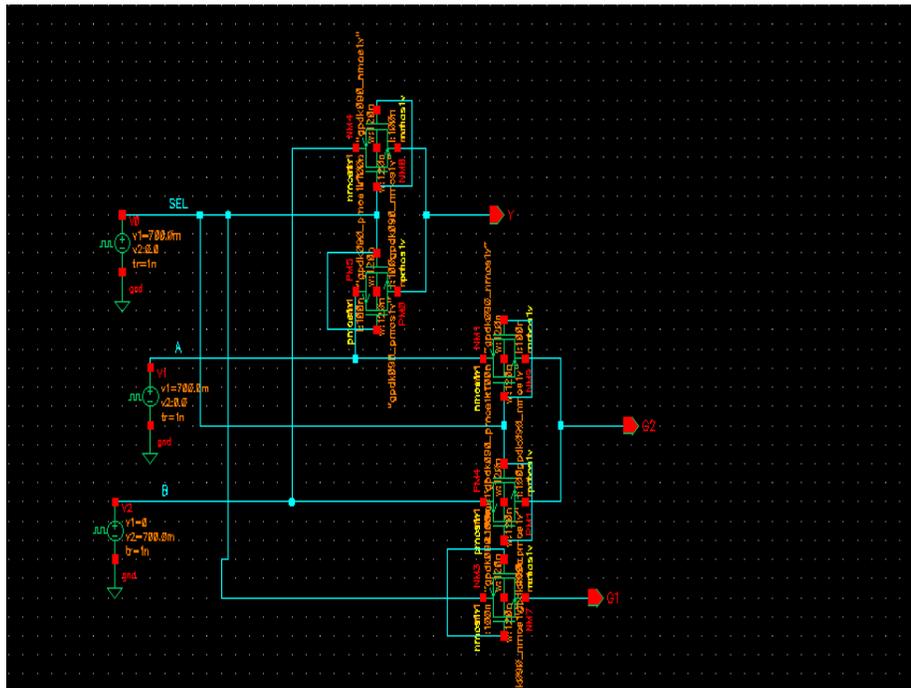
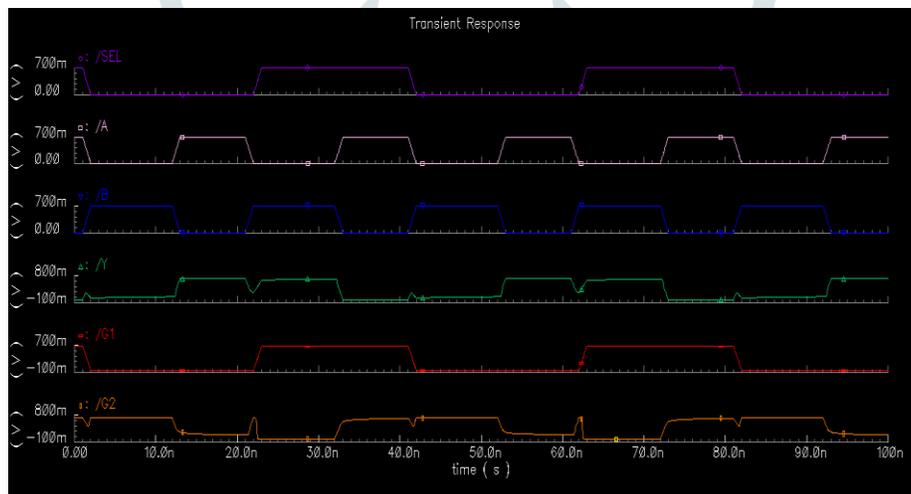Fig:8 Schematic of Proposed CBRM using CBDF
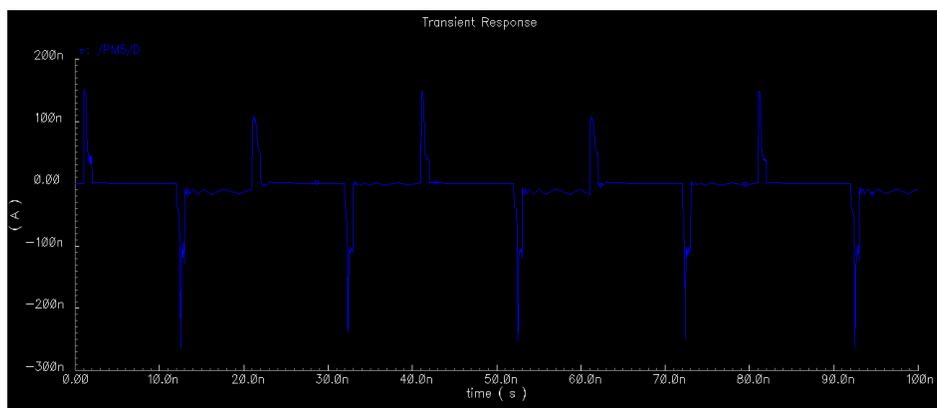

Fig:9 Output waveform of Proposed CBRM using CBDF

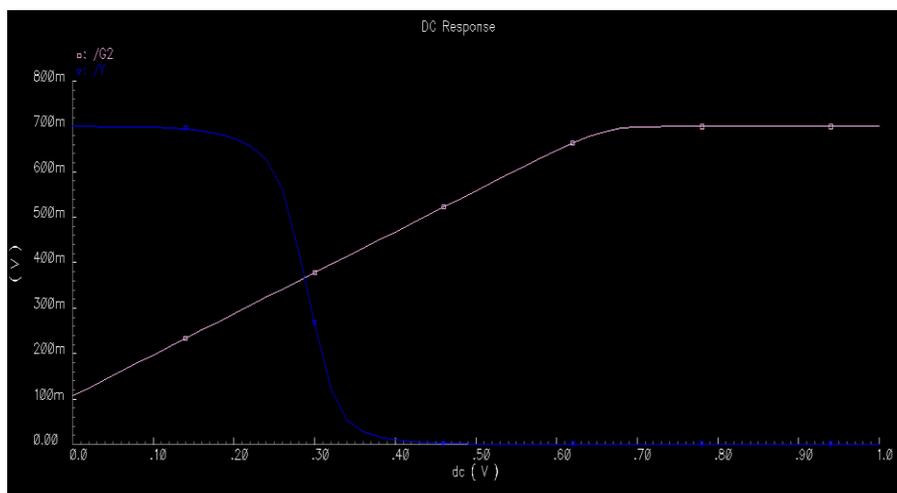Fig:10 LC waveform of Proposed CBRM using CBDF

Fig:11 DC Response of Proposed CBRM using CBDF

4:1 CBRM

The suggested reversible gate enables the construction of 4:1 CBRM, as seen in Figure 4. There are three gates necessary for this design, and the result is six useless outputs. The truth table of 4:1 CBRM is illustrated in Table II; in this scheme, the non-essential trash outputs are simply thrown away.
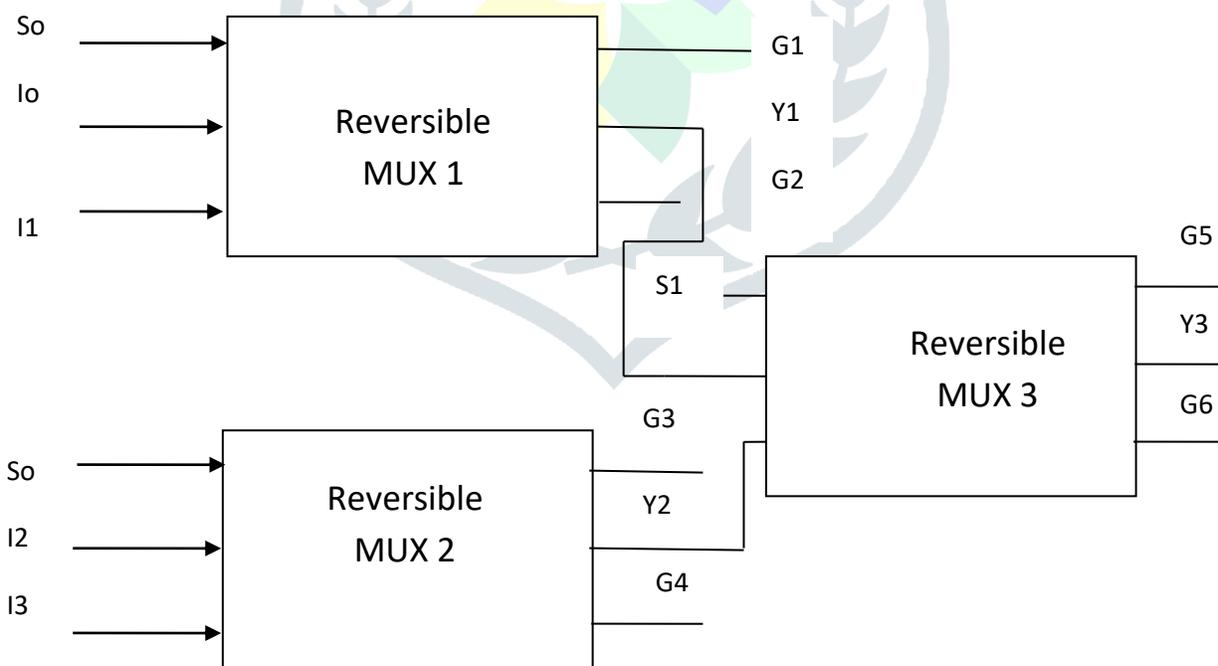

Fig.12 Block Diagram of 4:1 CBRM

Table II Truth Table of 4:1 CBRM

Select Inputs		Output
S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

According to the truth table above, 4:1 CBRM retains all of its pre-existing functionality relative to that of an irreversible multiplexer. For the final result "Y," the corresponding equation is as follows:

$$Y = \overline{S_1}\,\overline{S_0}\,I_0 + \overline{S_1}S_0I_1 + S_1\,\overline{S_0}\,I_2 + S_0S_1I_3$$

Proposed 4:1 CBRM

The CMOS technology, including PMOS and NMOS, is used to implement the planned 4:1 CBRM. The 4:1 CBRM algorithm generated six garbage bits, which are denoted by the letters G1, G2, G3, G4, G5, and G6. The following are considered to be inputs: So and S1, I0, I1, I2, and I3. The message bits that correspond to the selected option are sent to the outputs Y1, Y2, and Y3 in accordance with the selection input S. The schematic of the proposed 2:1 CBRM can be seen in Figure 12, and the transient response of the proposed 4:1 CBRM can be seen in Figure 13.
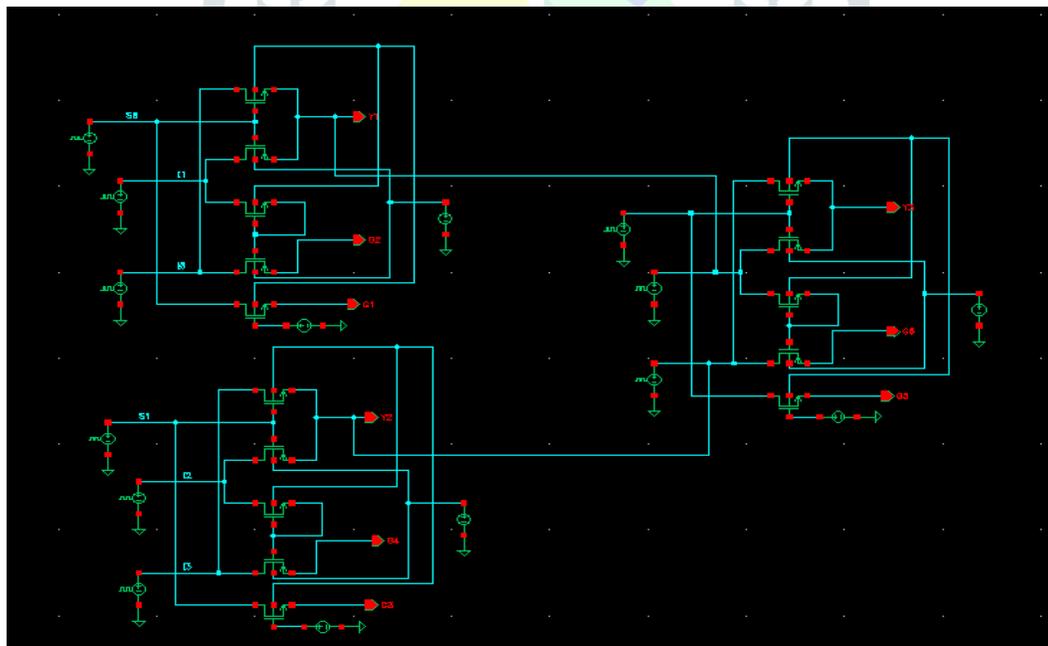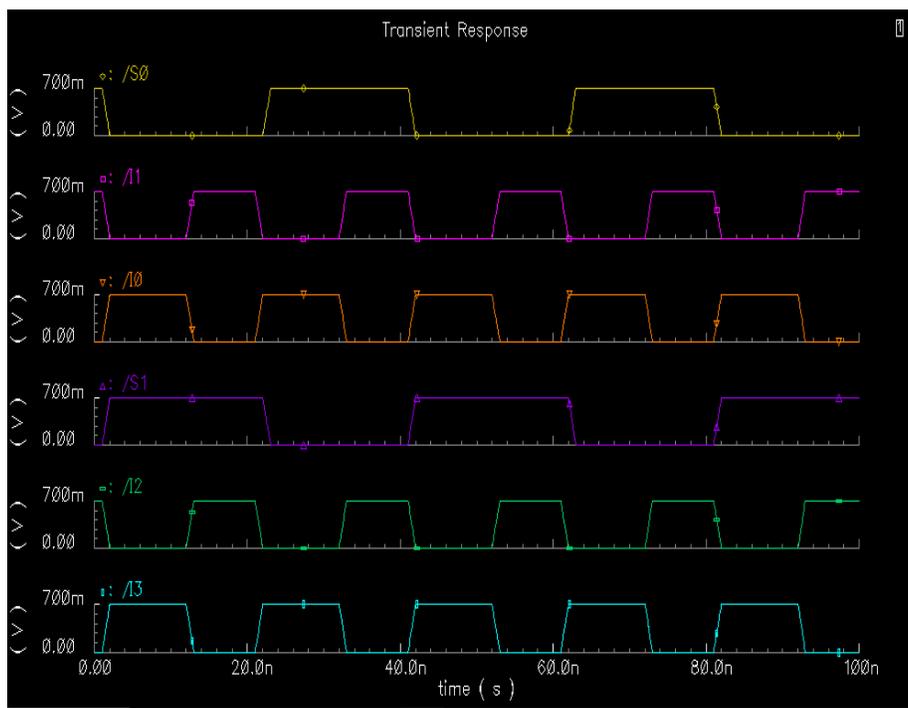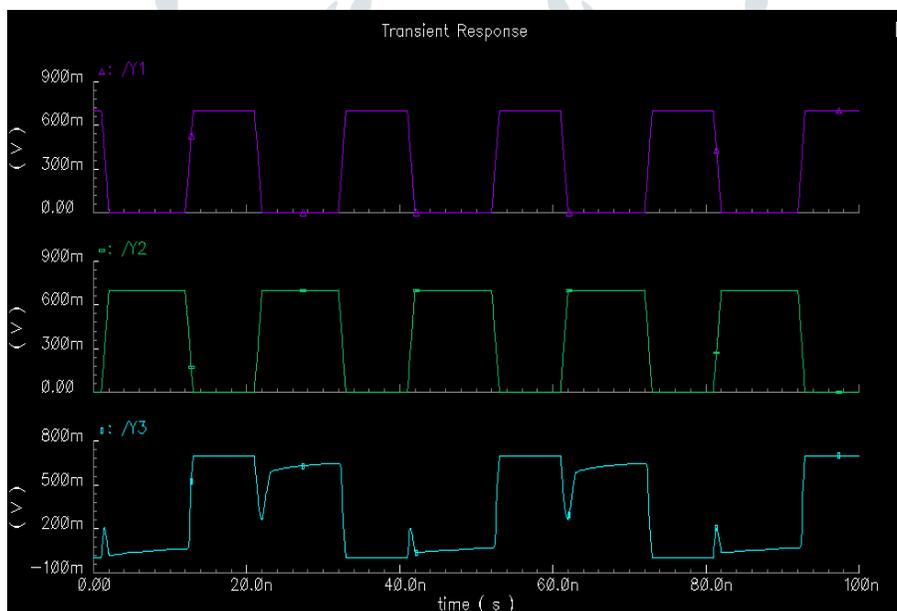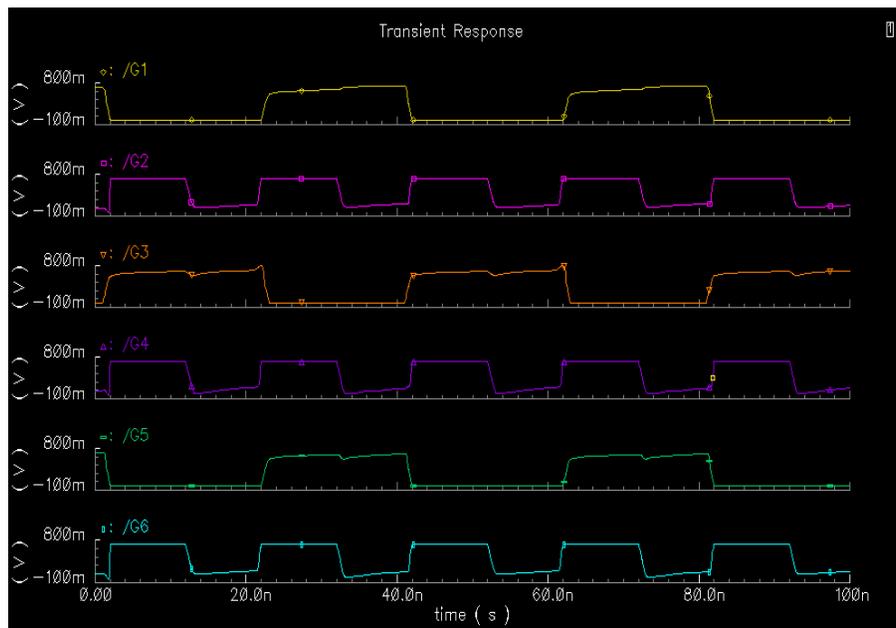

Fig.12 Schematic of Proposed 4:1 CBRM

(a)

(b)

(c)

Fig.13 Transient Response of 4:1 CBRM

6.Simulation Result

2:1 and 4:1 The simulation of a CBRM circuit was carried out using the cadence tool using a technology of 90 nm and a notional supply voltage of Vdd equal to 0.7 V. Simulations of CBRM has been performed with the help of the cadence tool. The nominal supply voltage used was Vdd = 0.7 V, and the technology used was 90 nm. At 27 degrees Celsius, the gate leakage is the sole dominating mechanism, thus many methods have been employed to decrease power consumption while keeping the performance of the CBRM circuit unchanged via the CBDF methodology. Table.1 displays the results of a comparison of CBRM circuits using the CBDF approach, including measurements of leakage current and leakage power.

Table 1 summarizes the findings from a comparative analysis of the 2:1 and 4:1 CBRM circuits, with the 2:1 CBRM circuit using the CBDF method.

Table 1 Conclusions Based on Simulations

Performance Parameter	2:1 CMOS-Based Reversible MUX (CBRM)	CBRM Circuit using CBDF technique	4:1 CMOS-Based Reversible MUX (CBRM)
Technology Used	90nm	90nm	90nm
Supply Voltage	0.7V	0.7V	0.7V
Leakage Power	3.17nW	1.3nW	8.14nW
Leakage Current	4.53nA	1.1nA	7.23nA
Delay	2.11ns	1.2ns	4.21ns

Table 2 Comparison shows previous work

Performance Parameter	Previous work [26]	Proposed work
Supply Voltage	1.14 v	0.7v
Power	11.264 μW	3.17nW
Current	0.987mA	4.53nA
Delay	4.894ns	2.11ns

7.Conclusion

Compared to the suggested reversible MEDD gate, conventional systems often use more constant inputs, garbage outputs, and reversible logic gates. This is done in an effort to reduce the amount of power that is used by the device. It can function as a 2:4 decoder, 4:2 encoder, and 1:2 de-multiplexer. The research evaluates the new 90 nm 2:1 and 4:1 CBRM. Cadence is used to produce the simulation results. When working with COMS-based DG FINFET (CBDF) technology, it might be difficult to develop reversible MUX circuits that are both low-power and energy-efficient. This article describes the logic structure and operation of the underlying circuit that is used to produce a CMOS Reversible MUX utilizing CMOS and CBDF devices. A CMOS Based Reversible MUX (CBRM) is built using CMOS and CBDF at the transistor level. CBRM gate power dissipation is measured to be 3.17nW at 90nm CMOS technology. It has been determined that CBDF consumes 1.3nW less power than CBRM. The improved performance of computers is a direct result of this design, which serves as a tipping point for the construction of increasingly complicated arithmetic systems based on these reversible logic gates.

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