JETIR.ORG ISSN: 2349-5162 | ESTD Year : 2014 | Monthly Issue
JOURNAL OF EMERGING TECHNOLOGIES AND INNOVATIVE RESEARCH (JETIR)
An International Scholarly Open Access, Peer-reviewed, Refereed Journal

HDL PLATFORM A GAME CHANGER FOR REAL TIME PROCESSING AND POWER OPTIMIZED EMBEDDED SYSTEMS

[1]Umashankar C P, [2]Shashikala T G

[1]Engineer,Vedhya Technologies Pvt Ltd, Rajajinagar, Bangalore, India

[2]Assistant Professor, Department of Physics,

Government First Grade College, Vijayanagar, Bangalore, India

Abstract : Embedded Systems plays an vital role as it is considered as the element of digital world which is used in many areas like appliances, transportation, computing, health care, military technology, etc. The most integral part of Embedded Systems is micro-controller which is made out of semiconductor.

The micro-controller is a sequential in nature at a given point of time which will be executing a single instruction to enhance the performance, the software-based scheduler is used to perform multiprocessing of task. The scheduler is utilized in most popular RTOS (Real Time Operating System) for micro-controller like FREERTOS/uKernel/Linux and other commercial RTOS like VxWorks/Integrity. As embedded system evolved over the period, OEM started rolling out multi-core concept to offload the different task to a particular core to enhance the parallel execution, which reduce the latency for speed optimization, but the power consumption substantially increased.This paper briefs how to address the existing challenges like power optimized and real time processing using FPGA and HDL as programming language over a traditional micro-controllers and C/C++ programming Language.

Keywords: Hardware descriptive language,Field programmable gate arrays, Real Time Operating System,VHDL,Verilog, Hardware Scheduling

I. INTRODUCTION

FPGA based HDL platform has been introduced to primarily expose the engineers to the power of the FPGA which is gaining importance and implementation in many complex and highly technical critical applications across industries as compared to micro-controller. At present, micro-controller such as CortexM4, RISCV5 is fulfilling the most of the embedded application using embedded programming languages like C/C++. FPGA uses HDL (VHDL/Verilog) as a programming language. The major key parametric difference between C/C++ and HDL are listed in table.1 which is shown below.

Parameters	Embedded C / C++	HDL
Language	System level language	Hardware descriptive language
Processing	Sequential	Sequential and Concurrent
Latency	In milliseconds	In microseconds
Resources	More Memory required (MB)	Memory is fixed with FPGA selection in few KB
Targeted Applications	Soft Real time	Hard real time
Scheduling	Software based	Hardware based

Table.1Comparison between C/C++ and HDL

As per the independent research done by SIEMENS, most of the popular upcoming programming languages adapted for using popularly increasing HDL language are gaining more popularity as compared to C/C++ or any other design language.

Based on the analysis (as shown in fig.1) with respect to popularity and adaption, HDL is going to gain a momentum to address the upcoming industry challenges in various verticals like AI-ML, Big-DATA etc.

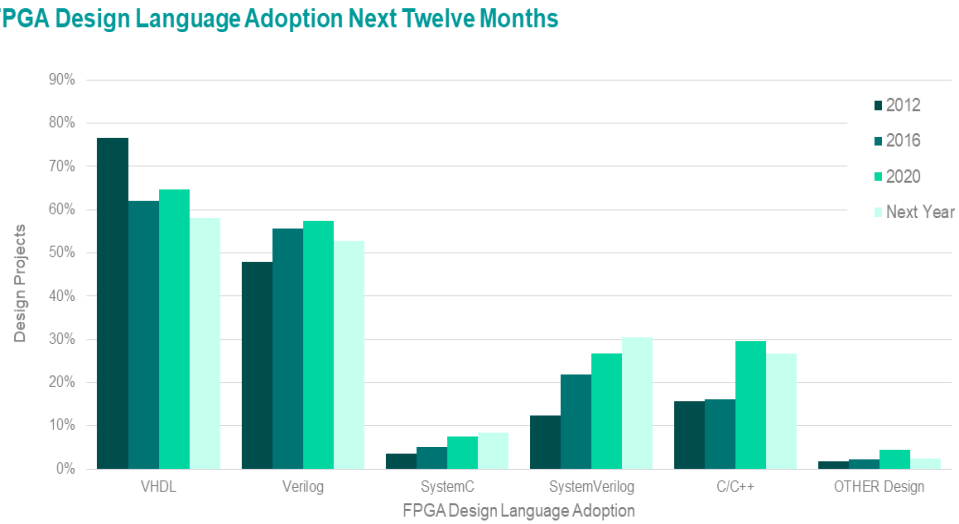

Fig.1 FPGA Design Language Adoption

HDL is the language which helps to design any simple or complex digital design instead of using gate level design which will be more tedious and complex. At present most economically viable FPGA are available from Original Equipment Manufacture (OEM) like LATTICE, ACTEL, GOWIN, EFFINIX starting 1K to 9K LUT. This FPGA resource is self-sufficient which can be tightly coupled with SDRAM/DDR to address the IoT, primitive AI-ML applications. HDL by default support parallel processing(concurrent), developing a hardware-based scheduling (as shown in fig.2) compared to software-based scheduling used by RTOS will have no overhead.

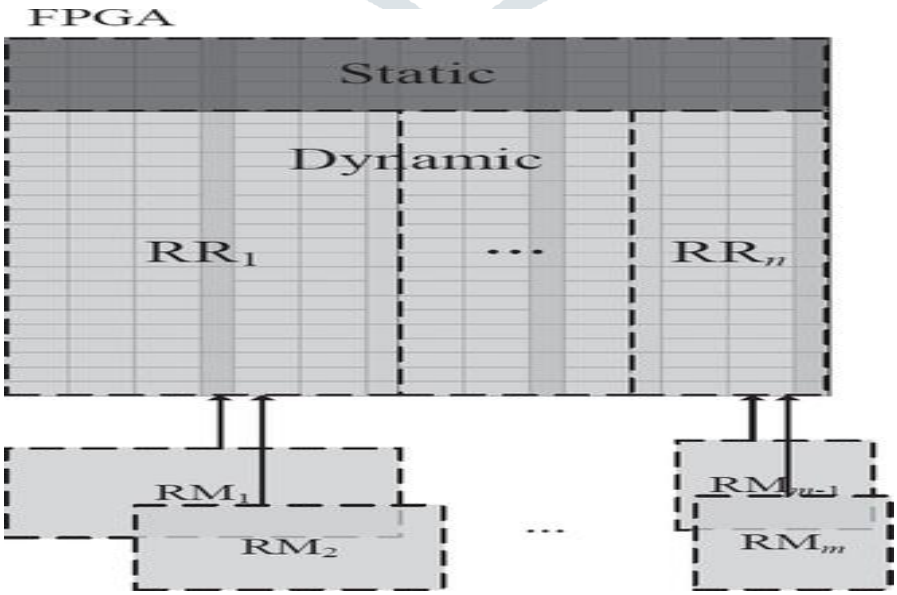

Fig. 2 Typical Hardware based Scheduling

2.CONCLUSION

In recent years with the widespread popularity and availability of FPGAs by various upcoming OEM vendors like Gowin, Effinix, Renesas etc. are having most viable and economical variant of FPGA resources which is helping in addressing various challenges faced in the embedded fields such as IoT, Artificial intelligence, Data centers, and Cloud computing to especially optimized the power and performance. The hardware based scheduling within the FPGA-based hardware will significantly helps to avoid the usage of RTOS to process multi tasking features. The above mentioned trends will shorten the learning curve for any enthusiastic engineer to take up HDL as programming language and contribute towards the industry and also equally enable to get the innovative products to address the present challenges as addressed in this paper.

3.REFERENCES

[1] https://community.element14.com/technologies/fpga-group/w/documents/5003/how-to-boost-compute-performance-with-fpga-based accelerators#:~:text=FPGA%20accelerators%20need%20a%20server%20to%20function%20and,giving%20a%20boost%20to%20the%20CPU%20server%20engine.

[2] https://ietresearch.onlinelibrary.wiley.com/doi/full/10.1049/cje.2021.07.021.

[3] https://i0.wp.com/semiengineering.com/wp-content/uploads/Siemens_WRG-verification-study-2020-pt2-Figure-7.-Trends-in-languages-for-FPGA.png?ssl=1

[4] https://semiengineering.com/trends-in-fpga-verification-effort-and-technology-adoption/