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A COMPARATIVE STUDY OF DUAL GATE MOSFET CONCEPT

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ABSTRACT

Recently, integrated circuits have relied heavily on the Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET). There have been several reports of MOSFET architectures with a channel length of 0.1 pm or less in the business literature due to the rapid development of this technology. In this study, a source follower based on a dual-gate MOSFET is designed [1]. The theoretical foundations of the key themes at play in this work have been examined. Mathematical analysis of circuit layout from first principles has been completed. The goal is to make the source follower in RF applications more reliable and easier to use. Short Channel Effects (SCEs) and other issues plague the standard Double Gate (DG) MOSFET. In this work, a Core Insulator Double Gate (CIDG) MOSFET with a specially constructed channel is presented for use in low-power digital circuits. The channel of the proposed device is insulated by a thin layer of material. Using a rectangular core insulator helps the device's performance characteristics by lowering the leakage current significantly. After verifying the simulation findings against the DG MOSFET reference data, a structural analysis is performed [2]. In this paper, we examine the advantages and disadvantages of both the double-gate and single-gate MOSFET configurations, with respect to a variety of performance parameters and channel material configurations, and we evaluate and compare a variety of channel materials, as well as the orientation of its structure and potential future applications.

Keywords: Architectures, Structural, Orientation, Performance, Insulator, Semiconductor

INTRODUCTION

The Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is an extremely popular semiconductor that serves as a valuable power device in both digital and analogue circuits. With its status as the first miniaturized transistor, it can be used in many other kinds of electronics. Because to its small size, the MOSFET is a crucial part of the integrated circuit and may be developed and produced on a single chip. It has four connectors labeled Source (S), Gate (G), Drain (D), and Body (B) respectively. In order for the MOSFET to operate as a field-effect transistor, the body is normally linked to the source terminal. A Field-Effect Transistor (FET) known as a Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET, MOS-FET, or MOS FET) is often made by oxidizing silicon in a regulated manner. The device's conductivity is controlled by the voltage applied to its insulated gate. Its voltage-dependent conductivity property has applications in electrical amplification and signal switching. Similar to a MOSFET is the Metal-Insulator-Semiconductor Field-Effect Transistor (MISFET). Insulated-gate field-effect transistor is another name for this device. Several technical advances in the 21st century is said to have been made possible by the MOSFET. Its low current consumption makes it superior to the BJT for controlling loads. By switching the MOSFET to enhancement mode, the conductivity may be raised from its "usually off" condition. Conductance in the "usually on" state may be reduced by applying a voltage via the gate. MOSFETs can be easily miniaturized by a straightforward procedure, making them suitable for use in small devices. The metal-oxide semiconductor field-effect transistor (MOSFET) has a number of benefits that make it well-suited for large-scale integration. They include fast switching (especially in regard to digital data), low power consumption, and high density.

The metal-oxide semiconductor field-effect transistor (MOSFET) has become pivotal in integrated circuits in recent years. Silicon metal-oxide-semiconductor field-effect transistor (MOSFET) based VLSI circuits have consistently increased performance and also decreased costs for semiconductor chips for information handling

and memory activities due to innovative advancements and the high adaptability of the device structure. Recent research has concentrated on MOSFETs with channel widths of 0.1 pm or less; faster speed and thickness and reduced power requirements for putting a whole framework on a chip are motivations for further scaling. Many 0.1 pm MOSFET device designs have been documented in the literature. Since every device structure has pros and cons, it's important to compare and contrast the main offered gadget designs side by side using the same arrangement of imperatives. Yet, it is difficult to perform a thorough device comparison because of the multiple trade-offs between the characteristics of MOSFETs.

LITERATURE REVIEW

Kosmani, N.F. & Hamid, F.K.A. & Razali, M.A. (2019) As CMOS continues to shrink in size, the planar MOSFET's structure will soon hit a wall as short channel effects (SCEs) become the primary issue with further shrinking. If CMOS scaling is to be achieved, it is believed that Double-Gate and Gate-all-Around nanowire MOSFETs will need to replace planar MOSFETs. This work so reports the outcome of device simulation for Double-Gate and Gate-All-Around nanowire MOSFETs conducted using Silvaco TCAD tools. The goal of this simulation work is to examine the impact of physical parameters on the electrical behavior of both the GAA nanowire and the DG MOSFET. Gate-All-Around nanowire simulation results are compared to existing literature. The subthreshold slope of DG was observed to increase from 62mV/dec to 162.7mV/dec when the gate length was scaled from 80nm to 10nm. Instead, GAA has a subthreshold slope that is rising from 65.8mV/dec to 127mV/dec. At Lg=80nm, DG has a threshold voltage of 0.40646V while GAA's is -0.17505V. Heavy doping worked well to dampen SCE; however, a lower doping concentration is preferable because to the larger on-state currents seen in the DG and GAA nanowires ($1.42x10^{-3}$ A and 3.2310^{-4} A, respectively). It was also shown that when channel doping is varied from low to high concentrations, the threshold voltage of DG and GAA nanowires both increased, from -0.0734V to 0.2312V and -0.0319V to 0.2232V, respectively.

Wagaj, Santosh & Chavan, Yashwant (2017) This study proposes a dual-material-gate silicon-on-insulator junctionless transistor (DMG SOI JLT). The EDA tools used for simulation are utilized to show off its features and compare them to those of a single-material-gate Silicon-on-insulator junctionless transistor (SMG SOI JLT). The data demonstrates that the DMG-SOI JLT can drive more current than a conventional single-Material-Gate-SiO2 JNT. DMG SOI JLT's potential distribution has a sharp jump at the boundary between two gates, which boosts the electric field in the channel. DMG SOI JLT has a shorter channel length than SMG SOI JLT, less DIBL, and less sub threshold slope fluctuation. At a channel length of 20 nm, transconductance of SMG SOI JLT is measured to be 0.25 mS.

Chakrabarti, Himeli & Maity, Reshmi & Maity, Niladri (2019) In order to better understand the surface potential profile of a totally depleted DMDG metal-oxide-semiconductor-field-effect-transistor (MOSFET), this research offers a two-dimensional (2D) investigative model. Many oxide thicknesses, doping concentrations, and gate voltages have been analyzed. It has also been observed that the suggested surface potential model is affected by the temperature and the interface charge density. For this study, we additionally factor in the various channel length ratios. We have accounted for the impact of high dielectric constant materials like HfO2 in our model and conducted a comparative investigation of the impact of various parameters. The surface potential along the channel in DMDG structure exhibits a step function, as predicted, which dampens a variety of short channel effects (SCEs). The model predicts that HfO2 will need a thicker oxide layer than SiO2 to achieve the same surface potential. The conclusions of the analytical model have been validated by simulations using technology computer-aided design (TCAD). They all seem to be very in sync with one another.

Das, T. & Pradhan, R. & Singh, Debabrata & Rath, Adyasha & Pattnaik, S. (2017) When silicon CMOS technology enters the sub-20nm realm, manufacturing constraints fundamentally restrict the ability to further shrink transistor sizes. In order to miniaturize transistors and boost their performances, advances in device architectures and materials are needed quickly. Unwanted effects such as drain induced barrier lowering (DIBL), gate leakage current, short channel effects, etc., are beginning to appear when device dimensions near their scaling limit. When the gate material work function is carefully controlled, a Tri-Material Double Gate (DMDG) construction may be used to simultaneously reduce SCE and increase device performance. Our research focuses on hot carrier effect, sub threshold swing, impact ionization, ion scattering, potential distributions, and short channel effects (SCE). TMDG MOSFET outperforms DMDG and SMDG MOSFET

in terms of surface potential, electric field, carrier mobility, and electron velocity, allowing it to mitigate scaling effects like DIBL, HCEs, etc., according to a study of the devices' electrical properties.

De, Arpan & Karmakar, Ananya & Ghosh, Rittik & Saha, Priyanka (2022) In order to detect hydrogen (H2) gas molecules, the authors of this study have attempted to create a simulation model for a MOSFET with a gate made of molybdenum disulfide (MoS2), called a MoS2 DG-MOSFET. Here, the NEGF approach is included into SILVACO ATLAS to evaluate the simulation model of the suggested gas sensor. Studying the change in threshold voltage vs the change in metal (gate) work-function with gas exposure has also been used to assess the device's performance. The findings show that a metal work function variation of 200 meV causes the greatest change in the threshold voltage (exactly 232 mV). Changes in the density of states, transmission probability, etc., due to the presence of H2 gas molecules are also shown in the research. The suggested device solves problems inherent in using traditional Si-based MOSFETs for gas sensing, accounts for a sensor's scalability, and enhances the OFF-state leakage current while maintaining a high ION/IOFF ratio.

RESEARCH METHODOLOGY

We have developed a double-gate MOSFET for use as an RF CMOS switch, specifically a double-pole four-throw (DP4T) switch, in wireless communication systems, and compared its performance characteristics to those of the single-gate MOSFET. Short Channel Effects have various restrictions that we've run across (Drain Driven Barrier Lowering, Subthreshold Leakage Current) (SCE). Figure 1 depicts a novel layout of double gate MOSFETs that was developed to address these issues. Here, the gate oxide separates the two gates on different sides so that they may function independently. This guarantees gate control over the channel and gate coupling and yields improved drain current.

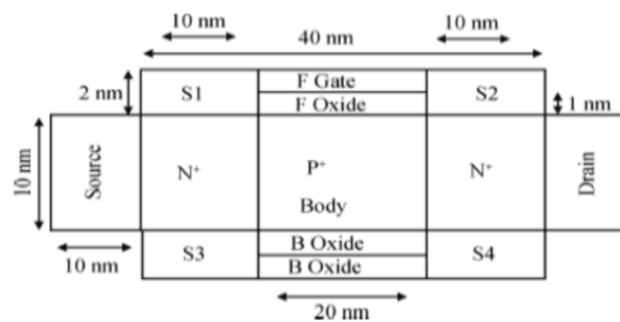


Figure 1: Structure of Double-Gate MOSFET

Layout and characteristics of single- and double-gate MOSFETs

Two symmetric gate voltages, DG and SG, are shown in the configuration of an n-MOSFET in Fig. 2(a) and (b), with the output going via V_{out}. Microwind 3.0 was used to create this layout. The standard meanings of the colors are applied here. With a MOSFET width of 600 nm and a length of 120 nm, the design is optimized for high speed. The poly, drain, and source are all present in these layouts. Due to the metal connection with the output voltage, the resistances are also provided in this configuration. Capacitances of 0.19 fF, 90Ω, 2 µm, 0.13 fF for metal, 0.06 fF for diffusion, and 0.86 fF for the gate are all present in this device's drain and source. Double-gate MOSFETs have a thickness of 3 µm and a resistance of 68Ω, whereas single-gate MOSFETs are 32Ω thick and 2 mm wide. For this study, we applied a gate voltage of 1.2 V at a low level and measured the start time, rise time, fall time, and pulse time for this signal at 0.475, 0.025, 0.025, and 0.475 ns for DG MOSFETs and 0.600, 0.025, 0.025, and 0.475 ns for SG MOSFETs. If a DG MOSFET is assumed to have a symmetric gate, then the structure and voltage supplied to both gates will be identical.

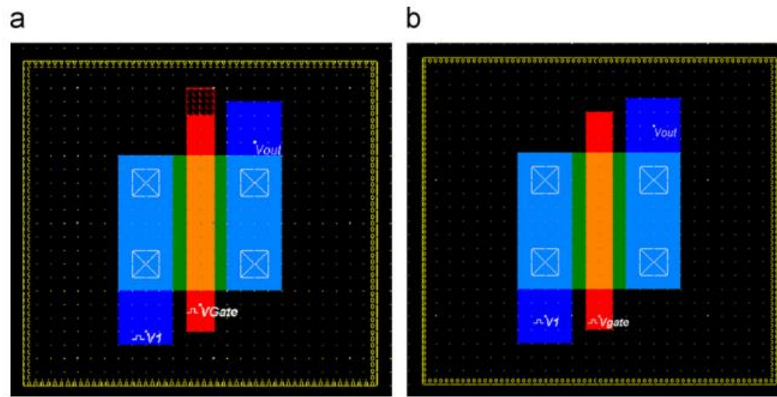


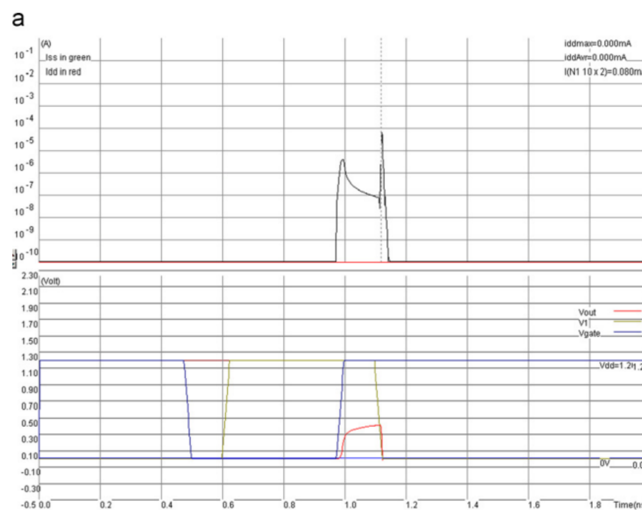
Figure 2: Layout of (a) the DG MOSFET and (b) SG MOSFET

C-V measurements are often used in thin-oxide MOSFETs to determine the drain current. However, due to the slightly thick oxides in this DG MOSFET device (resulting in a very small capacitance), the standard charge equation Q = Cox(Vgs-Vth) will be applicable, providing direct and accurate values for the density of charge carriers; this holds true even in the presence of double activated gates, where the linear relationship is strictly adhered to. The following equation may be used to determine the drain current given the charge Q:

$$I_{ds} = \mu Q V_{ds} \frac{W}{L} \quad (1)$$

Where μ, Vds, W, and L represent the mobility of the channel, the drain-to-source voltage applied, the channel length, and the channel width, respectively.

The drain current is greater in DG MOSFETs than in SG MOSFETs because charge Q is larger in the former due to larger capacitance values (as will be shown in the next part of this article). The currents drawn on the log scale for 1.0-1.1 ns are 80 μA for the DG MOSFET and become stable at 0.10 μA in Fig. 3(a), and 76 mA for the SG MOSFET in Fig. 3(b), respectively.



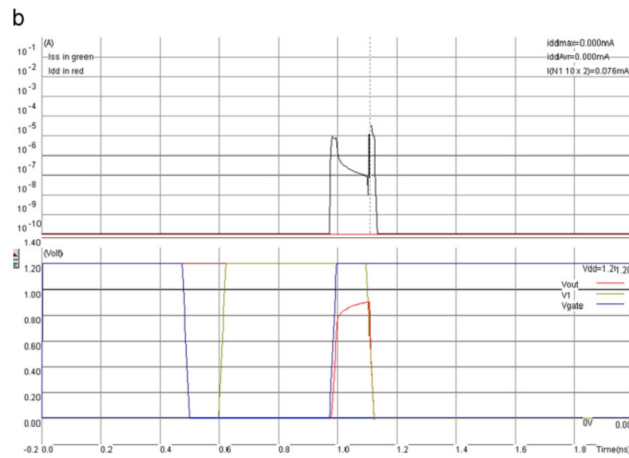


Figure 3: Current of (a) DG MOSFET and (b) SG MOSFET with output voltage

DATA ANALYSIS

Potential Uses of Si1-xGex in Various Configurations for Double-Gate MOSFETs

The findings of our research, comparison, and analysis of the various Si1-xGex combinations are given in Tables 1, 2, 3, Figures 4 and 5. We've also compared our findings to those of other studies' settings to highlight its merits and drawbacks. With Si1-xGex, the findings reveal that double-gate MOSFETs perform better than single-gate MOSFETs.

- Power dissipation is reduced,
- Voltage control is dynamic,
- Gate electrostatic control in the conducting channel is enhanced and
- The device is very reliable.

Table 1: Different Configurations of Si1-xGex used

Configurations of $Si_{1-x}Ge_x$	Single Gate	Double Gate
Si	Utilized	Utilized
$Si_{0.2}Ge_{0.8}$	Utilized	Utilized
$Si_{0.6}Ge_{0.4}$	Utilized	Utilized

Table 2: Single-Gate MOSFET using Si1-xGex and Double-Gate MOSFET using Si1-xGex

Performance Parameters	Single Gate MOSFET using $Si_{1-x}Ge_x$	Double Gate MOSFET using $Si_{1-x}Ge_x$
Bandgap of Channel Material	Multiple of 1.12 eV	Multiple of 0.66 eV
Drive Current Delay	In the Range of 0.1 ns	In the Range of 0.05 ns
Electric Field	$3*10^5$ Vcm^{-1}	10^5 Vcm^{-1}
Electron Mobility of Channel	Magnitude Order of 1500 $cm^2V^{-1}s^{-1}$	Magnitude Order of 3420 $cm^2V^{-1}s^{-1}$
Hole Mobility of Channel	Magnitude Order of 450 $cm^2V^{-1}s^{-1}$	Magnitude Order of 1610 $cm^2V^{-1}s^{-1}$
Off-State Leakage Current	More than 1 $nA\mu m^{-1}$	Less than 1 $nA\mu m^{-1}$
Power Dissipated	In Between 0.5 Js^{-1} and 0.7 Js^{-1}	In Between 0.1 $Js^{-1}$and 0.3 Js^{-1}
Threshold Voltage	In Between 350 mV and 450 mV	In Between 100 mV and 300 mV

Table 3: Double-Gate Configuration for pure Si and for Si1-xGex (x = 0.8 i.e., Si0.2Ge0.8)

Performance Parameters	Double-Gate using pure Si	Double-Gate using $Si_{1-x}Ge_x$ (x = 0.8 i.e., $Si_{0.2}Ge_{0.8}$)
DIBL	80 mdB	66.66 mdB
MMCR	$1.3*10^8$	$2.7*10^8$
Subthreshold Swing	82.23 mV/dB	86.84 mV/dB
Threshold Voltage	In Between 100 mV and 300 mV	In Between 100 mV and 300 mV

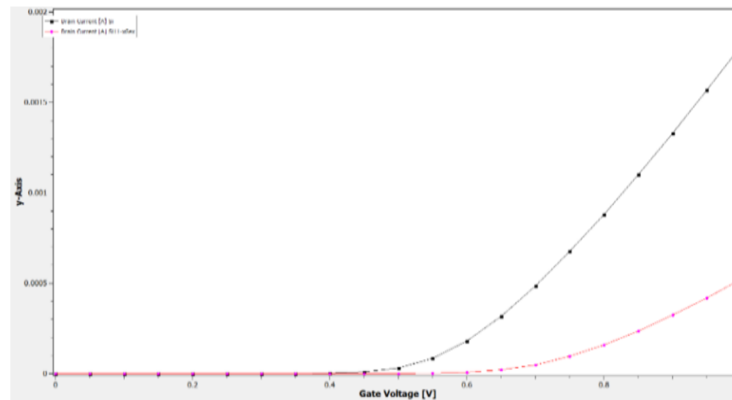


Figure 4: Comparing Id-Vg characteristics of double-gate configuration for pure Si and double-gate configuration for Si1-xGex

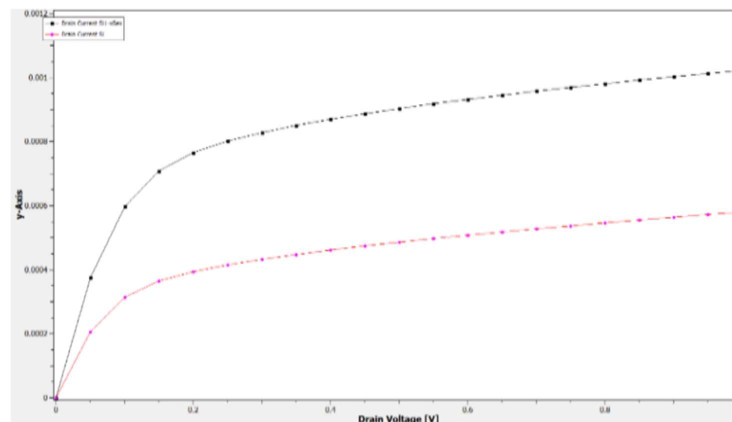


Figure 5: Comparing Id-Vd characteristics of double-gate configuration for pure Si and double-gate configuration for Si1-xGex

In the preceding part, we measured a variety of performance indicators, the values of which are already specified in Table 3.

The DG MOSFET and SG MOSFET effective capacitance of RF CMOS

Fig. 6(a) and (b) depict models of a double-gate MOSFET and a single-gate MOSFET transistor, respectively, in the ON-state of the switch, when the transistor is biased in the linear area. In normal operating conditions, the ON-resistance and substrate resistance of a double-gate MOSFET or a single-gate MOSFET are sufficient to overcome the insertion loss. In contrast, signal coupling via parasitic and junction capacitances means that the switch's isolation is not infinite. While at the cut-off area, the resistance of the MOSFET (R_{ON}, R_{ON1}, and R_{ON2}) goes to zero. If we assume that all possible capacitances exist simultaneously, we may achieve maximum capacitance. Whereas a single-gate MOSFET has just the parasitic capacitances Cds, Cgs, and Cgd and the junction capacitances Csb and Cdb, a double-gate MOSFET has the additional capacitances Cds1, Cds2, Cgs1, Cgs2, Cgd1, and Cgd2.

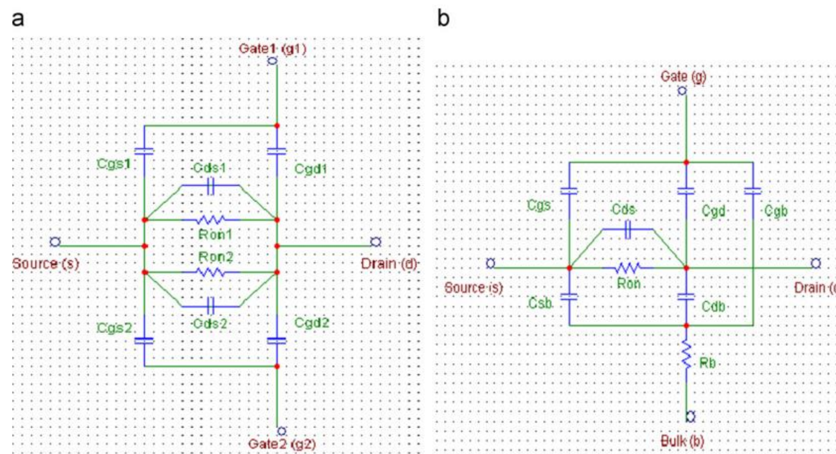


Figure 6: Models of a (a) DG MOSFET and (b) SG MOSFET transistor operating as a switch at ON-state

When both transistors in a DG MOSFET are turned on, neither Csb nor Cdb is present; as a result, fewer signals are linked to the substrate, and the substrate resistance Rb does not dissipate. As there is no capacitive coupling between the source and drain while the transistor is in the cut-off zone, a rise in Cds1, Cds2, Cgd1, Cgd2, Cgs1, and Cgs2 results in more isolation between the source and drain. Whereas for SG MOSFET, raising Csb and Cdb causes more signals to be coupled to the bulk and dissipated in the bulk resistance Rb while the transistor is ON. Capacitive coupling between the source and drain decreases transistor isolation in the cut-off region (higher Cds, Cgd, and Cgs). Figure 6(a) shows the maximum possible capacitance between the source and drain of a DG MOSFET.

$$C_{DG} = C_{ds1} + C_{ds2} + \frac{C_{gs1}\, C_{gd1}}{C_{gs1} + C_{gd1}} + \frac{C_{gs2}\, C_{gd2}}{C_{gs2} + C_{gd2}} \quad (2)$$

The ON-resistance will equal the sum of the resistances imposed by gates 1 and 2, as shown below:

$$R_{DG} = \frac{R_{ON1}\, R_{ON2}}{R_{ON1} + R_{ON2}} \quad (3)$$

Maximum source-to-drain capacitance for an SG MOSFET is shown in Fig. 6(b).

$$C_{SG} = C_{ds} + \frac{C_{gs}\,(C_{gd} + C_{gb})}{C_{gs} + C_{gd} + C_{gb}} + \frac{C_{sb}\, C_{db}}{C_{sb} + C_{db}} \quad (4)$$

Where Cgb is the capacitance between the gate and the bulk, and ON-resistance is the sole resistance present because of the single gate:

$R_{SG} = R_{ON}$ (5) where

$$R_{ON} = \frac{1}{\mu C_{ox}(W/L)(V_{gs} - V_{th})} \quad (6)$$

As capacitance CDG>CSG was calculated using Eqs. (2) and (4), this demonstrates that double-gate MOSFETs are more isolated than single-gate MOSFETs. Another indicator that double-gate MOSFETs have superior source-to-drain current flow is the lower RDG<RSG resistance. Parameters for DG MOSFETs and SG MOSFETs are compared in Table 4. DG MOSFETs are more suitable for RF CMOS switch design since their gain remains constant up to 0.60 V, whereas SG MOSFETs only maintain their gain up to 0.40 V. Here, the DG MOSFET is suitable for the DP4T switch since its ON-resistance (R_{ON}) is just half that of the SG MOSFET.

Table 4: Comparison of the various circuit parameters of the DG and SG MOSFETs for the proposed model

Parameters	Double-gate MOSFET	Single-gate MOSFET
Gate/control voltage (V)	1.2	1.2
Drain to source current ($I_{ds,max}$) (μA)	80	76
Output voltage ($V_{out,max}$) (V)	0.53	0.90
Capacitance	C_{DG} (More)	$0.7C_{DG}$ (Less)
ON-resistance (R_{ON})	0.5 R_{ON} (Less)	R_{ON} (More)
Thickness of oxide layer (μm)	3	2
Resistance of poly/gate (Ω)	68	32
Number of capacitors	6	6
Bulk capacitor	No	Yes
Gain (up to 1) (V)	0.60	0.40

Similar models and simulations of a DG MOSFET and SG MOSFET have been created. When the DG MOSFET and SG MOSFET have been designed, we create the layout and run simulations on the MOSFETs' accessible parameters.

CONCLUSION

Due of their many applications, metal-oxide semiconductor field-effect transistors (MOSFETs) are highly sought after. As compared to bipolar transistors (bipolar junction transistors/BJTs), a MOSFET's key benefit is that it needs practically minimal input current to regulate the load current. The Metal-Oxide-Semiconductor Field-Impact Semiconductor (MOSFET) has formed the backbone of integrated circuits for quite some time now. Technology has progressed to the point where several MOSFET configurations have been discovered with channel lengths of 0.1 pm or less. A bright future for Si1-xGex's capabilities, such as high carrier mobility, high speed, low power consumption, and low power dissipation, emerges from this investigation. As performance metrics are taken into account, it has the potential to replace Si within the next decade. It satisfies all requirements for maintaining CMOS circuit design of ICs, which is crucial in many fields, including electronics and communications. After much debate, we settled on the conclusion that DG MOSFETs are superior than SG MOSFETs. The suggested DP4T CMOS switch design employs double-gate transistors to provide isolation at lower control voltage and higher switching speed than is possible with standard analog switch circuit design.

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