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Low Power Voltage Controlled Oscillator using Hybrid CMOS CNTFET Technology

Dolly Sharma
Department of Electronics & Communication
Shri ram College of engineering and management, Banmore

Ashish Dubey
Assis.Prof.
Department of Electronics & Communication
Shri ram College of engineering and management, Banmore

Abstract: A voltage-controlled oscillator (VCO) made of hybrid CMOS is presented in the study; it has a low power consumption and a linear response across a broad power range. field-effect transistors based on carbon nanotube hybrid voltage CMOS. In this study, controlled ring oscillators are introduced. These designs use the capabilities of the CNTFET in addition to the benefits of high-frequency performance without sacrificing power consumption. have a significant impact on the three-stage ring oscillator's oscillation frequency when supplied at 0.7V. An output frequency regulator was used. The frequency of CMOS voltage-controlled oscillators (VCOs), power dissipation, and hybrid VCOs are examined. Without the necessity for a resistor or broad device, Combine the responsiveness of CMOS and CNTFET outputs using a CMOS-VCO hybrid. Excellent linearity is shown by the circuit when compared to a CMOS pure circuit with tuning and control voltages of 0.7V.

Key Words: Voltage Controlled Oscillator, Operating Frequency, CMOS, Power consumption, Cadence.

I. INTRODUCTION

The VCO is a mixed-signal analogue electrical circuit component that is frequently employed in electronic circuits that combine and convert analogue and combined signals, such as in PLLs (Phase-Locked Loops) and ADCs (analog to digital converters) [1], [2]. VOC designs consist primarily of topologies like LC tank oscillators and VCOs. VCOs have a relatively broad tuning range in PLL applications; in contrast to LC oscillators, the silicone region is narrower in VCOs, making them highly suitable for silicone integration [3]. The noise phase efficacy of superior LC tank oscillation with PLL design when compared to the VCO spring oscillator [5] [4]. A voltage control oscillator-based current CSVCO structure is used that consists of various stages of the VCO that resemble current starved voltage controlled oscillators and inverter stages that are voltage regulated. [6]. With hysteresis and a solitary inverter comprising a solitary VCO phase, Schmitt triggers require a reduced number of circuit transistors when compared to CSVCO. This work suggests the use of Schmitt's CMOS and CNFET-Ansatz to create a hybrid voltage-regulated oscillator. Hybrid circuits are considered to be specifically designed to have improved linearity and lower power consumption compared to pure CMOS circuits. The proposed VCO is simulated in the HSPICE environment.Carbon nanotube-enhanced gate electrostatics, exceptionally high electron mobility, and effective carrier transport all contribute to the exceptional interface channel performance of CNFETs.[7][8]. CNFETs were subjected to comprehensive analysis not only in the context of fundamental integrated circuits like logic portals and ring oscillators, but also in various analogue and RF (radio frequency) circuits. Recently, it has been demonstrated that highly linear RF circuits and potential applications can benefit from CNFETs. The linearity of CNFETs is found to be similar to that of conventional MOSFETs, as demonstrated by researchers in [9]. The hybrid advancement of electronic circuits, employing both traditional MOSFETs and contemporary nanoelectronic systems, was a challenge encountered by numerous researchers. The [10] study proposes the incorporation of hybrid 3D CMOS-CNFET inverters. [11] A study conducted by researchers from Stanford University documented the implementation of co-integration for PCNFET and NMOS cascade amplifiers. [12] describes a chemical sensing application utilising a hybrid CMOS-CNFET configuration. CNFETs are recommended for gating in CMOS transistors that require power replacement [14]. These novel monolithic 3D building blocks comprising memory, RF, analogue, and computer components will help future-proof nanoelectronic systems. Researchers have demonstrated such three-dimensional integrated systems in [15] as hybrid

cointegration structures comprised of conventional CMOS silicon blocks and CNFET logic construction blocks. In this configuration, integrated circuit layers are stacked vertically.

II. LITERATURE WORK

Static and dynamic variations of a number of ring oscillator designs have been documented in prior research. The variable-length ring oscillator (VLRO) design proposed by Jordi P. Puigdemont et al. [16] is able to synchronously alter the output frequency while maintaining a glitch-free signal. Even with supply voltage ranges that are substantially below the prescribed values, the VLRO operates dependably in all circumstances, according to the authors. In their study, Vandana Shikhawar et al. [17] devised and simulated a nine-stage ring oscillator circuit. They reached the conclusion that the circuit operates at a minimal power consumption of 18.9% and provided a reference paper to support their claim. power dissipation, Jitter, noise margin, noise factor, phase margin, and other parameters of a nine-stage CMOS ring oscillator were examined by S. Kumar et al. [18]. As determined by the authors, the phase noise is -6.4 kdBc/Hz and the period fluctuation is zero at 933.5 picoseconds. Daniel P.Bautista et. al. [19] introduced a novel VCO that operates with a reduced power consumption and a broad frequency range. The delay cell incorporates partial positive feedback, supporting a single two-stage circuit and high speeds. Also, the VCO has good output frequency-control voltage linearity. Er F. Khtoon et al. [20] demonstrated how a ring oscillator is constructed by connecting numerous delay stages in a cascade with positive feedback. The suggested circuit, which has a tuning range of 125MHz to 561.798MHz, is best suited for PLL and timer circuits, according to the research. This oscillator requires an average power consumption of 3.6 mV and can operate on a 2.5 v power source. Victor Karam et. al. [21] examined the static CMOS inverter dependency oscillator to increase multi-GHz oscillation frequency. The technique was shown to provide a 21% speed improvement over previous efforts. 40 times less power is used than with the previous design approach, according to Vrastislav Michal et al. [22], who developed a straightforward method for optimising the CMOS ring oscillators' power and frequency dispersion. Abbas Ramazani et al. [23] analysed the relationship between variations in supply voltage and delay time, and proposed an innovative type of ring oscillator comprised of a standard inverter and a current-starved inverter. The authors claim that this CMOS ring oscillator has excellent stability even with voltage changes. SS Ali Salih et al. get. [24] studied the effect of two-phase phase alignment method on ring oscillators. The authors suggest that this new approach helps reduce the noise level in ROs and reduce the power consumption of ring oscillators.Because low power has so many applications, it is essential for building low power circuits in VLSIs. The main limitation for any low power VLSI circuit is power consumption because of its widespread use [25–28]. Throughout the design history, the primary goals of VLSI design have been to maximise power consumption and performance in order to achieve computationally real-time functions.

III. CIRCUIT DESCRIPTION

Ring-based oscillator design output from the initial stage entry. Figure 1 is a block diagram of the VCO of a single-stage N-delay inverter. A phase change of 2β and voltage increase of the apparatus are required to be executed in the event of an oscillation. Ring-based oscillator design output from the initial stage entry. Figure 1 is a block diagram of the VCO of a single-stage N-delay inverter. A phase change of 2β and voltage increase of the apparatus are required to be executed in the event of an oscillation. In the case of a late cell, it is necessary to specify a phase shift of Ÿ/N, where N denotes the overall count of delay phases. The residual ρ phase shift is generated through the inverter delay cell's dc reversion. DC inversion in the design of single-end oscillators is highly dependent on the unusual number of delay phases. N represents the total number of delay steps, while td denotes a delay for each stage. fo = 1/2Ntd represents the VCO oscillation frequency. The literature on transducer design has documented a range of delay cell configurations, such as dual-delay paths, single-ended delays, and multisfeedback loops. A variety of coupling cells, including delay cell strategies and latches and inverter stages, have been implemented. The efficacy of a VCO model is significantly impacted by the enhancement of delay phases, which are fundamental components of every VCO model. In light of the importance of energy consumption and frequency range, a novel delay cell is proposed in this study.

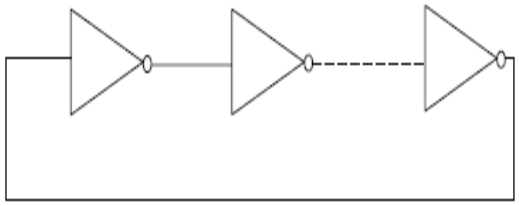

Figure.1: Inverter N-delay Single-ended VCO block diagram

Each delayed cell inverter's timing relies on the ring's VCO output frequency. Three transistor gates are used in the suggested designs for delay cells made of NAND. Figure 2's 3-transistor NAND gates were powered by an inverter.

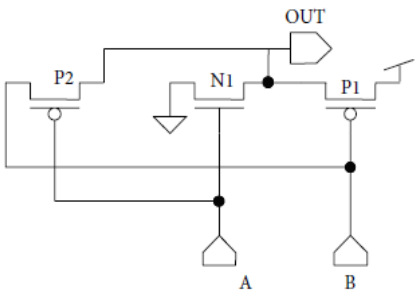

Figure.2: 3- CMOS transistor NAND gate.

IV. Proposed Hybrid CMOS Voltage Controlled Ring Oscillator (HCVCRO)

Due to the expansion of portable electronic devices as well as the reduction of technological scale and the limitations of MOSFET channel length reduction, the design of a low power ring oscillator with a wide frequency range and having the ability to adjust the frequency is necessary for many applications and many efforts are made in this field by designers [29-31]. To answer the challenges in [32], tunable ROs based CNTFET inverters have been proposed and have taken advantage of CNTFET. The high frequency and low power ROs introduced in

[32] have the ability to adjust the frequency and do not have any additional mechanism for adjusting the frequency. In [29] hybrid ROs based on CNTFET CMOS are introduced.

The circuit is examined in response to variations in parameters including control voltage (CV), induced frequency, and power dissipation. The ring oscillator uses a voltage-controlled order (VCO) consisting of n stages, each of which introduces nonlinearity.By implementing the topology depicted in Figure 3, this issue can be resolved by employing a solitary current stage of deprivation succeeded by a hysteresis trigger Schmitt. One of the uses for a Schmitt trigger is to power an RC oscillator. Schmitt is also capable of constructing a voltage-controlled oscillator in conjunction with current sources. Hybrid CMOS is employed in the fabrication of the Schmitt trigger according to the proposed design. Current sources are also reflected in MOSFETs PM0 and NM6 by HCVCRO. NM0 and PM2 both function as transistors. The inverter is constructed using standard MOSFETs. W/L=1.2 represents the hybrid implementation of MOSFETs. An important criterion for the use of PLL in VCOs is the overall bias. The linear response of hybrid circuits is improved compared to pure CMOS.As a result of employing high Vth devices to decrease power dissipation, unadulterated CMOS circuits exhibit a non-linear response. The crossover CMOS VCRO waveforms are depicted in Figure 4.

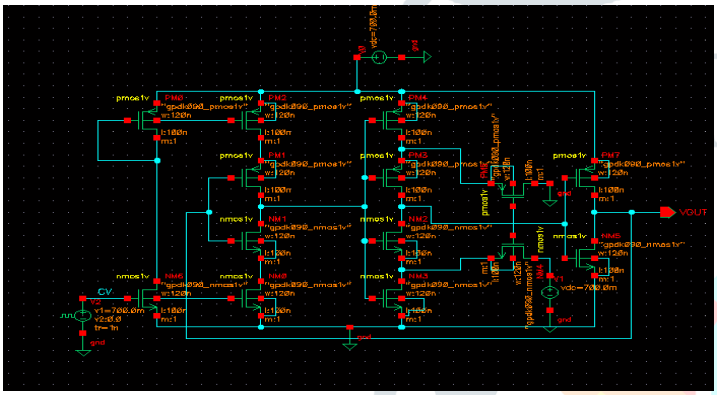

Figure.3. Schematic of HCVCRO

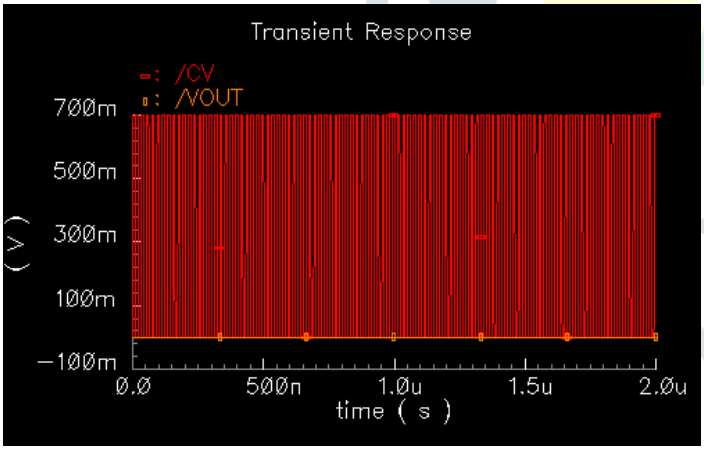

Figure.4. HCVCRO the output waveform of a hybrid CMOS device.

V. Proposed Hybrid CNTFET CMOS Voltage Controlled Ring Oscillator (HCCVCRO)

The aggregate nonlinearity of ring oscillator VCOs is contributed to by each of the n stages that comprise the VCO. the topology illustrated in Figure 6 may utilise a Schmitt trigger with hysteresis subsequent to a solitary current deprivation stage. Schmitt triggers serve as an integral component of an RC oscillator. Voltage-controlled oscillators can also be created by combining current sources with Schmitt triggers. In order to fabricate the Schmitt trigger, the proposed design employs CNTFETs. Furthermore, in the same way that transistors M5 and M6 reflect the currents in CNTFETs M1 and M4, they function as current sources. By utilising standard MOSFETs, the inverter is constructed. The starting voltage of 0.323V is related to the choice of CNTFET channel length.With an inter-CNT pitch of 4nm, three tubes are utilised.

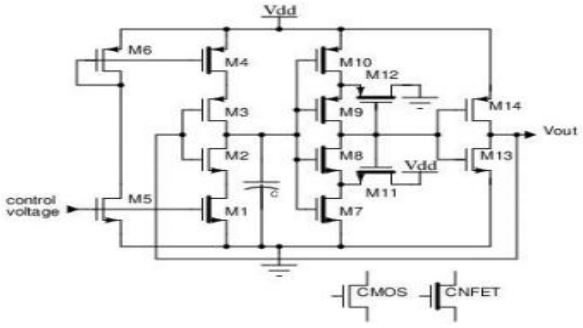

Figure 5: Voltage-controlled oscillator Combining CMOS and CNFET

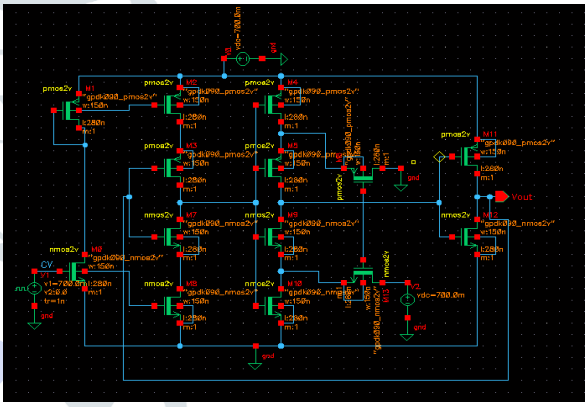

Figure.6. Voltage-controlled Hybrid CNTFET Ring oscillator (HCNTVCRO) diagram

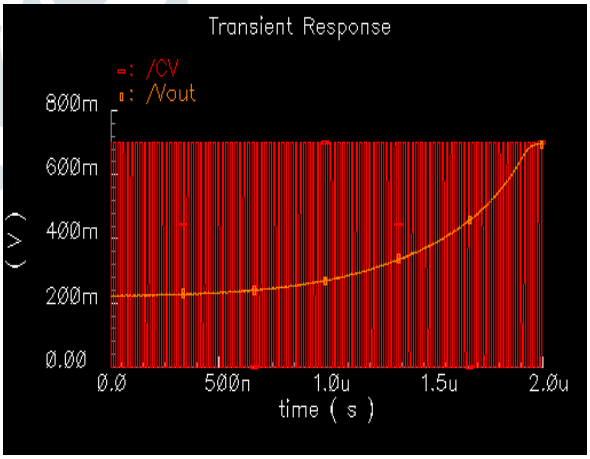

Figure.7. the voltage-controlled ring oscillation (HCNTVCRO) output waveform of a hybrid CNTFET.

In connection to these parameters, the regulated voltage, number of CNFET tubes, gate oxide thickness, inter-CNT pitch, CNFET chiral vectors (threshold voltage), and power dissipation of the suggested circuit are examined. The oscillator frequency in a

CNFET exhibits a linear relationship with the quantity of nanotubes present, given a specific control voltage (Figure 5). This provides an easy solution to meet VCO requirements for a PLL application by scaling the VCRO frequency during design. A CNFET's thin gate oxide increases the driving current and transconductance. gate oxide thickness's impact on a hybrid VCRO's frequency and power dissipation. Higher gate oxide thicknesses for low power VCOs may be utilised to lower driving current and lower dynamic power consumption.

VI. RESULTS AND DISCUSSION

The synthesis and simulation are completed for each design. CADENCE tool, a 90 nm technology, has a nominal supply voltage Vdd=0.7 V. It evaluates the performance of current adder designs and suggested hybrid CMOS and CNTFET VCRO solutions. At normal temperature (27 °C), delay cells are the only dominating mechanism with significantly reduced gate leakage. Reducing power loss and increasing design efficiency may be achieved by directly connecting ground and Vdd and tabulating all relevant characteristics, such as frequency and leakage power.

Table 1 Comparing the Performances of CMOS VCO with HCVCO

Performance Parameter	Proposed Hybrid CMOS VCRO	Proposed Hybrid CNTFET VCRO
Technology Used	90nm	90nm
Supply Voltage	0.7V	0.7V
Power consumption	11.09 µW	9.5 µW
Operating Frequency	4.8GHz	1.6GHz

VII. CONCLUSION

To linearize the VCRO response, CMOS-VCRO hybrid devices are employed, eliminating the need for a broad device or resistor. With a tuning and control voltage of 0.7V, the device exhibits superior linearity as compared to the pure CMOS circuit. Controlling the output frequency requires a supply voltage of 0.7V. The power frequency and power consumption of the scheme were studied in different parameters such as voltage control, number of CNFET tubes, gate oxide thickness, CNFET hole starting voltage and CNT gap.When a CNFET has a certain number of nanotubes, the oscillator frequency rises linearly with that CV. VCOs with a broad and linear tuning range are among the most important requirements for PLL applications.

REFERENCES

[1] Wang,S. F., 2015, "Low-Voltage, Full-Swing Voltage-Controlled Oscillator with Symmetrical Even-Phase Outputs Based on Single-Ended Delay Cells," in IEEE Trans. on Very Large Scale Integration (VLSI) Systems, 23(9), pp. 1801-1807.

[2] SawS. K., and NathV., 2015, "Performance Analysis of Low Power CSVCO for PLL Architecture," Advances in Computing and Communication Engineering (ICACCE), Second International Conference on, Dehradun, pp. 370-373.

[3] Kamalinejad, P., Keikhosravy,K., Molavi,R., Mirabbasi, S., and Leung,V. C. M., 2014, "An ultra-low-power CMOS voltage-controlled ring oscillator for passive RFID tags," New Circuits and Systems Conference (NEWCAS),IEEE 12th International, Trois-Rivieres, QC, pp. 456-459.

[4] Li, G.,and Afshari,E., 2010, "A Low-Phase-Noise Multi-Phase Oscillator Based on Left-Handed LC-Ring," in IEEE J. of Solid-State Circuits, 45(9), pp. 1822-1833.

[5] Ling, Sun, et al., 2010, "CMOS ring VCO for UHF RFID readers," The J. of China Universities of Posts and Telecommunications, 17(3), pp.20-23.

[6] Kougianos, Elias, and Mohanty, S. P., 2009, "Impact of gate-oxide tunneling on mixed-signal design and simulation of a nano-CMOS VCO." Microelectronics J., 40(1),pp. 95-103.

[7] Yang, M. H. et. al., 2006, "Advantages of top-gate, high-k dielectric carbon nanotube field-effect transistors," Appl. Phys. Lett., 88(11), pp. 113507.

[8] Appenzeller,J., Knoch,J., Martel,R., Derycke,V., Wind,S. J., and Avouris,P., 2002, "Carbon nanotube electronics," in IEEE Trans. on Nanotechnology, 1(4), pp. 184-189.

[9] Alam,A. U., Rogers,C. M. S., Paydavosi,N., Holland,K. D., Ahmed, S., and Vaidyanathan,M., 2013, "RF Linearity Potential of Carbon-Nanotube Transistors versus MOSFETs," in IEEE Trans. on Nanotechnology, 12(3), pp. 340-351.

[10] Meric,I., Caruso,V., Caldwell,R., Hone,J., Shepard,K. L., Wind,S. J.,2007, "Hybrid carbon nanotube-silicon complementary metal oxide semiconductor circuits," J. Vac. Sci. Technol. B, 25(6),pp. 2577-2580.

[11] Akinwande,D., Yasuda,S., Paul,B., Fujita,S., Close,G., and Wong,H., 2008, "Monolithic integration of CMOS VLSI and carbon nanotubes for hybrid nanotechnology applications," IEEE Trans. on Nanotechnology, 7(5), pp. 636-639.

[12] Cho,T.S., Lee,K.J., Pan,T., Kong,J., Chandrakasan,A.P., 2007, "Design and characterization of CNT-CMOS hybrid systems," MTL Annual Research Report.

[13] Chakraborty et. el., 2007, "Hybridization of CMOS with CNT-based nano-electromechanical switch for low leakage and robust circuit design," IEEE Trans. on Circuits and Systems—I: Regular Papers, 54(11),pp. 2480-2488.

[14] Kim,K. K., Kim,Y.B., and Choi,K., 2011, "Hybrid CMOS and CNFET power gating in ultralow voltage design," IEEE Trans. on Nanotechnology, 10(6), pp. 1439-1448.

[15] Shulaker,M. M., Wu,T. F., Sabry,M. M., Wei,H., Wong, H. S. P., and Mitra,S., 2015, "Monolithic 3D integration: A path from concept to reality," 2015 Design, Automation and Test in Europe Conference and Exhibition (DATE), Grenoble, pp. 1197-1202.

[16] J. P.-Puigdemont, France Moll and A. Calomarde, "All digital simple clock synthesis through a glitch free variable length ring oscillator," IEEE Trans. On circuit and system -II: Express Briefs, vol. 61, no. 2, February 2014.

[17] V. Sikarwar, Neha Yadav and S. Akashe, "Design and Analysis of CMOS ring Oscillator using 45nm technology," ,IEEE International advance computing conferece,2013, pp. 1491-1495.

[18] Sushil Kumar and Dr. Gurjit Kaur, "Design and Performance analysis of nine stages CMOS based ring oscillator," International journal of vlsi design and communication systems, vol.3, no.3, june 2012.

[19] D. P. Bautista and Monico Linares Aranda, "A Low power and high speed CMOS voltage-controlled ring oscillator," IEEE ISCAS, 2004, vol. 4, pp.752-755.

[20] Er F. Khatoon and Er T A chandel, "Design of ring vco using nine stages of differential amplifier," International Journal of Research in Engineering and Technology, vol.03, june 2014. [21] Victor Karam, N. Fong and C. Plett, "parasitic –aware delay optimization for multi-GHz static CMOS ring oscillators," IEEE North-East Workshop on Circuit and System, 2006, pp. 101-104.

[22] Vratislav Michal, "On the low power design, Stability improvement and frequency estimation of the CMOS ring oscillator," International Conference Radioelektronika, 2012, pp. 1-4.

[23] Abbas Ramazani , S. Biabani and Gholamreza Hadidi, "CMOS ring oscillator with combined delay stages," International Jouranal of electronics and communications, vol. 68, pp. 515-519, 2014.

[24] Sajjad Shieh Ali Saleh and Nasser Masoumi, "The dual-edge alignment technique with improved spur reduction effects in ring oscillator," Microelectronics Journal, vol. 42, pp. 874-882, 2011.

[25] Uroschaint Yodprasit, C. Botteron and P-Andre Farine, "Shunt Feedback ring oscillator: A new topology for wideband multiphase signal generations," IEEE International workshop on radio-frequency integration technology, Dec 2007, pp. 78-81.

[26] M Kumar, Sandeep K. Arya and Sujata Pandey, "Low power voltage controlled ring oscillator Design with substrate biasing," International Journal of information and electronics engineering, vol. 2, no. 2, March 2012.

[27] Wen-Tsong Shiue, "Leakage power estimation and minimization in VLSI circuits," IEEE International Sympposium on Circuit and System, 2001, vol. 4, pp. 178- 181.

[28] Rishi Todani, A K Mal, and Kanchan Baran Maji,"IACSIT International Journal of engineering and technology, vol. 4, no. 6, December 2012

[29] A. Baghi Rahin, A. Kadivarian, V. Baghi Rahin, "Investigation of Different Combinations of CNTFET and MOSFET in the Structure of a Hybrid Ring Oscillator," 2021 IEEE 6th Conference on Technology in Electrical and Computer Engineering (ETECH 2021), 2021.
[30] A. Baghi Rahin, A. Kadivarian, V. Baghi Rahin, "Extremely High Frequency and Low Power Ring Oscillators Using DGCNTFET Transistors," 2021 IEEE 6th Conference on Technology In Electrical and Computer Engineering (ETECH 2021), 2021.
[31] A. Baghi Rahin, M.H. Akhtarzadeh, A.S. Alijanpour, V. Baghi Rahin, "Tunable Ring Oscillator Based on DTMOS and FGMOS Inverters with High Frequency and Low Power in 180 nm CMOS Technology," 8th National Conference on Modern Studies and Research in Computer, Electrical, and Mechanical Sciences of Iran, 2022.
[32] A. Baghi Rahin, A. Kadivarian, S. Naseri Akber, V. Baghi Rahin, "Tunable Ring Oscillators Based on Hybrid FGMOS/CNTFET Inverters with High Frequency and Low Power," International Conference on New Researches and Technologies in Electrical Engineering (ICNRTEE) University of Science and Culture (USC), 2023