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Efficient 128-bit Binary Counter With Optimized Clock Period

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Abstract: The design of a high-performance 128-bit binary counter is examined in this work, with a major goal of minimizing clock period and delay. The suggested counter increases speed and efficiency by utilizing semiconductor technologies and sophisticated circuit design. To minimize power consumption, the design examines cutting-edge technology like Fin FET transistors and includes parallel computing and effective flip-flop utilization. Stages in the pipeline are also added to further maximize performance. With its thorough examination of the design decisions, simulations, and experimental findings, the paper sets itself up for publication in a respectable journal or conference. The research, that has been carried out with Xilinx 14.5 and Verilog coding, shows a viable direction for improving digital circuit design.

Index Terms - Backward Carry propagation / Johnson Counter / Pre-scale Enable Signal / **Pre-Scaled Counter** ***/ Binary counter***

I. Introduction

The incredibly creative field of counters extends its reach beyond simple measuring methods into ADC, frequency divisions, PLL frequency synthesizers, and other domains. With the development of technology, there is an increasing need for large, quick counters that can count at a steady pace. However, a paradoxical dance develops between the counter size and the counting pace, where an increase in counter size causes a carry to require a longer journey, upsetting the balance.

To meet this challenge, the traditional ripple carry chain gracefully moves aside to allow the cutting-edge carry look-ahead circuit to take its place. This transformation not only calms the waves but also sets up a dance in which the carry chain takes on the grace of a tree, opening the door to previously unheard-of speed.

The Manchester carry chain, a clever conductor arranging the carry propagation symphony, now comes into play. A maestro-like state look-ahead conducts a D flip-flop symphony, erasing the rippling effects that had disturbed the counters tranquility. After serving as the primary character, the binary sequence makes way for systolic structures and backward carry propagation (BCP).

By acknowledging the hierarchical structure of binary sequences, BCP reveals its genius by enabling more important bits to fly higher than their less important counterparts. The torchbearer, or least significant bit (LSB), efficiently guides the entire counter. However, problems arise the fan-out problem, in which the LSB bears the entire demand with the crippling problem of input ports exceeding the maximum value of the LSB.

A pre-scaling-based synchronous binary counter that generates sub-blocks that establish clock periods and enable signals to develop in the pursuit of counter-perfection. Unfortunately, the fan-out problem still exists and could potentially overshadow the design's genius. The fan-out problem becomes a powerful antagonist as counter-size grows, resulting in delays that reverberate along the propagation corridors. But the answer turns out to be a binary sync counter—a miracle that overcomes the limitations of fan-out problems. This counter achieves synchrony that makes counter size irrelevant by adopting the BCP methodology and doubling the single-bit Johnson counter.

The LSB emerges as the only conductor, arranging a climax of counting velocity unrestrained by the counter's size. Reprogrammable clocks reveal themselves through a dynamic interplay that enables counters to adjust to a wide range of clock speeds and applications. However, the counter's delay values pirouette in unison with the clock's fluctuations, displaying a ballet of flexibility and resiliency. The counter's output dances between different bits, up to 128 in this innovative symphony, providing a tapestry of clock rates, each woven with distinct variations in area and delay.

2. Existing and Proposed Counters Top of Form

2.1. Existing Counter

When it comes to counters, the current leader is the n-MOD ripple counter, which may rise to 2n states and then return to the modest zero with grace. Imagine a flip-flop ballet, with every flip-flop rotating in toggle mode, and the external clock signal gently caressing one lonely flip-flop. Like the lead dancer, this selected flip-flop sends out a pulse that serves as the maestro's cue for the subsequent flip-flops. So the counting dance begins, with the Least Significant Bit (LSB) taking center stage as it gets the pulse from the external clock.

Enter the synchronous counter, which, unlike its asynchronous predecessor, is a virtuoso. In this case, a single world clock creates a work of art by directing every flip-flop to change states simultaneously. Because there is no cumulative delay, the synchronous counter has a magical characteristic that enables it to dance at frequencies higher than those of its asynchronous cousin.

The synchronous counter moves as one, driven by the heartbeat of a single clock, in a dance of accuracy and unanimity. Its unification characterizes the way it moves as well as its propensity to travel at higher frequencies, causing the asynchronous counter to fall behind.

The synchronous counter appears as a composed performer in this counting choreography, coordinated and harmonious, moving to the beat of a single beat. A synchronous counter moves with a grace beyond the broken motions of an asynchronous mode equivalent, as the external world clock pulses via its circuitry. It's a performance where every flip flop, in perfect harmony, embraces change simultaneously, creating a mesmerizing spectacle of counting prowess.

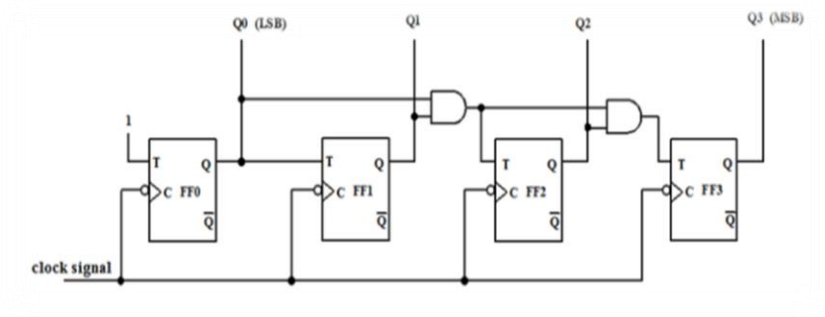


Figure 1. Synchronous Counter.

Ring counters frequently use shift registers. The ring counter and the shift counter are almost the same. The only difference is that the final f/f's o/p is related to the beginning f/f's; it serves as both an input and an outlet in ring counters and shift registers. Apart from that, not much has altered. The total number of states in the ring counter is equal to the total number of f/fs. It continuously produces a sequence of 1s and then 0s around the ring by connecting the output of the previous shift register to the source of the first register. Below is a schematic of the aforementioned counter.

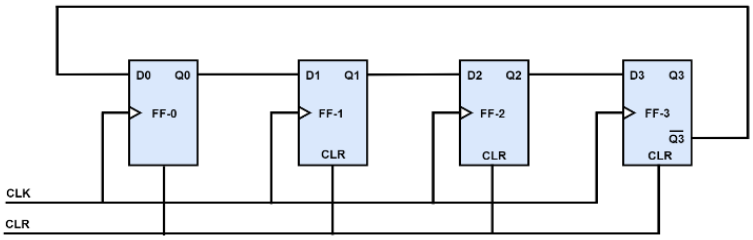


Figure 2. Schematic of Johnson Counter.

Flip-flops are used by the Johnson counter, also known as a creeping counter or synchronous counter, to generate an n-bit shift counter. In this setup, a reversing ring is formed by connecting the last flip-flop's output to the first one's input. The combined effect of the active and inactive stages yields 2n states in an n-bit Johnson counter, of which 2n−2*n states are used. The Johnson counter doubles the number of states while having a similar number of flip-flops as the ring counter. In those counters, J-K and D flip-flops are frequently used. The Johnson counter counts input signals continuously while using self-decoding technology. However, a drawback is that it doesn't follow a binary sequence, leading to a significant number of unused states compared to useful ones.

Additionally, only half as many clock signals are required for flip-flops, allowing for the incorporation of various timing patterns. For a reliable binary output, a synchronous binary counter is recommended. A ripple carry counter employs a one-bit adder with carry-out linked to the carry-in of the next step. The term "ripple carry chain" describes how ripples are introduced into the carry pulse, causing delays in a synchronous counter's carry chain. To address this, a carry look-ahead design has been introduced to replace the conventional ripple carry chain, resulting in significant performance gains.

Attempts to enhance counter speed include altering flip-flop designs and utilizing real single-phase clocks. High-speed counters with systolic structures, pipelined chains for carry propagation, and other innovations have been developed, albeit with increased hardware overhead. Another technique involves using a Linear Feedback Shift Register (LFSR) to modify state sequences, creating different states corresponding to powers of two.

Introducing Binary Carry Propagation (BCP) with a carry look-ahead strategy helps reduce logic depth. In this approach, three phases (a, b, c) are employed to split the counter. Phase A outputs are connected to the carry look-ahead design to decrease logic depth, enabling faster processing. BCP, outlined in the proposed section, involves toggling signals based on clock pulses and specific gate configurations.

Backward carry propagation is utilized to combine information from phase A and phase B, creating toggle outputs for phase C. Cascaded AND gates are employed for phase C, generating a small BCP sequence for each bit. The ripple carry sequence of a basic counter limits data transmission time, taking advantage of the fact that more significant bits go high before less significant bits in a binary sequence. However, challenges arise with the least significant bits (LSB) in terms of fan-out and exceeding maximum values. To address this, a pre-scaling-based synchronous binary counter has been introduced.

2.2. Proposed Counter

The key to quickly implementing synchronous counters is to understand the fundamentals of Binary carry propagation (BCP). This invention takes advantage of the intrinsic characteristics of the binary number system, which is that the most significant counter bit rises before the less significant ones. Each counter bit in this architecture has its own reverse-attached link, as opposed to a traditional binary counter with a single chain. Signals arriving earlier in a carry chain are examined before those arriving later.

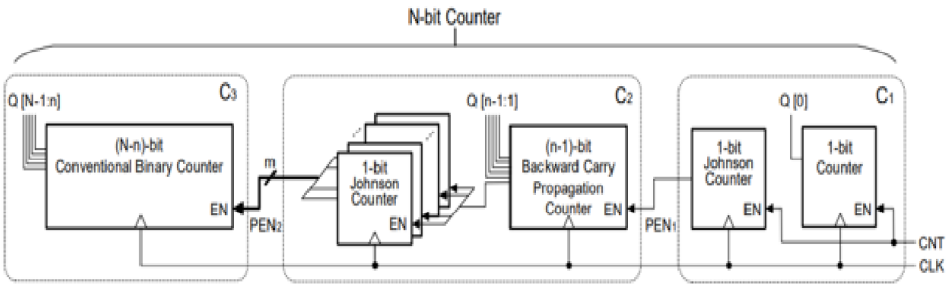


Figure 3. Schematic of proposed N-bit Counter.

The initiation of a least significant bit (LSB) change pulse is seamlessly integrated with the final AND gate of the carry chains. This results in the definition of the backward carry propagation critical delay path, where the latency of the ultimate AND gate and a T-flip-flop are pivotal factors affecting propagation delay. Notably, the LSB (Q.(0)) connects all AND chains, leading to substantial fan-out. Alternatively, the burden on the LSB is considerable for rapid operation, relying on fan-out for the crucial route delay.

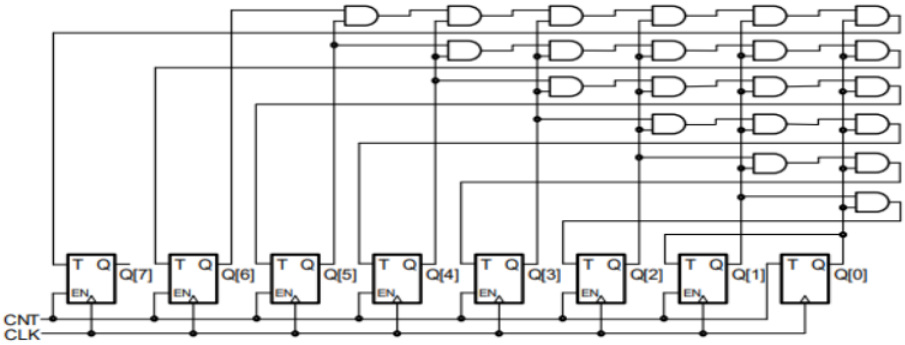


Figure 4. 8-bit synchronous counter made with BCP.

This counters sequence manufacture proceeds through a block of counters, 00...000 through 11...111. A standard counter consists of an increment component that determines the value that will be incremented and a register that holds the current state. The counting rate is mostly constrained by the computation time of the increment, and pre-scaling appears as a way to reduce this latency. By dividing the suggested counter architecture into three sub-counters, an N-bit size is achieved.

$C1$: A single-bit counter alternating between 1 and 0 per clock cycle.
$C2$: An (n-1)-bit counter utilizing BCP.
$C3$: A binary counter of size (N-n)-bit.

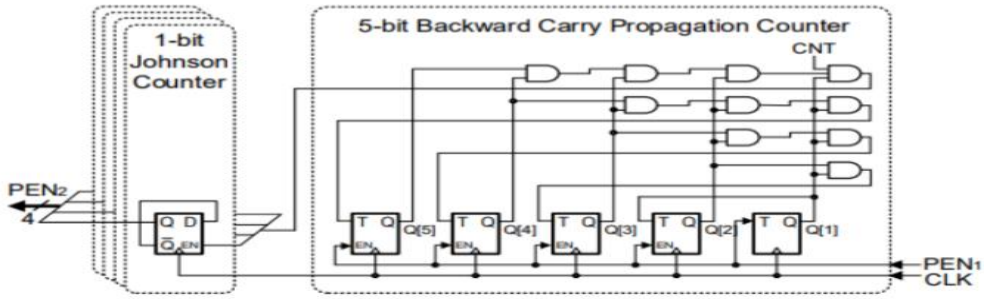


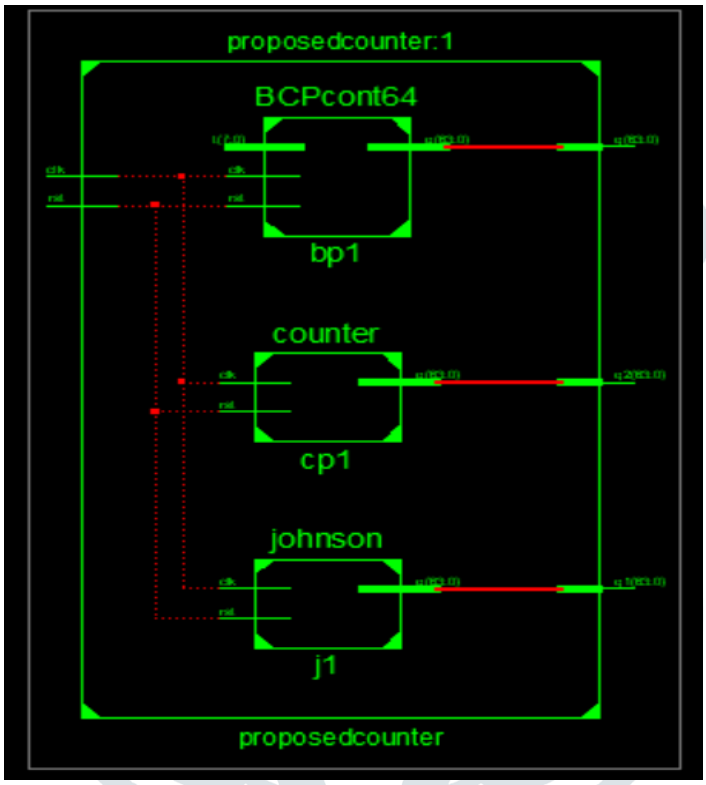
Figure 5. Pre scaled enable signal production having redundant Johnson counter.

The partitioned counter assumes pre-scaling in the high-order block while considering the lower-order block. The duration of PEN2 created in $C2$ is less than the synchronous ripple carry binary counter $C3$'s propagation delay. The (n-1)-bit carry propagation counter $C2$, a sub-counter of the 1-bit counter $C1$, is enabled backward, ensuring that $C2$'s carry propagation takes less time than $C1$'s PEN1 formation. To synchronize the PEN signal with the clock without fan-out delay, a two-bit ring counter generates pre-scaled enable signal 1, and a 64-bit ring counter generates pre-scaled enable signal 2. Despite PEN1 having negligible fan-out, PEN2's control over 58 enable ports in $C3$ necessitates addressing the delay induced by significant fan-out. The implementation and simulation results reveal that PEN2's propagation delay poses a critical route challenge.

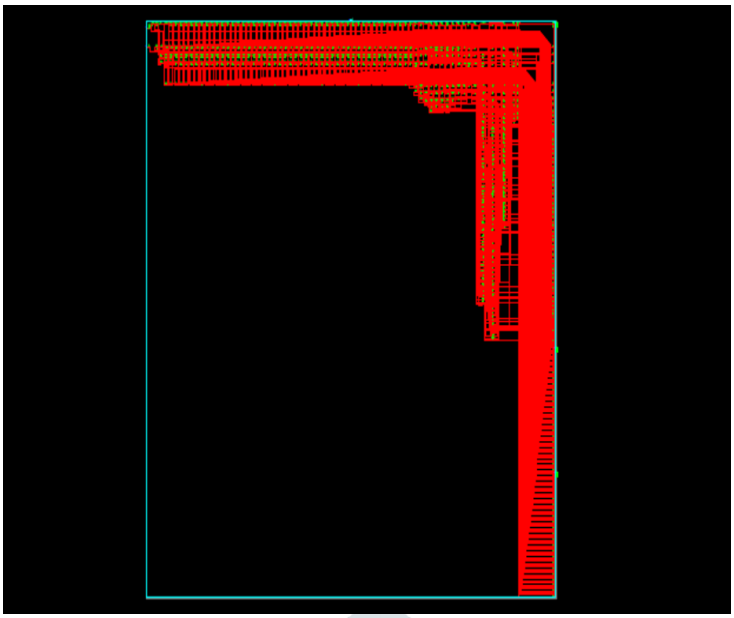
To overcome the fan-out issue, a 2n-bit ring counter replaces a bit Johnson counter, where N is 64, and n and m are 6 and 4, respectively. The single-bit Johnson counter, copied twice to handle nodes with substantial fan-out, follows the formula m = (N-n)/L to determine the number of redundant Johnson counters. The complexity introduced by redundancy is minimal, given the limited number of redundant flip-flops, making it a minor fraction of the total counter's complexity.

3. Performance Analysis

This section implements a 128-bit counter using 3 sub-counters and the schematic and evaluation are given below. The performance analysis between the pre-scaled counter employing ring counters, backward carry propagation counter, and the proposed counter technique is described below:



(a)



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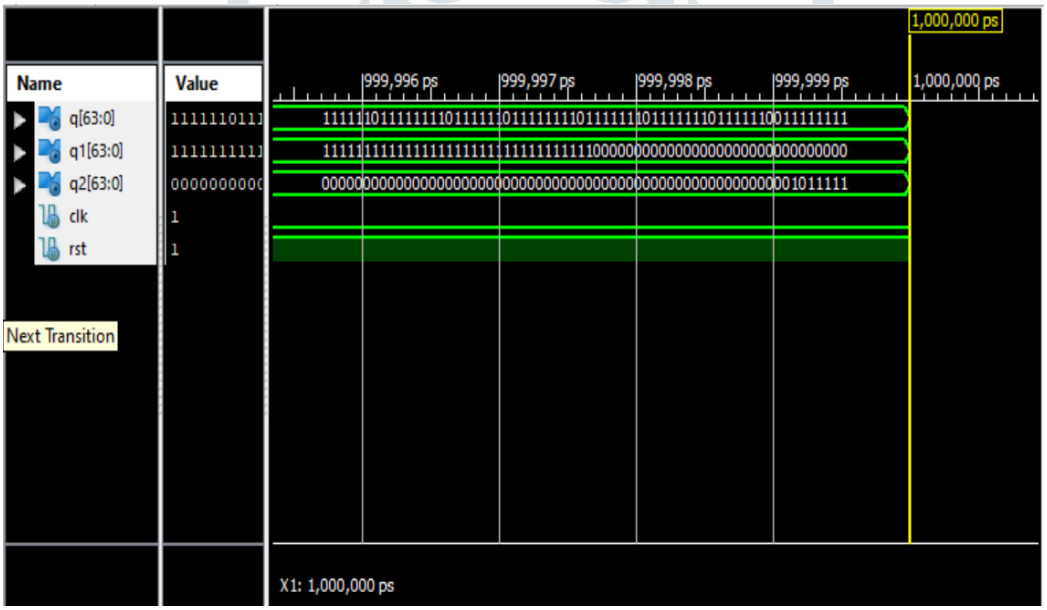

(c)

Figure 6. (a) RTL Schematic; (b) Technology Schematic; (c) Simulation.

Table 1. Performance analysis and evaluation of the proposed design of the counter.

	Comparison		
	Evaluation		
	Area (LUT'S)	Delay(ns)	Counter Size(bits)
Previous prop	104	2.44	64
Proposed prop	144	3.23	128

Table 2. Defines the performance comparison of various techniques used for the low number of flip-flops. It is quite evident from the table above that the proposed counter has few flip-flops compared with other techniques.

Various techniques used	Comparison			
	Previous work		Proposed work	
	No. of Flip Flops		Overall gate counts	
Backward Carry propagation	65	200	1600	9312
Pre-scale counter using a ring counter	100	124	850	4656
Proposed counter	65	74	800	9312

4. Conclusion

Explore the world of creativity with a synchronous binary counter, a marvel that gracefully uniformly in delay across a range of sizes. A flip-flop dance develops, its beat unaffected by the size of the counter. See how the clock changes shape to accommodate applications with different tempos and how a dynamic ballet introduces different delay values. The visual symphony that is the output of the counter reveals complex patterns up to 128 bits and provides a range of clock rates that add complexity to the paper concerning area and delay. Time and design connect smoothly, with the binary counter working as a conductor in this technical waltz.

4. References

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