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Simulation of PD, POD and APOD Control Techniques Based Cascaded H-Bridge Multilevel Inverter

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Abstract: **Since its invention, power quality has been a significant concern, but only recently, has it established the main focus for consideration by various researchers because of its dangerous effects on electrical equipment. Not only are options to ensure stable power supply assured with proper consideration of power quality, but inverters with harmonic reduction are also required. Seven methods combined with various level shifted Pulse Width Modulation strategies namely phase disposal, phase opposition disposition and alternative phage opposition disposition for cascaded H bridge Multilevel Inverter are ran with seven. line voltage and total harmonics distortion is obtained and compared in this project titled "SIMULATION OF PD, POD AND APOD CONTROL TECHNIQUES BASED CASCADED H-BRIDGE MULTILEVEL INVERTER"**

Keywords: **Inverter, Simulation, PD, POD, APOD, THD.**

I. INTRODUCTION

Nowadays the world community relies heavily on non-renewable energies, but just after the big oil crisis the use of renewable energy has greatly increased and has become the main interest of many countries for its many advantages such as minimal impact on the environment, renewable generators requiring less maintenance than traditional ones and it has also a great financial impact on economy. It is easy to get charmed by the advantages of using the renewable resources but we must also be aware of their disadvantages. One of the major disadvantages is that the renewable energy resources are intermittent and thus they have led scientists to develop new semiconductor power converters among which is the multilevel converter used in medium voltage and high voltage. These inverters convert the available direct current supplied by the PV panels or batteries and produce a staircase output waveform used to feed the grid. One of the major advantages of multilevel inverters is the remarkable improvement of the spectral quality of the output signals and therefore they have proven to be more effective than the conventional two-level inverters. In addition, two-level inverters are exposed to thermal stresses created by converting the full voltage imposed by the continuous source, so the performance and lifetime of its components are actually affected whereas using the limitation of voltage, multilevel inverters reduce such stresses by splitting continues tension introduced to the inverter. To reduce this kind of problem researchers are in the hunt of new kind of architectures and switching techniques. In this scenario, a new switching technique is evolved and it's quite promising when compared with traditional techniques. There are two pulses with modulation techniques used to control multilevel inverters the first depends on fundamental switching frequency and the other depends on high switching frequency. Multilevel inverter has drawn tremendous interest in high power applications because it has many advantages: it can realize high voltage and high power output through the use of semiconductor switches without use of transformer and without dynamic voltage balance circuits. When the number of output levels increases, harmonics of the output voltage and current as well as Electro Magnetic Interference (EMI) decrease. The Multi-Level Inverter using cascaded-inverter with separate DC sources (SDCSs) synthesizes a desired voltage from several independent sources of dc voltages, which may be obtained from batteries, fuel cells, or solar cells. This configuration recently becomes very popular in ac power supply. This new inverter can avoid extra clamping diodes or voltage balancing capacitors. The ac output of each of the different level of full-bridge inverters are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. In this topology, the number of output phase voltage levels is defined by m = 2s+1, where s is the number of dc sources. A 5-level cascaded-inverters based inverter, for example, will have two SDCSs and three full-bridge cells. Minimum harmonic distortion can be obtained by controlling the conducting angles at different inverter levels. For a three-phase system, the output voltage of the three cascaded inverters can be connected in either Wye or Delta configuration. Multilevel inverter can be defined as a device that is capable to produce a stepped waveform.

Sinusoidal pulse width modulation (SPWM) is simple, easy to implement and widely used. In this paper, multiple multi-carrier SPWM methods for cascaded h-bridge are simulated, analyzed and compared with the conventional SPWM technique. These carriers are being implemented with different sinusoidal dispositions PDPWM, PODPWM and APODPWM.

II. Related Work

2.1: Multilevel Inverter

A multilevel inverter is a power electronic device which is capable of providing desired alternating voltage level at the output using multiple lower-level DC voltages as an input. Mostly a two-level inverter is used in order to generate the AC voltage from DC voltage. First of all, one can ask the following question: if there is a two-level inverter, then why use multilevel? To explain this, find out what this concept means, First take the case of a two-level inverter. A two-level Inverter creates two different voltages for the load i.e. suppose we are providing Vdc as an input to a two-level inverter then it will provide + Vdc/2 and – Vdc/2 on output. In order to build an AC voltage, these two newly generated voltages are usually switched. For switching mostly PWM is used as shown in the Figure 2.1, reference wave is shown in dashed blue line. Although this method of creating AC is effective but it has few drawbacks as it creates harmonic distortions in the output voltage and also has a high dv/dt as compared to that of a multilevel inverter. Normally this method works but in few applications it creates problems particularly those where low distortion in the output voltage is required.

2.2: Diode-Clamped (Neutral-Point Clamped) Multi-Level Inverter (NPC)

"The diode-clamped inverter, also called neutral-point clamped (NPC) or three-level inverter, obtains multiple voltage levels by connecting several power semiconductor devices, usually IGBTs or MOSFETs, together in a unique configuration. It utilizes clamping diodes and capacitor voltage sources to create multiple voltage levels at the output. The main advantage of the NPC inverter is its ability to generate more voltage levels than the number of DC voltage sources used, resulting in lower harmonic distortion and better waveform quality. However, it requires a high number of semiconductor switches and has limited scalability for higher voltage applications.

2.3: Flying Capacitor Multi-Level Inverter

Flying capacitor inverters utilize capacitors as voltage sources, arranged in a specific configuration to achieve multiple voltage levels at the output. The voltage levels are generated by dynamically charging and discharging the capacitors in a sequential manner. Flying capacitor inverters provide good waveform quality and reduced harmonic distortion. They require careful control algorithms to ensure proper balancing of the capacitor voltages, which can be a challenge in practice. Flying capacitor inverters are suitable for medium-voltage applications and offer better efficiency compared to diode-clamped inverters.

2.4: Modular Multi-Level Inverters

Modular Multi-Level Inverters (MLIs) are a type of multi-level inverter topology that offers scalability, fault tolerance, and ease of maintenance by utilizing multiple identical power electronic modules connected in parallel and series configurations. Unlike conventional multi-leveled control strategies, which produce levels of voltage with a semi-conductor switch's fixed arrangement, modular inverters have options for adding or replacing any new modules that may be required depending on the voltage levels.

III. Implementation of the Project

The cascaded multilevel H-bridge inverter is a power inverter utilized in various applications, including renewable energy systems, motor drive, and high-voltage power supplies. The inverter is intended to generate output voltage of high quality while minimizing harmonics and switching losses, unlike the traditional inverters. The following is the methodology employed in such inverters:

Sinusoidal PWM Analysis: As for the analysis of sinusoidal pulse width modulation, it is the simplest process that can be applied to the control of multilevel inverters. At the core, at a low frequency, the sinusoidal signal is continuously compared with

a high frequency. If the pulsation's value is greater than the values of the carrier, then the devices corresponding to it will be active. If the value of the pulsation is less than the values of the carrier, the devices corresponding to it will be inactive.

***3.1: PWM Dispositions*:** There are different categories of sinusoidal pulse width Modulation technique such as Phase disposition, Phase opposite disposition and Alternative phase opposite disposition

***3.1.1: Phase Disposition (PD)*:** Phase disposition PWM is the most used method because it gives the lowest harmonic distortion compared to the other two. In the PD PWM carriers are in the same phase Figure.

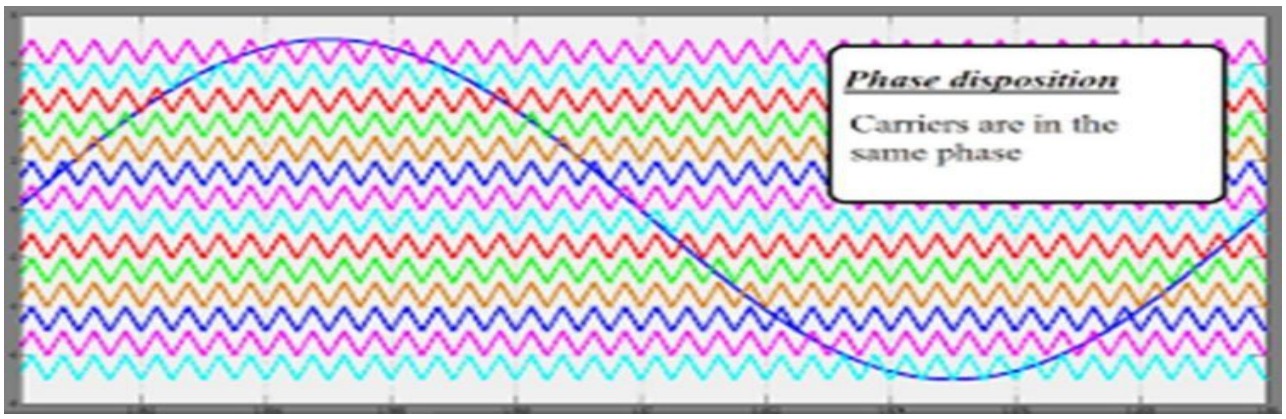

Fig-1: Carriers arrangement for phase disposition PWM

***3.1.2: Phase Opposite Disposition: (POD)*:** The difference between POD and PD techniques is that carriers above zero are 180° phase shifted with those below the zero.

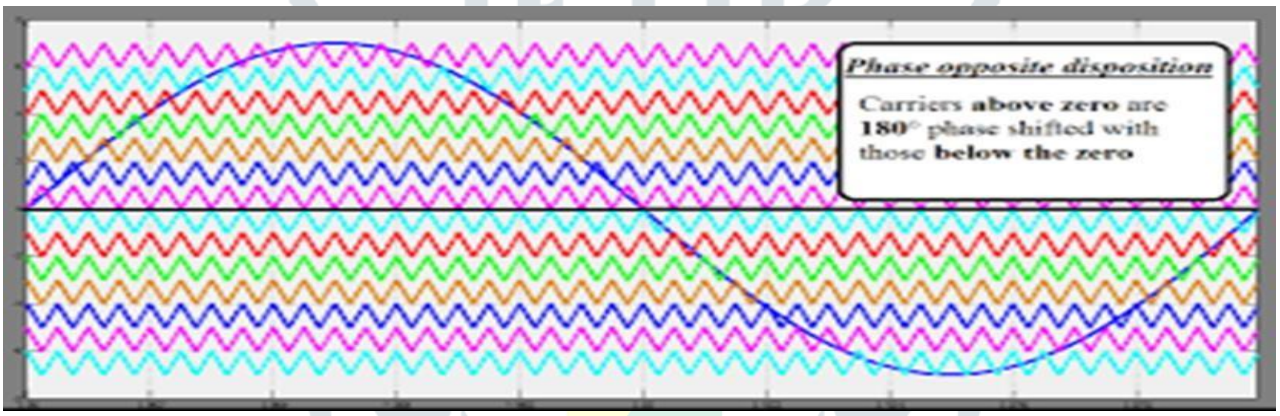

Fig-2: Carrier arrangement for phase opposite disposition PWM

***3.1.3: Alternative Phase Opposite Disposition (APOD)*:** This method of modulation is quite different from the two above in which the carriers are alternately phase shifted.

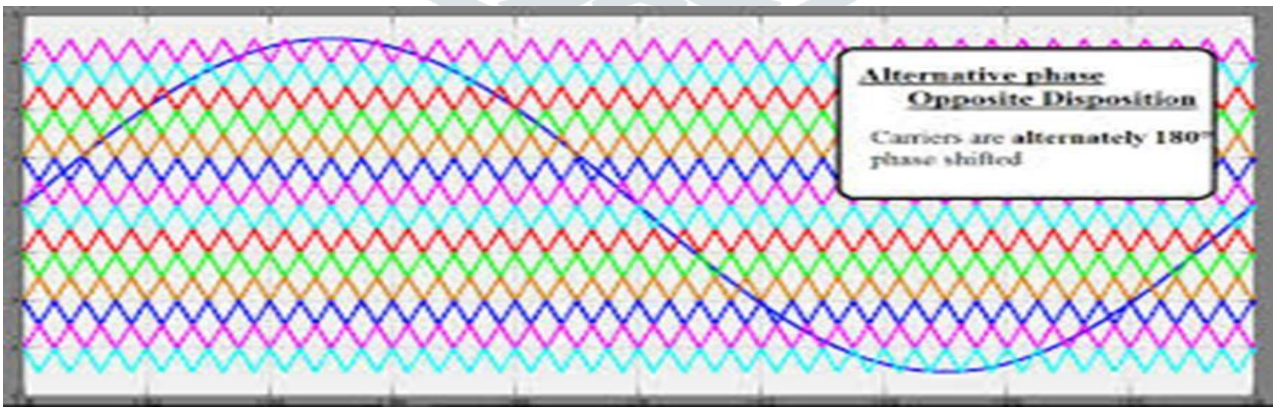

Fig-3: Carrier arrangement for Alternative phase opposite disposition PWM

IV. CIRCUIT DIAGRAM

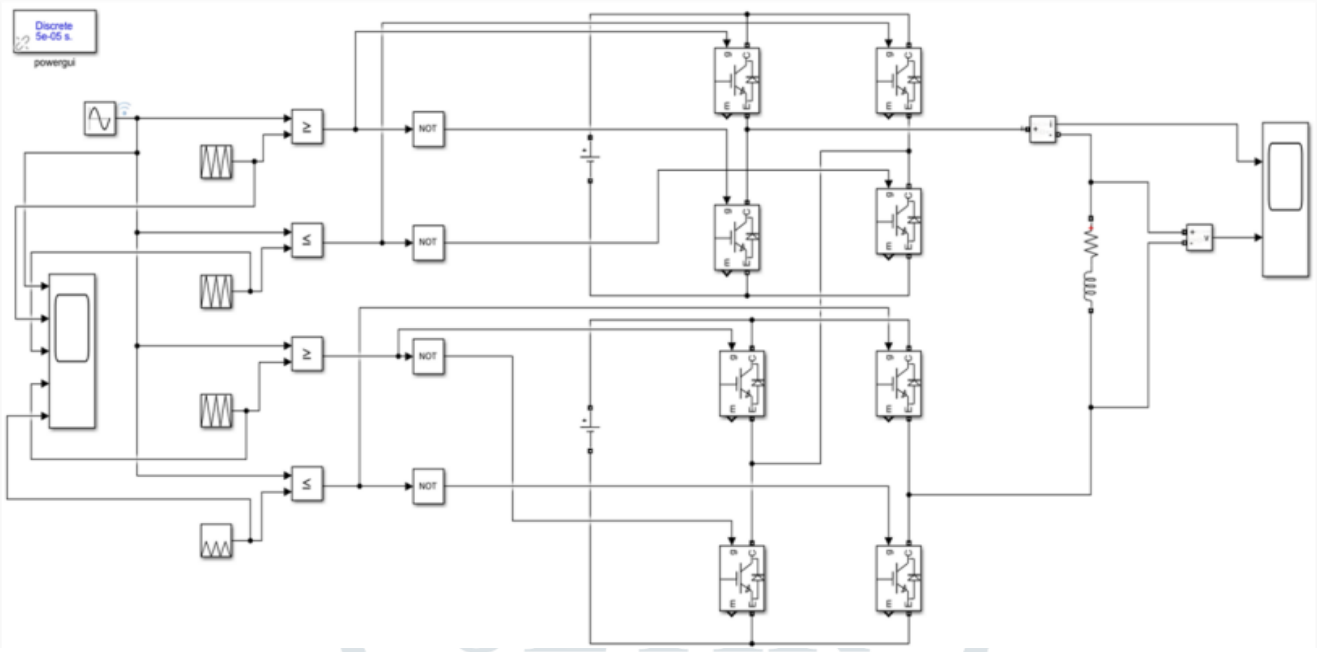

Fig-4: Matlab circuit diagram

V. RESULT AND DISCUSSION

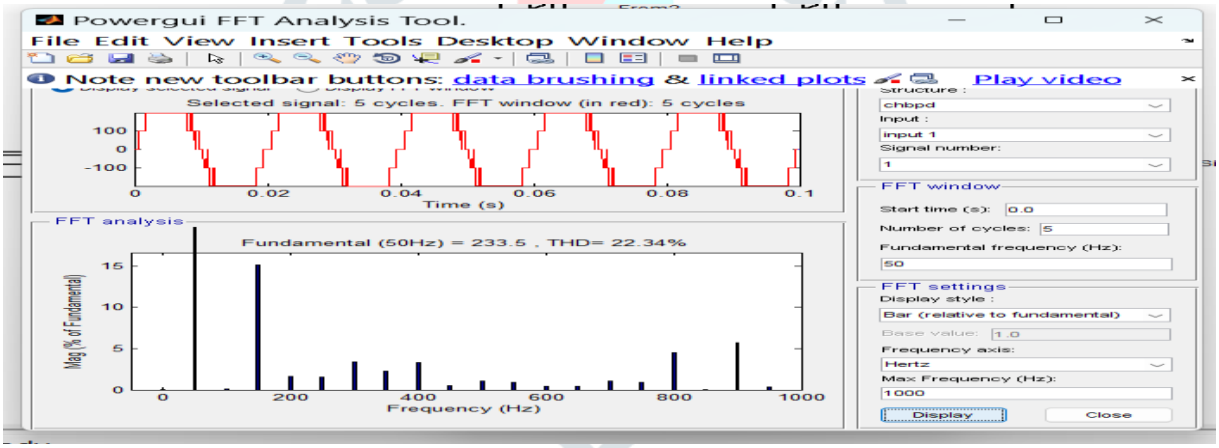

Fig-5: THD analysis of PD technique

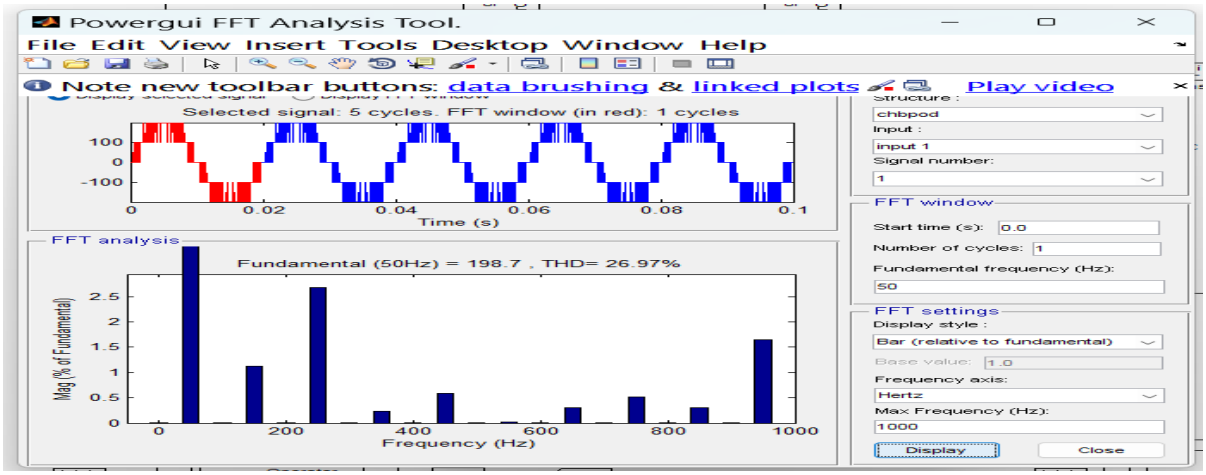

Fig-6: THD analysis of POD technique

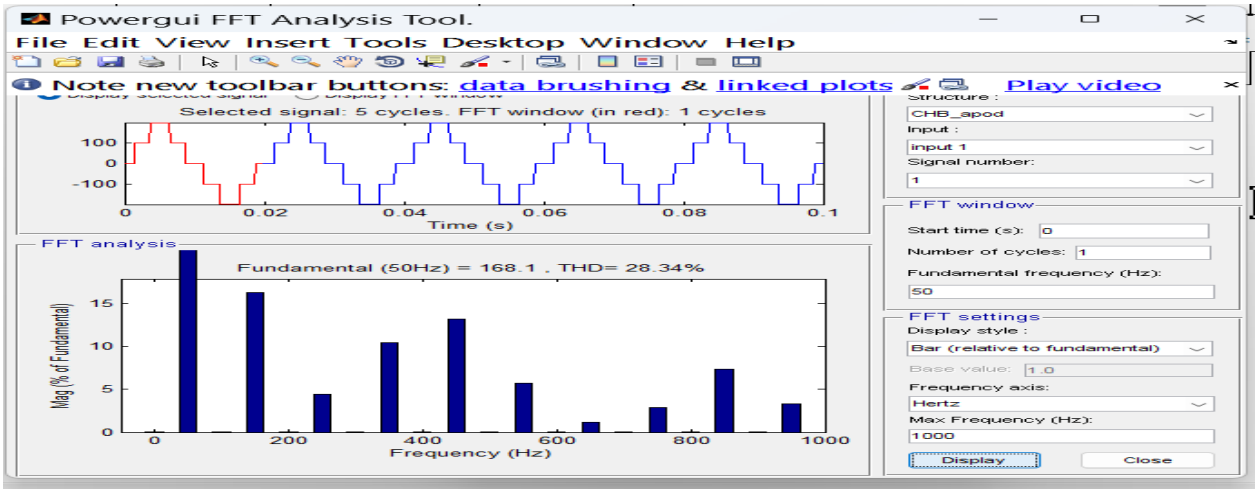

Fig-7: THD analysis of APOD technique

PWM TECHNIQUE	THD CONTENT IN %
PHASE DISPOSITION	22.34
PHASE OPPOSITION DISPOSITION	26.97
ALTERNATIVE PHASE OPPOSITION DISPOSITION	28.34

Fig-8: Comparison of THD values of PD, POD, APOD.

VI. CONCLUSION

From the simulation study conducted, several distinct features of the single-phase 5-level CHMI with PD POD and APOD scheme from the aspect of voltage can be identified. From the analysis, it can also be concluded that, in contrary to the conventional single-phase inverter, there is benefit in the harmonic performance by applying PD POD and APOD techniques to the 5-level CHMI. The PD scheme has advantages in applications due to the cancellation of the main carrier component between phase legs when the line voltages are formed. At high modulation index, the PD modulation strategy introduces the lowest line voltage THD. As a conclusion, the results suggested that the single-phase CHMI is most suitable to operate with PD technique promises a higher fundamental output voltage, and also lower significant harmonics. Among the three techniques it can conclude that the Phase Disposition Topology is better. Simulation results show that when we increase the number harmonics content will be reduced.

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