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POWER REDUCTION OF DIGITAL-BASED ANALOG AMPLIFIERS USING CMOS TECHNIQUES

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Abstract: A low-power CMOS dynamic OP-AMP is proposed for high frequency applications. Analog – digital converters (ADCs) are the converter electronic circuits which converts continuous signals into digital signals (binary data) for analyzing, estimation and transmission of signals. Device like transceiver uses an ADC in receiver part for converting a signal to digital form. However, high frequency applications like millimeter wave applications ADC consumes more power due to high frequency range. Therefore, a new adaptive power control dynamic (clocked regenerative) OP-AMP architecture is proposed with low power and high-speed performance for analog to digital converters. A low-power CMOS OP-AMP has been designed with optimized speed with total power of 30.25µW with supply voltage of 1V for ADC. The circuit is designed and simulated with 0.90µm CMOS technology.

1. Introduction

By nature, signals in environment domains are analog. For better perception these analog voltages are changed into digital signals. The converters like analog to digital converters (ADC) and digital to analog converters (DAC) act as overpass between the analog and digital world. Millimeter wave is an emerging technology for 5G communication; it uses a spectrum from 30 GHz to 300 GHz. ADC makes an effective role in communication purposes for mm-Wave transceivers to digitalize the signal. Even though, ADC is a baseband circuit still it dominates the overall power consumption of RF chain [1]. Countless and continuous investigation efforts are being taken in the field of high speed and low power ADCs [2]. As per the development in the process technology occurs, with the aid of minimized feature size; power consumption minimization can be attained. OP-AMP is a major building block of ADC [3]. Operating speed, gain, consumption of power, resolution and the offset are significant parameters of OP-AMP design, which has a substantial influence on the performance of the desired application. The symbolic representation of a OP-AMP is shown in Fig.1 (a). The essential objective of OP-AMP is to equate an input signal (VIN) with a reference signal (VREF) and to yield the output high or low based on whether the input is larger or lesser than reference voltage. Hence, it can be assumed as a decision circuit to select the binary value depending upon the value of input signal and reference signal.

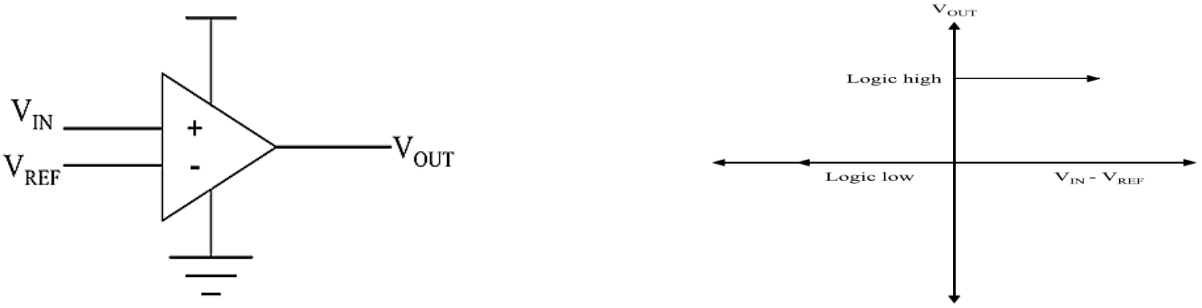

Fig.1. (a) Basic OP-AMP block diagram **(b) Ideal OP-AMP transfer characteristics**

The transfer characteristic of an ideal OP-AMP is illustrated in Fig.1 (b). The transfer characteristics of ideal OP-AMP is, if VIN > VREF, then V_{out} will be logic high and if VIN < VREF, then VOUT will be logic low. If the value of a reference signal is higher than the input signal, the OP-AMP will generate logic low signal at output (V_{OUT}) and if it is below, then the generated output is logic high.

Depends on the characteristics, OP-AMPs are classified into static and dynamic [4]. Earlier, static OP-AMPs were used for converters, but static OP-AMP has limited speed and consumes more power [4, 5]. In [4], therefore dynamic OP-AMP is preferred for high speed and also for zero static power dissipation. Dynamic OP-AMP will be in idle when it is in off state, so no static current

is consumed [6]. Comparison of input voltage is obtained after when the input differential voltage signal is amplified by pre amplifier stage to a valuable extent in dynamic OP-AMPs [7]. The first stage of the OP-AMP is a pre-amplifier stage, which consumes more power in whole ADC [8]. In order to achieve low power consumption in dynamic OP-AMPs, current bias can be replaced by clock controlled transistor that does not consume static power [9]. In another design [10], Positive feedback latch circuit is designed in the OP-AMP will considerably increases the area and size of the transistor and generates the kickback noise. Reduction in size of transistors results in reduced offset voltage [11]. A current mirror is used in double tail OP-AMP to reduce the kickback noise and for high speed, but power consumption is typically increased in this method [12]. Other double tail OP-AMP which reduces the power consumption and offset voltage but put up with huge kickback noise because input voltage transistors are connected directly to nodes of a latch with differential swing [13]. For low voltage converters, OP-AMPs with forward body bias scheme and dynamic offset cancellation techniques are used [14, 15]. Low resolution converters [16], the OP-AMP with clock signals is proposed with reduced power consumption. Various dynamic OP-AMPs are also employed in circuits depends on the application, but few common dynamic OP-AMPs has some limitations like power dissipation, delay, moreover OP-AMP [17] has noise and similarly [18-23], does not optimize for better performance parameter.

In this paper, an efficient OP-AMP is proposed with high speed performance and reduced power consumption for mm-Wave transceiver application. Moreover, the proposed method is compared with conventional OP-AMPs for parameters like power consumption, offset voltage and delay. In fact, the OP-AMP gives effective results than the existing designs.

2. Existing OP-AMP Designs

To fulfill the requirements like high processing speed and reduced power in OP-AMPs, a positive feedback dynamic OP-AMP is preferred [17]. Although many diverse architectures of dynamic OP-AMP are present in the literature, a comparison of the main state of art architectures in terms of speed (delay), offset, power, resolution is made in this section. The OP-AMPs published in recent time still operate with sampling rate inferior than the anticipated future requisite in CMOS technology with relatively high power consumption. To meet the necessity of high speed the dynamic OP-AMP is extensively used.

Generally OP-AMP operates in two phases, reset phase and evaluation phase. In reset phase, the output nodes are discharged and in evaluation phase, the comparisons between the input voltages are occurred and the comparison output is displayed at the output nodes of pre-amplifier stage. In [17], double tail dynamic OP-AMP (DC) as opposed to using the same clock which swings from VSS to VDD, a matching phase measured voltage quality swing is used. The main advantages of this circuit are high precision, low offset. However, it cannot operate beyond frequency of Megahertz range. In [18], dynamic OP-AMP (DC) the OP-AMP is a double period architecture which takes the advantage regarding cascading of pre-amplifier stage in addition to the usual latch stage. Important point of this structure will be a significant reduced input offset voltage quality without a major penalty on strength and area. The latch circuit is varied from the particular pre-amplifier stage in addition to each stage and works independently with the various clock phases. But delay due to clock pulses in considerably high. The differential dynamic OP-AMP (DDC) offers low kickback noise that reduces the clock load and removes the prerequisite of highly accurate clock timing over the wide range of the supply and common-mode voltage with reduced offset voltage plus high speed [19]. Due to double tail architecture the pre-latch stage consumes more static power which leads to more power consumption. Similarly in [20], in dynamic logic based OP-AMP (DLC) evaluation phase the two stages operate asynchronously. Due to the huge mismatch occurs in latch that leads to increase in power consumption for fast amplification.

By considering the above limitations like less frequency range, high latency and more power dissipation of existing OP-AMP designs [17-20], a new architecture is proposed. This paper follows with the proposed OP-AMP which is presented with power analysis. In Section 4 the results are shown which followed by Section 5 conclusion of the work.

3. Proposed OP-AMP

A new design of a OP-AMP is proposed to strike a balance between speed, offset and power. Fig.3 shows the proposed OP-AMP design. The major aim of the structure is to decrease the power consumption and delay and increase the latch generation speed as compared to the existing structures of OP-AMPs. The circuit where the input signals are applied is called pre-amplifier circuit. In the Fig.3 the transistors M9, M12 MC1, MC2, M10, M11, MSW1, MSW2 and M tail forms the pre-amplifier circuit. Similarly the circuit which generates output is called regeneration circuit. The regeneration circuit comprises of transistors M1, M2, M3, M4, M5, M6, M7 and M8. The operation of the design is explained as follows:

During pre-charge (reset) phase when clk=0, the pMOS transistor M9 and M12 are switched on and these pMOS transistor pull nodes fp and fn to VDD. This makes nMOS transistors MSW1 and MSW2 to switch on. So, the voltage starts flow to ground, but the clk is low in the Mtail transistor that prevents the discharge of the voltage to ground. The pMOS transistors MC1 and MC2 are off which makes the pMOS transistor M1 and M2 to off and the nMOS transistors M5 and M6 are made on to discharge the outputs to ground.

During regeneration phase when clk=VDD, the pMOS transistors M9 and M12 are switched off. The input signal is given to the circuit, the nodes fp and fn starts to discharge from VDD to ground in proportion to the input magnitude. If fn is low, the transistor M2 will turn on and the corresponding output will be generated. Similarly if fp is low, the transistor M1 will turns on and the output is produced respectively. If one of the node (fp and fn) voltage falls down that will able to turn on MC1 and MC2 transistors to the corresponding nodes and it will charged to VDD.

The drive current is reduced to fifty percent of the current in comparison to previous design as it was divided into M1 and M2 transistors. The pre-amplifier stage need not to be in active state throughout the amplification process. And also, in the control transistors (MC1 & MC2) when either one turns on, the current from VDD starts to drawn to ground through input terminals which results in static power consumption. To overcome that, two nMOS switches are added below the input terminals. Therefore, the proposed design is able to reduce the power consumption of the OP-AMP in ADC.

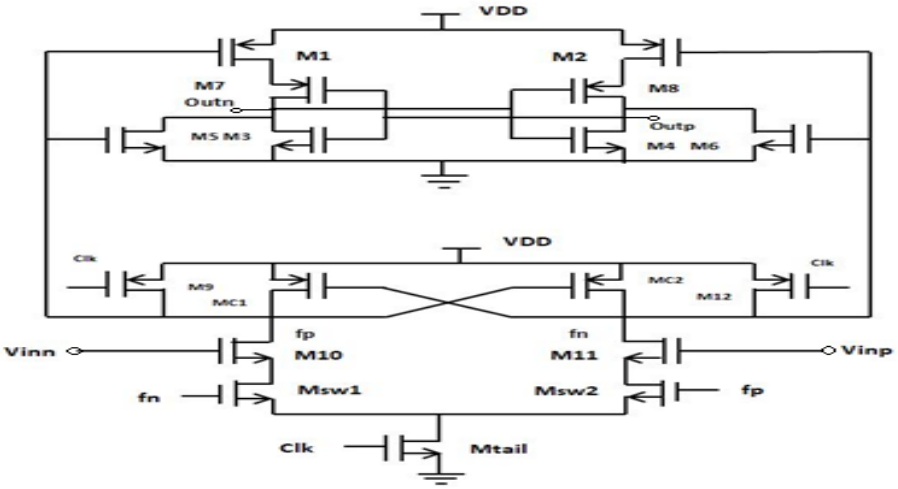

Fig.3. Proposed OP-AMP

Analytical analysis

Power estimation of OP-AMP is derived by various methods. The methods are derived for non-linear time variant and linear periodically time variant systems to estimate the power [24]. All the dynamic OP-AMPs are linear periodically time variant systems in practical [25]. The analytical power expression is presented by time variant model of transistors which is operated in regeneration phase of the OP-AMP. Therefore, the average power for one cycle of comparison is

$$P_{avg} = \frac{1}{t_{clk}} \int_{t0}^{tp} V_{DD}.I_D \, dt \qquad \textbf{(1)}$$

where, t_{clk} is the total time period of OP-AMP, I_D is the current drawn from the supply voltage to the circuit. Integration is performed in the limit from (t_0) is the start of regeneration phase to (t_p) the end of regeneration phase. According to [24] & Tsividis's [26] Operation & Modeling of the MOS transistor, the drain current expression for MOSFET is

$$I_D = I_Z \left[\left[ln\left(1 + e^{\left(\frac{V_{GS}-V_T}{2n\emptyset_t}\right)}\right)\right]^2 - \left[ln\left(1 + e^{\left(\frac{V_{GS}-V_T-nV_{DS}}{2n\emptyset_t}\right)}\right)\right]^2 \right] \qquad \textbf{(2)}$$

Where

$\emptyset_t$ = thermal voltage

$$I_z = 2\mu.C_{ox}.\frac{W}{L}.n.\emptyset_t^2 \qquad \textbf{(3)}$$

In this, C_{ox} is the total oxide capacitance, n is free electron concentration, W, L are the width and length of the channel. For the proposed OP-AMP, the transistor M7 draws current for a short period of time the by applying the equation (2) & (3) in (1),

$$P_{avg} = \frac{1}{t_{clk}} V_{DD}.I_{Z7} \int_{t0}^{tp} \left[\left[ln\left(1 + e^{\frac{(V_{DD}-|V_{fp}|-V_{outn}(t)-|V_{th}|)}{2n\emptyset_t}}\right)\right]^2 - \left[ln\left(1 + e^{\frac{\left((V_{DD}-|V_{fp}|-V_{outn}(t)-|V_{th}|)-n\left(V_{DD}-|V_{fp}|-V_{outp}(t)\right)\right)}{2n\emptyset_t}}\right)\right]^2 \right] dt \qquad \textbf{(4)}$$

By using the approximation, $\ln(1+x) \approx x$ for $|x| \ll 1$. Then, the expression further simplified by $(\ln e^y)^2 = y^2$ for $e^y \gg 1$. Therefore, the equation (4) will be,

$$P_{avg} = \frac{1}{t_{clk}}.V_{DD}.I_{Z7} \int_{to}^{tp} \left[\left(\frac{(V_{DD}-|V_{fp}|-V_{outn}(t)-|V_{th}|)}{2n\emptyset_t}\right)^2 - \left(\frac{\left(V_{DD}-|V_{fp}|-V_{outn}(t)-|V_{th}|-n\left(V_{DD}-|V_{fp}|-V_{outp}(t)\right)\right)}{2n\emptyset_t}\right)^2 \right] dt \qquad \textbf{(5)}$$

Therefore from equation (5), the process carried out for simplifying the expression by applying algebra and further calculations it becomes

$$P_{avg} = \frac{1}{t_{clk}}.V_{DD}.\ I_{Z7} \int_{t0}^{tp} \left[\frac{\left(2(V_{DD}-|V_{fp}|-V_{outn}(t)-|V_{th}|)-n\left(V_{DD}-|V_{fp}|-V_{outp}(t)\right)\right).\left(V_{DD}-|V_{fp}|-V_{outp}(t)\right)}{4n.\emptyset_t^2} \right] dt \qquad \textbf{(6)}$$

Where, V_{outp} is the discharge output that carries out with the expression with this design circuit in that σ is the ratio between the trans-conductance in the latch to the output load capacitance.

$$V_{outp} = \left(V_{DD} - |V_{fp}| - |V_{th}|\right)e^{\left(\frac{-(t-t_0)}{\sigma}\right)} \qquad \textbf{(7)}$$

Substituting the discharge output values in the equation (6), V_{outn} is not discharged enough. The final expression will be obtained with some analytical assumption by simplifying and applying the integral in equation (7), and taking the large value as constant to make more comprehensible.

$$P_{avg} = \frac{1}{t_{clk}}\frac{V_{DD}.I_{Z7}}{8n\emptyset_t^2}.\sigma.|V_{th}||V_{fp}|\left(2k - n\left(\left(2|V_{fp}|\right) - |V_{th}|\right)\right) + |V_{th}|\left(2k.e^{\left(\frac{-2(t_p-t_0)}{\sigma}\right)} + n\left(\left(2|V_{fp}|\right) - |V_{th}|\right).e^{\left(\frac{-2(t_p-t_0)}{\sigma}\right)}\right) -$$

$$-4k.e^{\left(\frac{-(t_p-t_0)}{\sigma}\right)}|V_{th}| \quad \textbf{(8)}$$

Further the equation (8) is simplified to obtain the expression for power consumption

$$P_{avg} = \frac{1}{t_{clk}}\frac{V_{DD}.I_{Z7}}{8n\emptyset_t^2}.\sigma.|V_{th}||V_{fp}|\left(2k - n\left((2|V_{fp}|) - |V_{th}|\right)\right) + |V_{th}|\left(2k + n\left((2|V_{fp}|) - |V_{th}|\right)\right).e^{\left(\frac{-2(t_p-t_0)}{\sigma}\right)} - -4k.e^{\left(\frac{-(t_p-t_0)}{\sigma}\right)}|V_{th}| \quad \textbf{(9)}$$

From equation (8), it is concluded that power consumption parameters are influenced by clock time, supply voltage, comparison time domain and transistor size. Depends on the transistor size the parameters of the power consumption may vary. The power delay product of the OP-AMP can also be calculated by

$$PDP = P_{avg} \times delay\ time \quad \textbf{(10)}$$

This expression is derived when transistor M7 draws current during a period of time when the OP-AMP operates in regeneration phase. If pMOS transistor M1 is on, the current draws to M7 to generate the output with respect to the input signal. The difference of the node voltage and threshold voltage in the above expression shows that power consumption is reduced in the proposed OP-AMP. The node voltage in the pMOS transistor M1 is deducted from the threshold voltage of the pMOS transistor M7 will give the reduced power consumption in analytical analysis of the OP-AMP circuit. This power consumption expression is derived for the one cycle of comparison, depends on the input voltages the value for the expression varied.

4. Simulation results

Without sacrificing speed, the power contraction is usually the prime focus of the current dynamic OP-AMPs. In this session, the simulated result of proposed OP-AMP is presented. This OP-AMP is operated for high speed ADCs in mm-Wave application. By resizing the transistor size, the better performance is obtained in the proposed OP-AMP. Moreover, this is not done here to see the effect of the OP-AMP. The challenging requirement of the region and power-efficient high speed ADC drive to the analysis and procedure associated with fully dynamic OP-AMP in order to improves power, region, and improves the speed.

The post-layout simulations have been done for proposed OP-AMP. Fig.5. displays the chip layout of proposed OP-AMP which uses an area of 6.9×7.8 μm^2. Depending on the number of transistors and it's routing, the area was calculated with the tool cadence. Fig.6 (a) & (b) shows the post-layout simulation results for transient response that converts the analog signal to digital signal. One of the important specifications is common-mode voltage in OP-AMP. Minimum changes in common-mode voltage will influence the delay and power of the OP-AMP. The power and offset voltage comparison further discussed in this chapter. In the proposed method, the tail current is reduced in the pre-amplifier stage which boost-up the gain of the latch, thus results in reduced offset voltage. The switches that implemented below the input transistors will reduce the static current of the circuit, that leads to reduce in overall power consumption of the circuit.

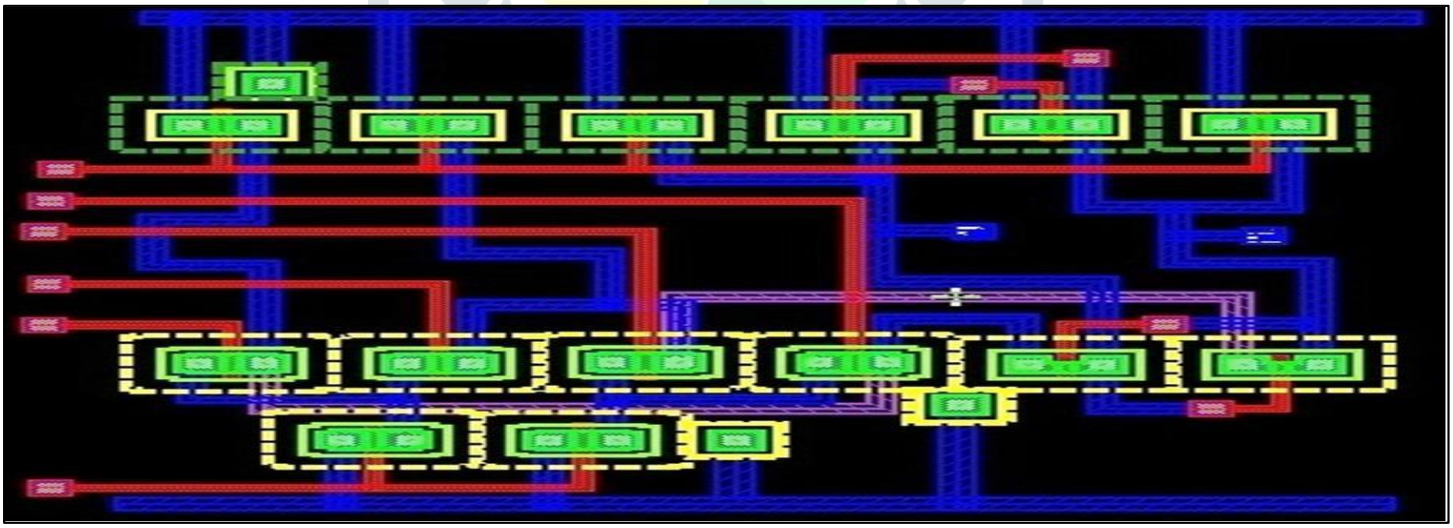

Fig.5. Layout of proposed OP-AMP

Fig.6 shows the transient response of the OP-AMP for given input voltages, in which Fig.6 (a) is for the input voltage where Vinp is greater than Vinn, so fn is discharged and pMOS transistor switch on which produced the output Outp. Similarly Fig.6 (b) is for the input voltage where Vinn is greater, so output Outn is produced. Thus the OP-AMP produces the output based on the input signal with reduce power consumption and offset is shown in this chapter. The power consumption of the OP-AMP varies depends on the supply voltage.

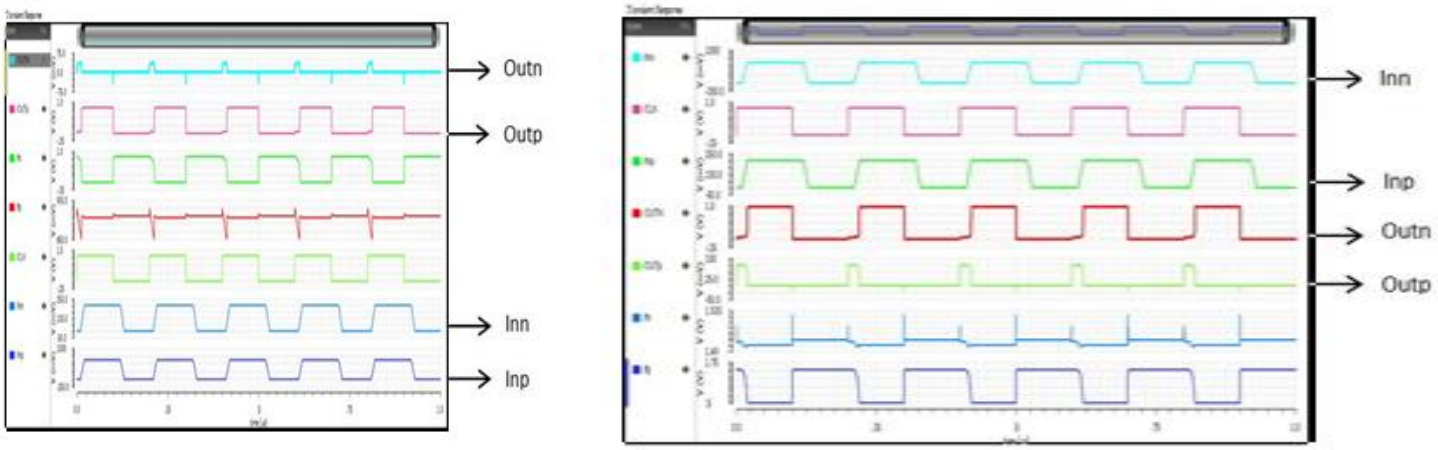

Fig. 6. (a) Transient response of OP-AMP when Vinp>Vinn (b) Transient response of OP-AMP when Vinp<Vinn

Fig.6 shows the transient response of the OP-AMP for given input voltages, in which Fig.6 (a) is for the input voltage where Vinp is greater than Vinn, so fn is discharged and pMOS transistor switch on which produced the output Outp. Similarly Fig.6 (b) is for the input voltage where Vinn is greater, so output Out is produced. Thus the OP-AMP produces the output based on the input signal with reduce power consumption and offset is shown in this chapter. The power consumption of the OP-AMP varies depends on the supply voltage

The below fig. 7, 8 & 9 illustrates the comparisons of various performance parameters of OP-AMPs with simulated results. The overall reduction in static power consumption that gives less power dissipation with varying V_{cm}'s that shown in Fig. 8. In general, in dynamic tail OP-AMPs delay does not have much variation with common-mode voltages. It is observed that the power dissipation starts driving lower with common mode voltage to the conventional OP-AMPs. The purpose of the proposed OP-AMP is to minimize the power reduction that is comparatively measured in the simulated results of power shown in Fig. 7. Fig.8 shows, the offset voltage is conventionally reduced and remains same in the range 1-1.2V of common mode voltage with supply voltage of 1V and offset voltage is not worsen due to power reduction in the pre-amplifier stage is shown by using Monte Carlo simulation in Fig. 9.

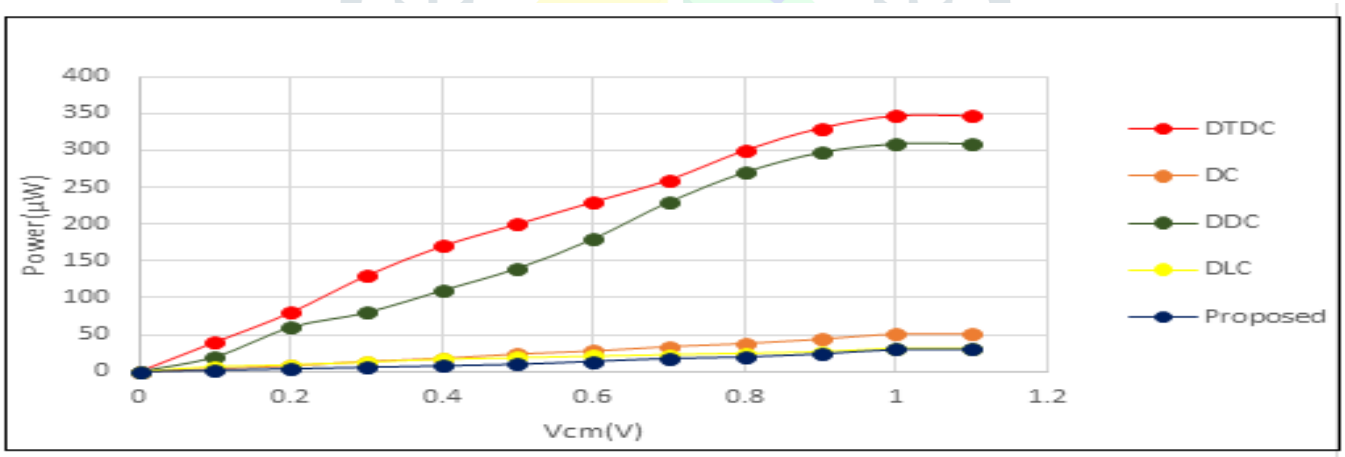

Fig.7. Parametric performance of power v/s. common mode voltage with v_{DD}=1V

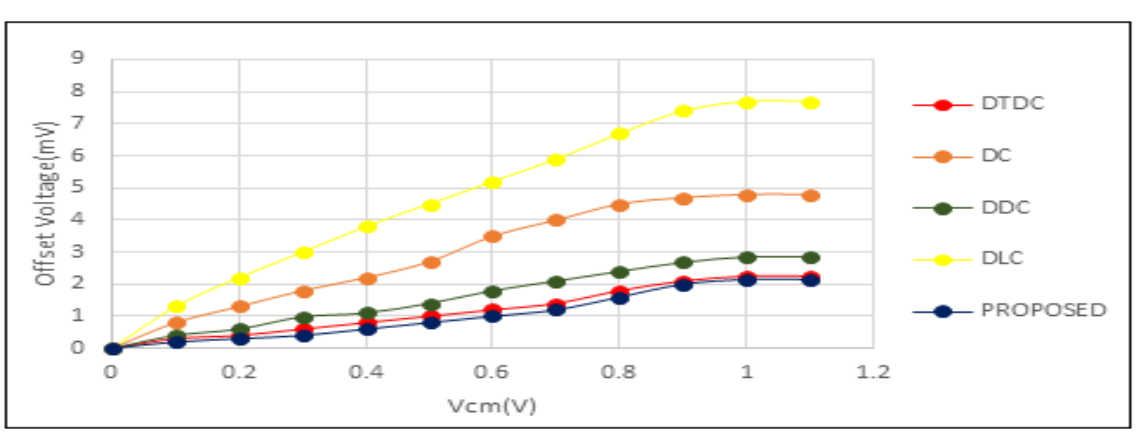

Fig.8. Parametric performance of offset v/s. common mode voltage with v_{DD}=1V

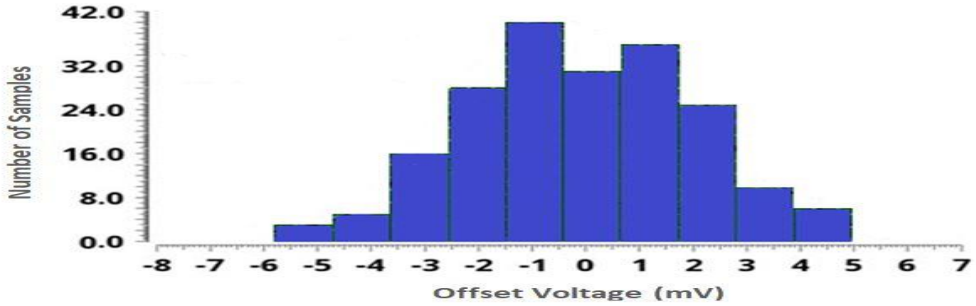

Fig.9. Monte Carlo histogram of Offset Voltage

Due to the reduction of current in pre-amplifier, the delay degradation takes place in the OP-AMP. Generally the delay in the dynamic tail OP-AMP is less influenced by the change in common mode voltage, which has a broad common mode range. Even the size of the transistor also makes variations in the delay of the OP-AMP.

In this section, the simulations are shown to uphold that proposed OP-AMP that gives the effective results. The transistor size also a major cause for the power reduction. To get good perception Table.1 illustrates the performance comparison of simulation layout results for various performance parameters including layout area.

Parameters	**OP-AMP-1 DTDC [17]**	**OP-AMP-2 DC [18]**	**OP-AMP-3 DDC [19]**	**OP-AMP-4 DLC [20]**	**Proposed OP-AMP**
Technology	180nm	90nm	180nm	90nm	90nm
Number of transistors	15	11	16	13	17
Delay(ps)	220	152	230	50	110
Offset(mV)	2.2	4.8	2.85	7.7	2.15
Gain(dB)	33.85	33.81	29.26	30.27	31.96
Power (µW)	347.04	51.00	309.82	31.86	30.25
Area(µm x µm)	16.5 x 22.1	3.3 x 3.3	6.4 x 7.3	7.2 x 8.1	6.9×7.8

Table.1. Performance Comparison of OP-AMPs

From table.1 it is observed that the power and offset voltage of the proposed OP-AMP is comparatively low. The OP-AMPs were designed in 90nm CMOS technology with 1GHz sampling frequency with supply voltage of 1V. The area of the OP-AMP is estimated based on the size of the transistors and number of nodes.

CONCLUSION:

The new propose dynamic OP-AMP is presented to reduce power consumption. The design is easy to implement, from the conventional OP-AMP a proposed OP-AMP can be designed by simple modification. Thus, a low-power CMOS OP-AMP has been designed with optimized speed with total power of 30.25µW with supply voltage of 1V for ADC. The circuit is designed and simulated with 0.90µm CMOS technology with estimated area of $6.9\times7.8\mu m^2$. The proposed OP-AMP is used in ADCs for mm-Wave communication applications with low power dissipation.

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