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DESIGN AND ANALYSIS OF POWER FACTOR CORRECTION TECHNIQUES FOR SINGLE PHASE CONVENTIONAL AND INTERLEAVED DOUBLE BOOST CONVERTERS

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Abstract : Diode Rectifiers are one of the most important circuits in small and medium scale power supplies where the intended power flow in unidirectional. The capacitor connected in parallel to the load of such power supplies often distort the AC input power leading to very high THD and low power quality which in turn reduces the input power factor. To improve this power factor, power converter interfaces are used and the duty cycle is so shaped that the entire power converter and load is seen as purely resistive, thereby reshaping the input current to sinusoidal and increase power factor to a value as high as one. Thus, in this paper, an In-detailed study on such power factor correction circuits (PFC) are presented with two power converters: Conventional Boost converter (CBC) and Interleaved Double - Boost converter (IDBC). The study the proceeds with development of steady state model and development of control loop. The control scheme involves two loops: faster inner current loop and slower outer voltage loop. The entire design of control loop is carried out using frequency response techniques such bode plots with emphasis on setting correct bandwidth and phase margins to ensure the controller speed and overshoots are within limits. Finally, the results from CBC and IDBCs are presented with emphasis on ensuring improved THD and power factor levels.

IndexTerms **-power factor correction, boost converter, Interleaved double boost converter, controller design.**

I.INTRODUCTION

Direct Current (DC) power supplies are essential components in various technological applications, providing a stable and controlled flow of electrical energy in a unidirectional manner. The importance of DC power supplies stems from their versatility, efficiency, and suitability for a wide range of electronic devices and systems. significance of DC power supplies and their diverse applications across different industries from toys till satellites. Diode rectifiers play a crucial role in power supplies, converting alternating current (AC) to direct current (DC) by allowing current flow unidirectional. This process is essential for providing a stable and usable power source for various electronic devices and systems. In diode rectifiers, filtering capacitors are commonly employed to smoothen the rectified output voltage, reducing the ripple and providing a more stable DC voltage. While capacitors are effective in reducing voltage ripple, they can contribute to an increase in Total Harmonic Distortion (THD) in the input current. This phenomenon is often associated with the charging and discharging behaviour of the capacitor in conjunction with the diode rectification process. To address the increase in THD due to filtering capacitors, designers should implement power factor correction (PFC) techniques or active filters. These strategies actively control the input current waveform to mitigate harmonic distortion and improve power quality.

Active Power Factor Correction (PFC) is a crucial approach employed in power supplies to enhance the power factor and efficiency of electrical systems. Active PFC circuits actively correct and adjust the power factor, typically aiming to achieve a near-unity power factor of 1. In Active PFC circuits, the feedback loop is a fundamental component that plays a crucial role in ensuring the power factor is corrected efficiently. The feedback loop continuously monitors the input voltage and current, providing information to control the switching devices in the PFC circuit. The objective of the PFC is to replace the capacitive filter with a power converter and make sure that the entire power converter and the load behaves as purely resistive when seen from the terminals of the diode rectifier bridge. To accomplish this task, the inductor current is shaped/aligned in exact shape with the voltage across the bridge rectifier and the resulting duty cycle is fed to the power converter switch. One of the problems with such Active PFC is the poor voltage regulation at load side due to very slow acting voltage loop. This in-turn causes ripples in the output voltage across the load. To mitigate this, an additional power converter is designed to achieve ripple-free fast regulated output. The feedback loop additionally provides the Active PFC circuit with dynamic response capabilities. It can quickly adapt to fluctuations in load conditions or variations in the input voltage, ensuring effective power factor correction under varying circumstances. The stability and reliability of the Active PFC system heavily rely on the effectiveness of the feedback loop.

Proper design and tuning of the feedback control ensure that the PFC circuit operates consistently and maintains the desired power factor correction across different operating conditions.

II. LITERATURE SURVEY

Active PFC, which involves controlling the line current with switching devices like as MOSFETs (metal oxide semiconductor field effect transistors) and IGBTs (insulated gate bipolar junction transistors), is a result of advancements in power semiconductor devices and microelectronics. MOSFETs are by far the most popular choice for PFC in low and medium power levels up to a few kilowatts (kW) due to their switching speed, ease of driving, and robustness. BJTs and, more recently, IGBTs are utilised for high voltage medium power applications that MOSFETs cannot handle due to their high on-state resistances.

In order to achieve good input current wave shaping using active approaches, the switching frequency typically needs to be at least an order of magnitude higher than 3 kHz (= 50 x 60 Hz = 50th harmonic of line frequency). This is now possible thanks to recent developments in MOSFETs and IGBTs.

The application of active PFC techniques provides one or more of the following benefits.
• In comparison to passive approaches, the input current has a lower harmonic content.
• The output filter capacitor's rms current rating has been reduced.
•A near-unity power factor (0.99) is achievable with Total Harmonic Distortion (THD) as low as 3-5%.
• For higher power levels, active PFC approaches outperform passive PFC techniques in terms of size, weight, and cost.

The sub-sections that follows present recent improvements in single phase active PFC techniques. In this survey, active PFC procedures are divided into two basic types.

(1) Poor load dynamics using active PFC approaches (2.1): These are referred to as "conventional active PFC techniques" in this research. They are often followed by a dc-dc downstream converter that meets the load's requirements.

(2) Techniques for active PFC with quick load dynamics : In this case, the PFC unit can fulfil the quick dynamic requirements of a typical load. Due to increased complexity and control schemes, discussions on such circuits is out of the scope of this paper.

2.1 Conventional Active PFC Techniques

There are basically two approaches here. A current-source-type circuit [1-5], in which the PFC functions as a current source feeding the load, is one way. The other method yields the well-known voltage-source-type circuits mentioned. Though voltage source circuits [6]-[9],[10]-[21],[22]-[47],[48] are more common, current source circuits are beneficial in some niche applications. Both kinds of circuits and schemes are addressed in the following subsections.

2.1.1 Topologies

The current-source PFC converters [1-5] are typically of the buck type. The voltage-source-type PFC converter, on the other hand, can use any of the fundamental dc to dc converter switching cells, such as buck, boost, buck-boost, and Cuk converter. The boost and buck-boost topologies are the most popular. The salient properties of these topologies (both current and voltage source types) and some essential difficulties associated to these topologies are presented in the following sub-sections.

2.1.1.1 Boost Topology

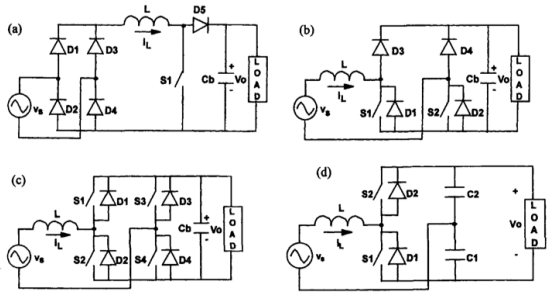

Figure 2.1: Different. Topologies in Boost PFC Topology. (a) Single Switch (b) Two Switch (c) Four switch (d) Half Bridge

Figure 2.1 depicts some of the most used boost circuits. Several aspects of the boost converter, including as the inductor's position on the input side (lower input current flow and EMI) and a dc voltage gain greater than unity, make it an obvious choice for active PFC applications [4]. The single-ended boost converter (figure 2.3a) is more popular due to the usage of a single active switch and the ease with which the switch can be driven. This converter can be operated in CCM [49], Boundary of CCM [50] and DCM [48]. This is a common option for medium and high-power applications. Because of the existence of the big boost input inductor, the supply tipple current due to switching is low in this case. As a result, the input filtering required is minimal. There is also an

isolated version of the boost PFC converter [51]. The following considerations should be considered while using the boost converter in CCM.

2.2.1.2 Buck-Boost or Flyback Topology

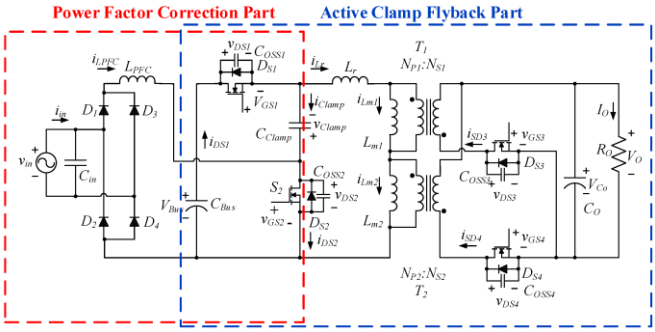

Fig 2.2: Flyback based PFC with active clamping Technique.

For low power applications, the flyback topology (figure 8) is appropriate.

(1) The boost topology's existing start-up inrush problem is not present here.
(2) When compared to the boost topology, the overload protection mechanism is straightforward.
(3) The output voltage can be higher or lower than the peak input voltage.
(4) Flyback topology simplifies the implementation of galvanic isolation between the input and output.

Flyback PFC converters [52][53] may operate in both CCM and DCM modes. However, the input current is cut in both modes, resulting in higher noise and EMI than with a comparable boost architecture. The DCM technique, on the other hand, eliminates the diode reverse recovery problem. The DCM operation of the flyback is popular due to its ease of control. If the switch duty cycle is maintained constant across one line half cycle [52], sinusoidal input current (after filtering the switching component) is generated automatically. A flyback topology, as depicted in figure 2.2, is used in [54, 55]. The switch (with its anti-parallel diode) and clamp capacitor Cc constitute an active snubber in this case.

2.2.1.3 Buck Topology

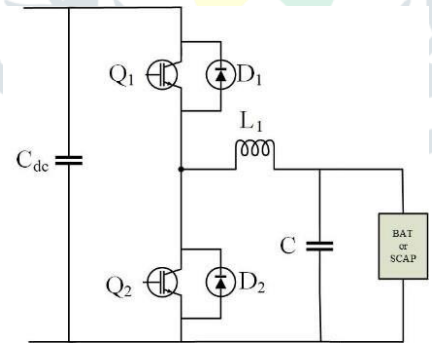

Fig 2.5: Circuit of Half Bridge Based Buck Converter

Buck topology - In voltage source type buck networks, the input voltage must be larger than the output voltage. As a result, when the input voltage is smaller than the output voltage, no current is pulled from the input; thus, the net input current is non-sinusoidal. The buck converter, on the other hand, has the advantage of being able to provide current limit support due to the series buck switch [48]. The input voltage varies across a large range (130 to 600 V) in the application described in [56]-[58], while the required output voltage is 400 V. As a result, the boost converter alone is unsuitable. To keep the input current sinusoidal, a topology with (Buck + Boost) operation is used. The buck operation is effective when the input voltage is larger than 400 V. The boost operation is carried out when the voltage falls below 400 V. Unlike the voltage-source-type buck converter, the current-source-type buck PFC converter draws a sinusoidal current for all input voltage values. To do this, the instantaneous output current must be kept higher than the instantaneous input current.

A three-phase buck converter that operates as a current-source type PFC converter is also described [59][60].It is also claimed that the notion can be applied to a single-phase instance. References [61]-[62] discuss the single-phase implementation in detail. [51] addresses a two-switch current source type PFC circuit (figure 2.5) based on the duality concept that was evolved from a half-bridge voltage source type PFC Converter [63],[64]. To provide bipolar blocking capability in these converters, a diode must be placed in series with the switch(es); this results in additional conduction power loss. The current-source buck PFC converter is

especially effective in applications where the output voltage must be decreased to low levels, such as dc motor control or an ac-dc rectifier with an overcurrent limit.

In view of the discussions, following are the objectives of the paper are:

1. To analyze the effect of capacitive filter on diode rectifier front-end and study its harmonic pattern.
2. To Design a Conventional Boost and Interleaved Double Boost based Power factor correction Circuits to reduce the AC current THDs so as to meet the grid standards.
3. To develop a control scheme and design the same using frequency response techniques to mitigate second harmonic ripple in the output.

III. DESIGN OF CONVENTIONAL AND IDBC PFC

In this section, design and analysis of active power factor correction for conventional and IDBC converters are presented in detail. The control loops are designed and discussed.

3.1 Design of Active CBC based Active PFC

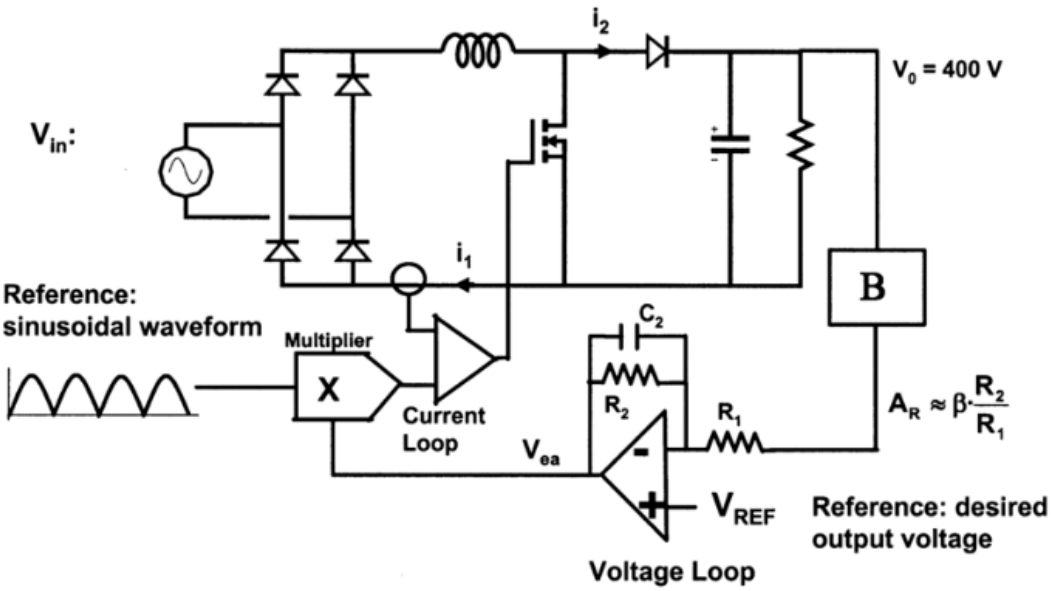

Figure 3.1 Schematic of CBC based PFC with control loop.

A conventional boost-based PFC is presented in Fig 3.1 along with its control scheme. The capacitive filter in a traditional rectifier system is replaced with a boost converter.

Here's a brief explanation of how a Boost PFC converter works:

1. Rectification Stage: The input AC voltage is first rectified to DC using a diode bridge. This converts the alternating current (AC) into a pulsating direct current (DC).
2. Boost Converter Stage: The DC voltage is then fed into a boost converter. The boost converter is a type of DC-DC converter that increases the voltage level. It consists of an inductor (L), a switch (usually a MOSFET or IGBT), a diode, and a capacitor. The inductor stores energy during the on-state of the switch and releases it during the off-state. The switch is controlled by a pulse-width modulation (PWM) signal. The duty cycle of the PWM signal determines the output voltage of the boost converter.
3. Power Factor Correction: The boost converter is operated in a way that ensures power factor correction. Power factor is improved by shaping the input current waveform to be in phase with the input voltage waveform. The control strategy involves adjusting the timing of the switch to control the amount of power drawn from the AC source during different parts of the AC voltage cycle. By controlling the phase relationship between the input voltage and current, the power factor is increased, and harmonic distortion is reduced.
4. Output Stage: The boosted and power-factor-corrected DC voltage is then smoothed using a capacitor to reduce voltage ripples.
5. Output Regulation: The output voltage is regulated to the desired level using feedback control. This is typically achieved by monitoring the output voltage and adjusting the duty cycle of the PWM signal accordingly.

The Boost PFC converter helps to achieve a high-power factor close to 1, indicating efficient use of electrical power. This is important for reducing power losses, minimising harmonics, and complying with regulations such as those outlined in the IEC 61000-3-2 standard for power quality. The parameters necessary are listed in Table 3.1.

Parameter	Vm (Peak)	Line-frequency	Switching frequency (fsw)	Output Voltage (Vo)	Current Ripple %	Voltage Ripple %	Load Current (Io)
Value	325 V	50 Hz	100 kHz	400 V	10	1	5 A

Table 3.1 Parameters for Steady State Design

$$D = 1 - \frac{V_m}{V_o} = 0.1875. \quad (3.1)$$

$$L = \frac{V_m D}{f_{sw} \Delta i_L} = 990.2\mu H \quad (3.2)$$

$$C = \frac{D}{R f_{sw} \frac{\Delta V_o}{V_o}} = 2.343\mu F \quad (3.3)$$

Using the parameters in Table 3.3 and the values of L and C are calculated using Equations (3.1)-(3.3).

The control technique of a PFC is very similar to that of the average current control except that the fact that the current reference generated by the outer loop is not constant, but its shape is that of |sin(ωt)|, and that the voltage loop has very low bandwidth, much lesser than 100 Hz. Hence, the control design presented here is developed based on techniques discussed in average current control. The simplified loop structure of the PFC is presented in Figure 3.2.

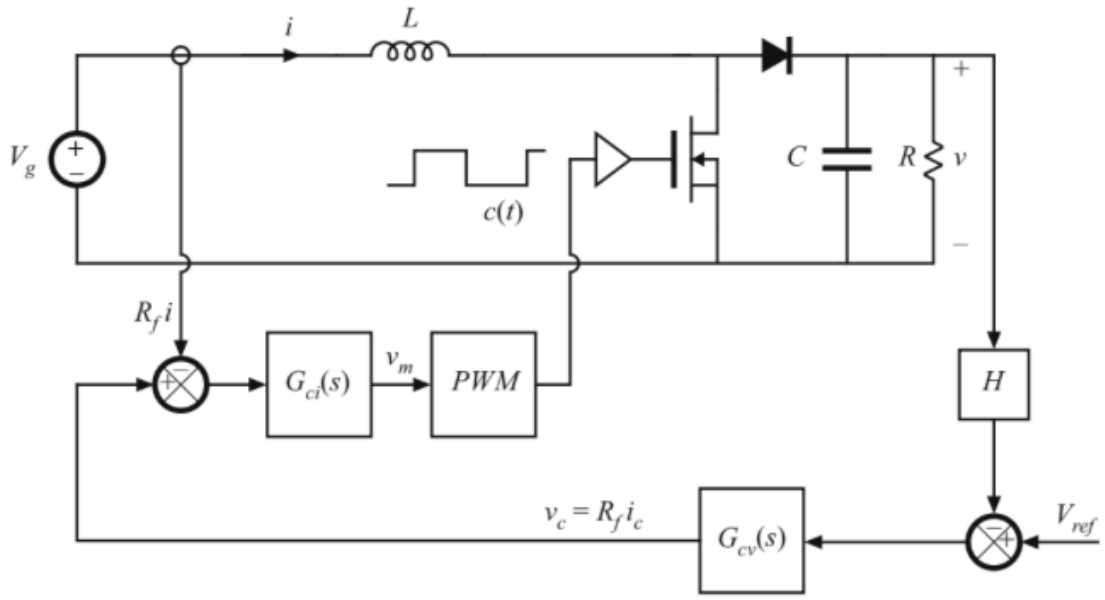

Figure 3.2 Simplified closed loop representation for demonstrating average current control in PFC.

The small signal model representation of the CBC is very well presented in [107] and the same has been represented here for design purpose in Fig 3.3

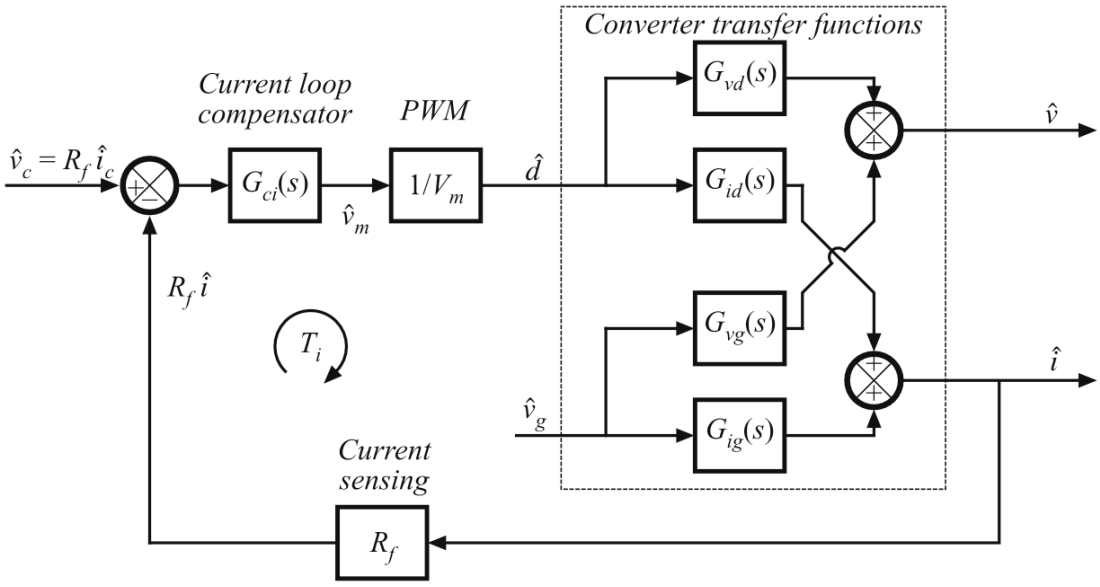

Figure 3.3 Block Diagram Representation of the small signal model of CBC converter

From Fig 3.3,

$$T_i = R_f G_{ci} \frac{1}{V_M} G_{id} \qquad (3.4)$$

Here, R_f is the gain of the current sensor, $G_{ci}$is the compensator (PI) of the current controller, Vm is the PWM gain and $G_{id}$is the transfer function relating current to duty ratio.

From Figure 3.3, G_{id} is given by,

$$G_{id}(s) = \frac{2V_o}{R(1-D)^2} \frac{1+\frac{s}{w_{zi}}}{1+\frac{s}{Q\omega_0}+\left(\frac{s}{\omega_0}\right)^2} \qquad (3.5)$$

Where, $w_{zi} = \frac{2}{RC}$ and Q=$R\sqrt{\frac{C}{L}}$

Using Equation 3.4 and 3.5, G_{ci} is designed such that T_i has a bandwidth of $\frac{f_{sw}}{10}$ and the Phase margin is >60 degree. With this inner loop closed, control to voltage transfer function $G_{vc}(s)$ is given by Equation 3.6 ,

$$G_{vc}(s) = \frac{1}{R_f} \frac{G_{vd}}{G_{id}} \frac{T_i}{1+T_i} \qquad (3.6)$$

To design the compensator, the voltage loop gain is derived and is given by equation (3.7)

$$T_v = HG_{cv}G_{vc}$$

Here, G_{cv} is the voltage loop compensator and H is the feedback gain of voltage sensor. The Voltage loop T_v is so designed that the Bandwidth of the outer voltage loop is less than 100 Hz and that the PM is at least 45 degrees.

To design the controller for PFC, following are the parameters chosen as in Table 3.2

Parameter	V_M	H	R_f	Bandwidth of inner loop	Bandwidth of inner loop
Value	4	3/400	0.25	10kHz	10 Hz

Table 3.2 Parameters to design controller for CBC converter

3.2 Design of Active IDBC based Active PFC

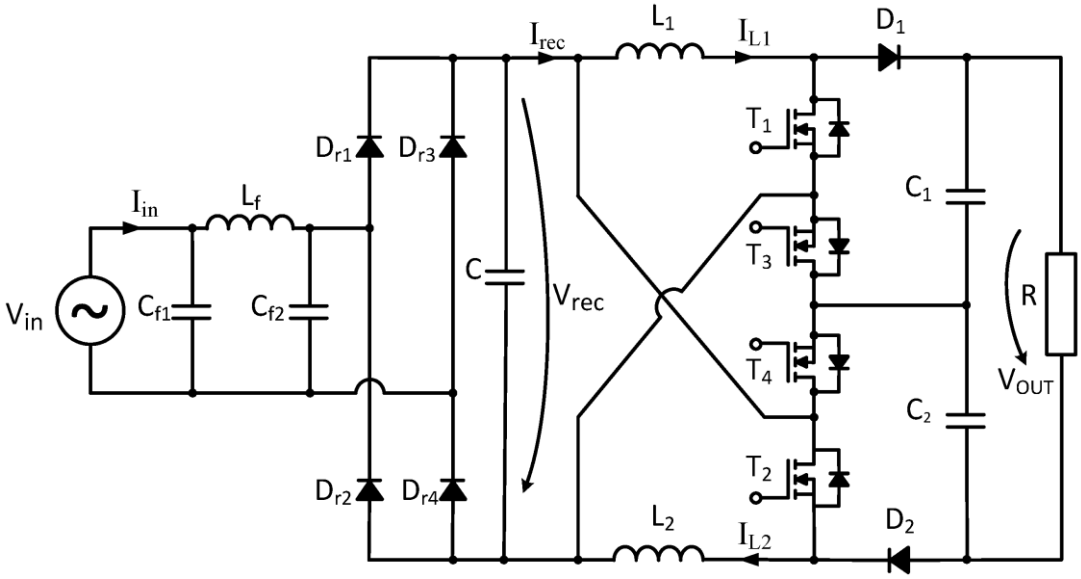

Figure 3.4 Proposed schematic of the IDBC converter

The proposed PFC application is built around a unique DC-DC power-stage topology known as the Independent Double Boost Interleaved Converter (IDBIC). The current architecture is based on [65] and its basic PFC converter topology is shown in Figure 3.4. Using the conventional steady state averaging techniques, the values of the passive components used in the converter is derived and is presented in Table 3.3

Parameter	L_1	L_2	C	C_1	C_2	R
Value	0.5mH	0.5mH	10mF	500uF	500uF	100 Ohms

Table 3.3 Design Values of IDBC Converter

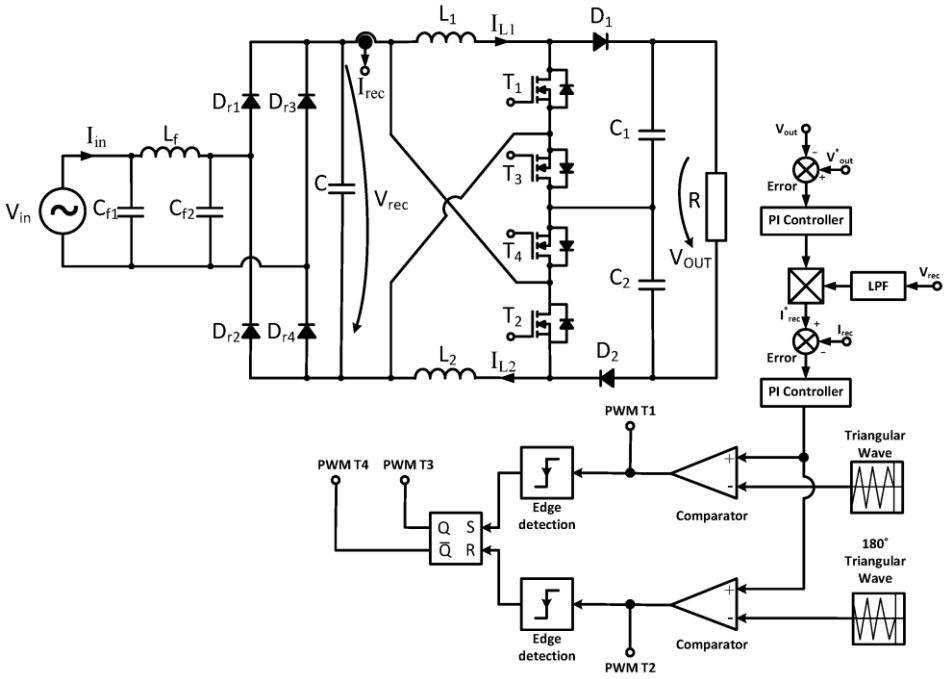

Figure 3.5 Schematic of the IDBC converter along with control scheme used for PFC application.

The control is very similar to the CBC converter, wherein the outer voltage loop is slow acting whose Bandwidth is close to 10 Hz and the inner loop is fast acting whose bandwidth is close to 1/10th of switching frequency. The output of the voltage loop compensator dictates the peak value of the current, and the shape of the current loop is synchronized with the voltage across the

diode rectifier terminals. The SR flip-flop switches the converter switches based on the error between the actual current and the reference current and is presented in Fig 3.5

IV. RESULTS AND DISCUSSION

In this section, results are presented for the design carried out in section III. The results from conventional power factor correction is presented initially followed by results from IDBC.

4.1 CBC Based Active PFC

In this section, the results of CBC based active PFC is presented in detail. This section starts with results from controller design followed by the results from PFC converter.

Fig 4.1 presents the bode plot of control to inductor current Gid(s). It is seen that the Phase Margin of Gid(s) is close to 90 deg at the cross over frequency of 64.4kHz. The phase of the Gid(s) varies from 0 to -90 degrees and hence the GM is infinite. Since the GM and PM are positive, the control to inductor transfer function is found to stable.

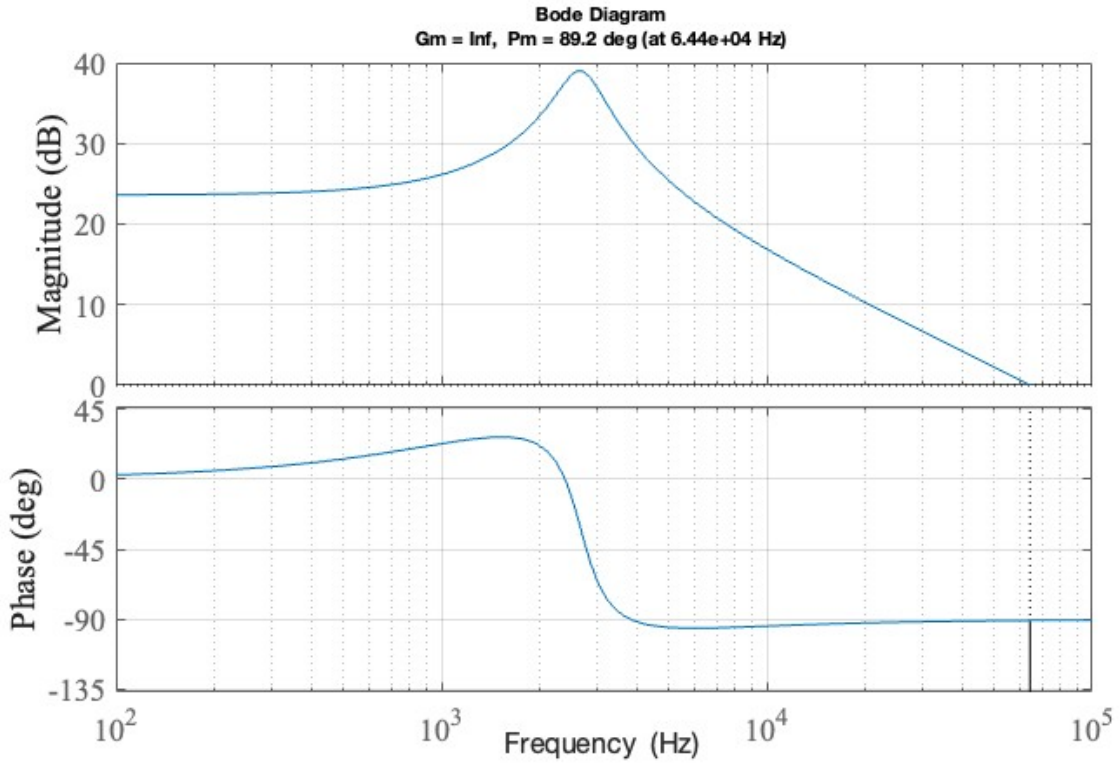

Figure 4.1 Bode Plot for Transfer function of Control to Current Gid(s)

Once Gid(s) is plotted, using Eq 3.4, the loop transfer function Tiu(s) is plotted with Gcv(s)=1, and the bode plot is presented in Fig 4.2. It is seen that the Phase Margin of Tiu(s) is close to 85 deg at the cross over frequency of 5.45kHz. The phase of the Tiu(s) varies from 0 to -90 degrees and hence the GM is infinite. Since the GM and PM are positive, the control to inductor transfer function is found to stable. Hence only a PI compensator is sufficient to set the controller bandwidth and PM to desired values.

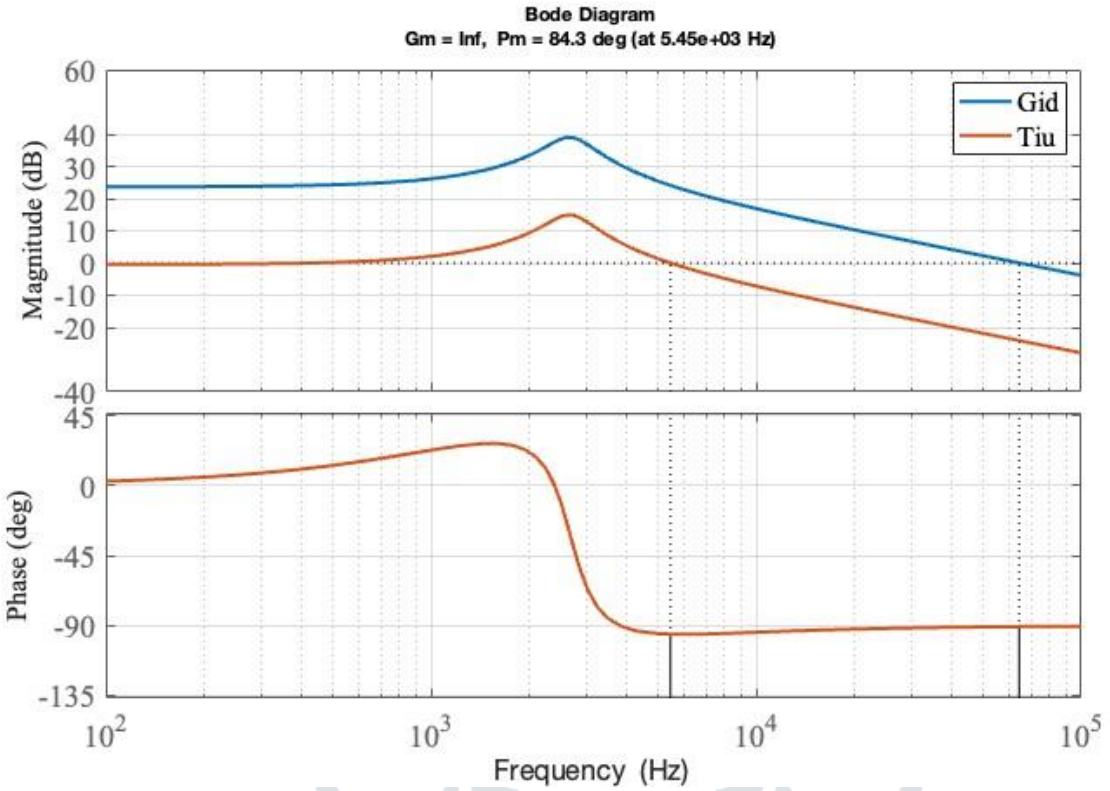

Figure 4.2 Bode Plot for Transfer function of Control to Current Gid(s) and Tiu(s)

It is desired to have a bandwidth of 10kHz and PM to 70 degrees. Hence a PI compensator is sufficient. It is seen that from Figure 4.2, at 10KHz, the required gain is 7.6dB and a PM to be reduced by close to 15 degrees. Therefore, the poles of the Poles of the PI compensators are placed at 1.66kHz and 60kHz with gain as 2.488. The resulting compensator is presented in Fig 4.3

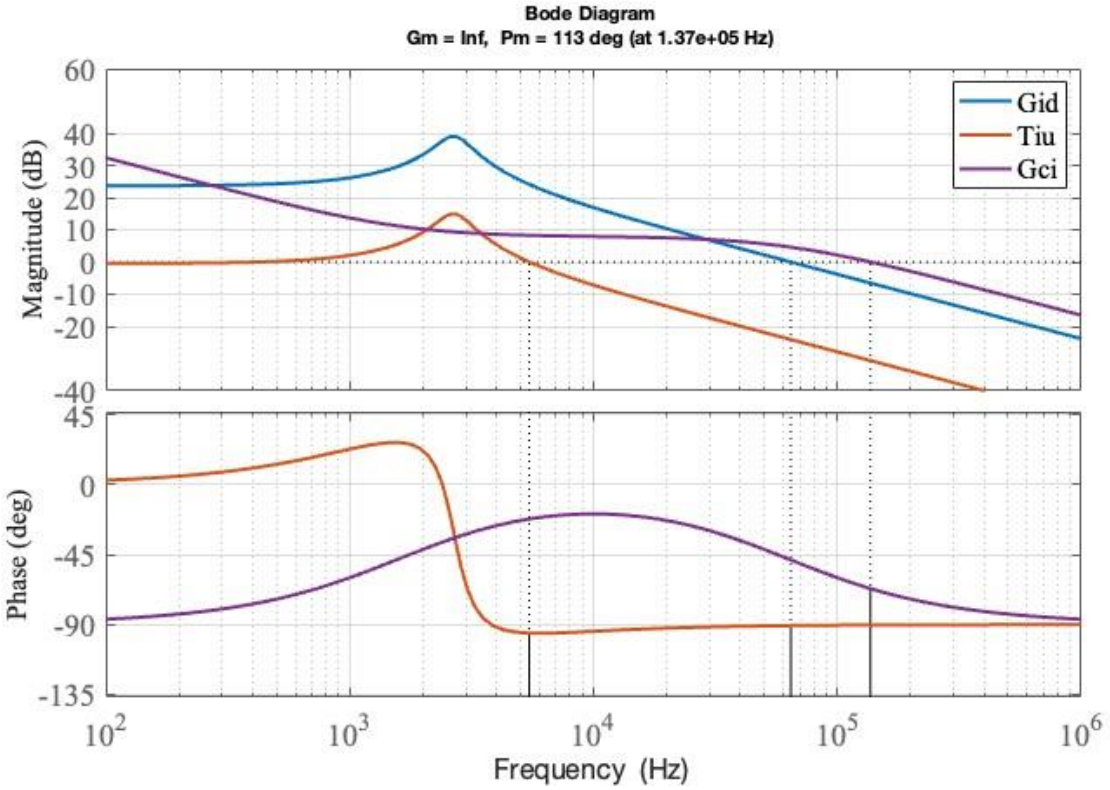

Figure 4.3 Bode Plot for Transfer function of Control to Current Gid(s), Tiu(s) and Gci(s)

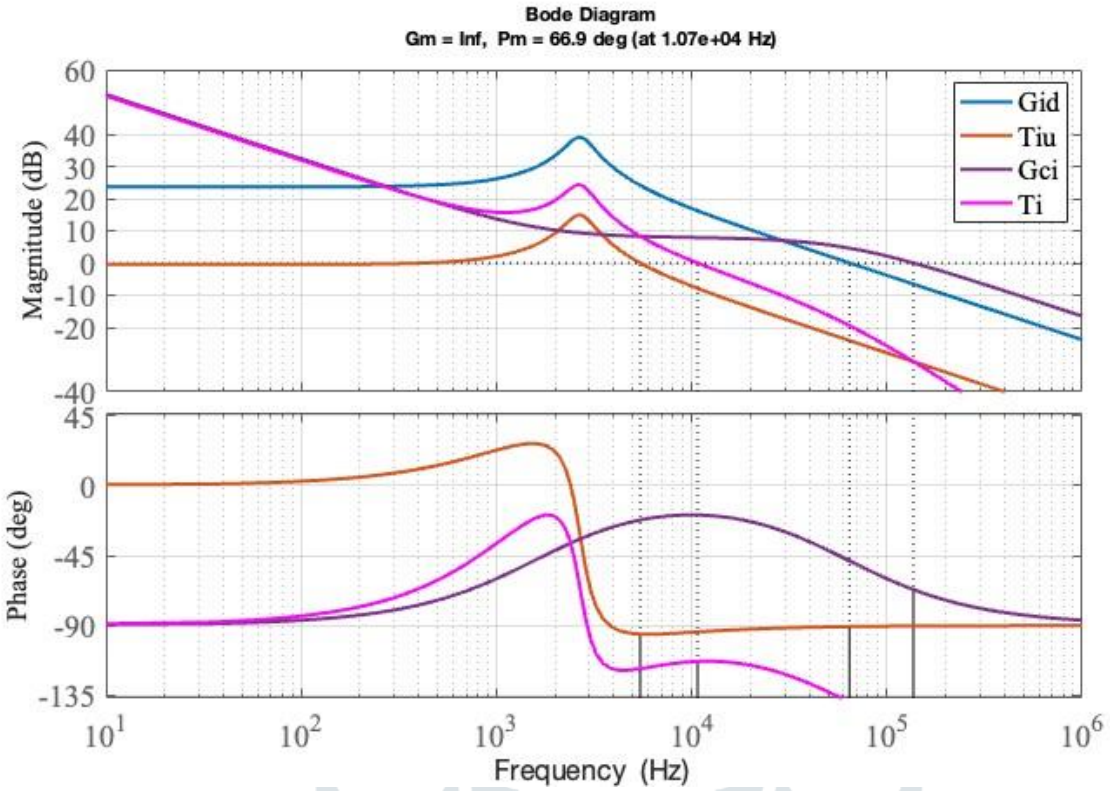

Figure 4.4 Bode Plot for Transfer function of compensated current loop gain.

The compensated loop is found by multiplying the uncompensated loop with the designed compensator, and the results are presented in Fig 4.4. The compensated loop is found to have a crossover frequency (BW) of 10KHz with a PM of 67 degrees. The corresponding step response for the same is plotted in Fig 4.5. It is clearly seen that the current reaches a base value of 4 A (this is because Rf = 0.25). Since the bandwidth is set to 10kHz, the settling time is seen as close to 0.8ms.

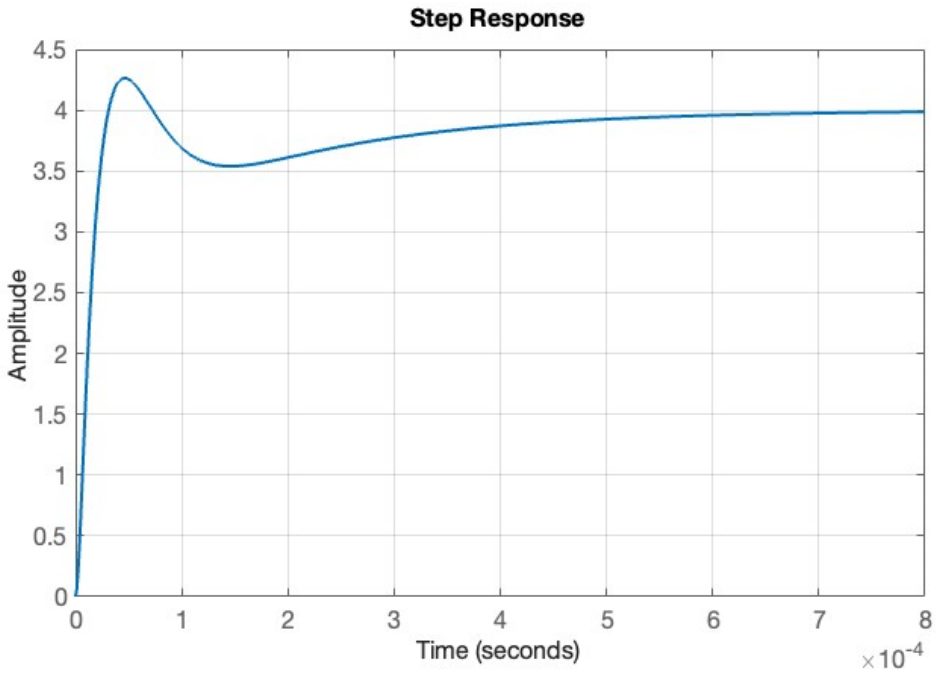

Figure 4.5 Step Response of the inner current Loop

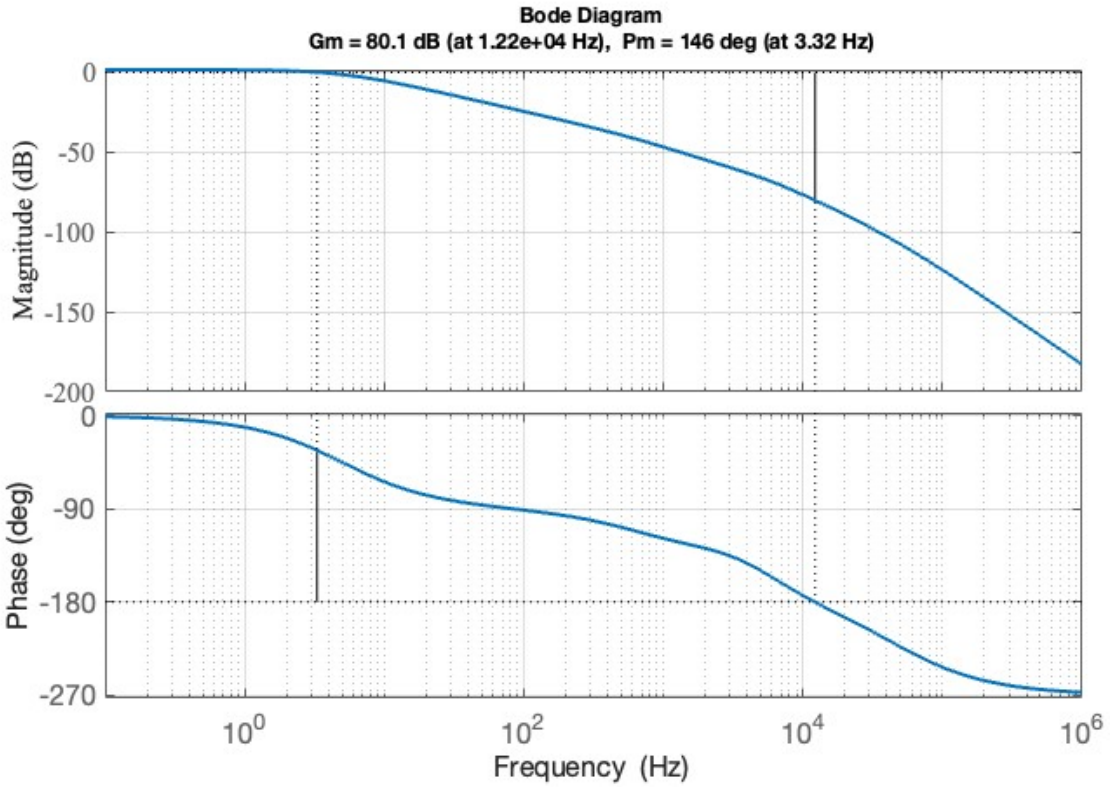

Figure 4.6 Bode Plot for Uncompensated Voltage Loop with current Loop closed.

With the current control loop closed, the next step is to design the voltage loop compensator. The design method remains the same except that the BW requirement is too low. The low bandwidth requirement is extremely important because, the CBC is required to not transfer the dominant 100Hz component from the rectifier terminals to the load. In this case, the BW is set to just 10Hz, which also makes the controller very slow. The bode plot of the uncompensated loop with current loop closed is given in Fig 4.6. It is seen that the PM is extremely high as 143 deg.

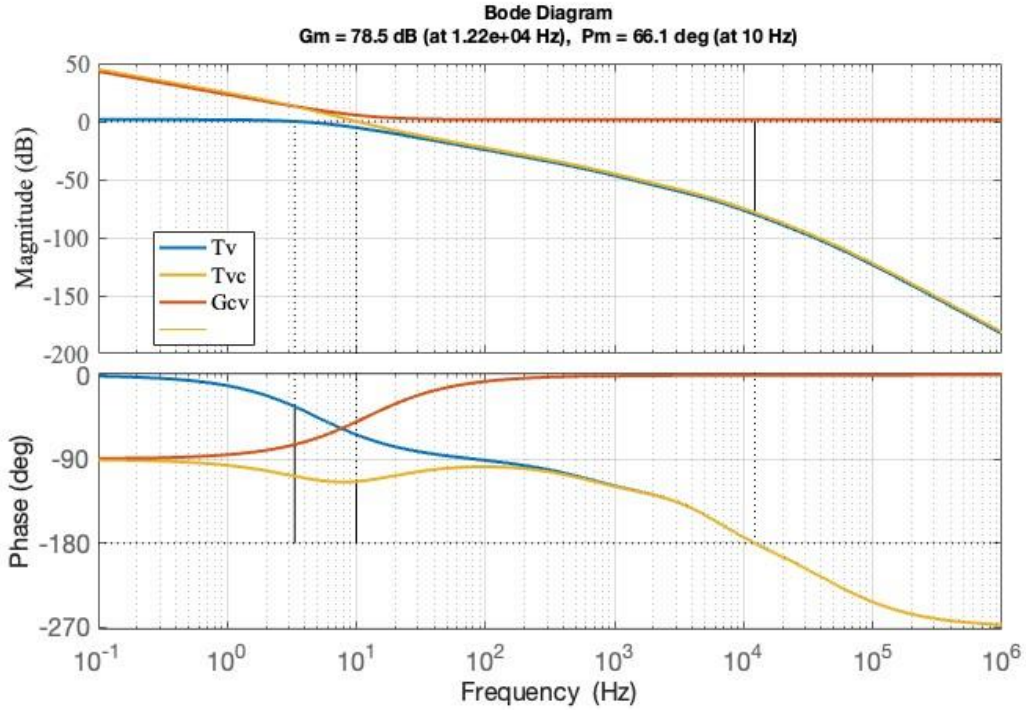

Figure 4.7 Bode Plot for Transfer function of compensated voltage loop gain.

Using the same technique as mentioned above, a simple PI is sufficient to set the PM to 70 degrees with cross over frequency to 10 Hz. The designed compensator along with compensated loop is presented in Fig 4.7. It is seen that the compensated loop has PM of 66 deg with BW of 10Hz. The corresponding normalized step response is plotted in Fig 4.8. The current controller being the fastest loop has a settling time of 0.8ms, while the slower voltage loop has a large setting time of 0.14s.

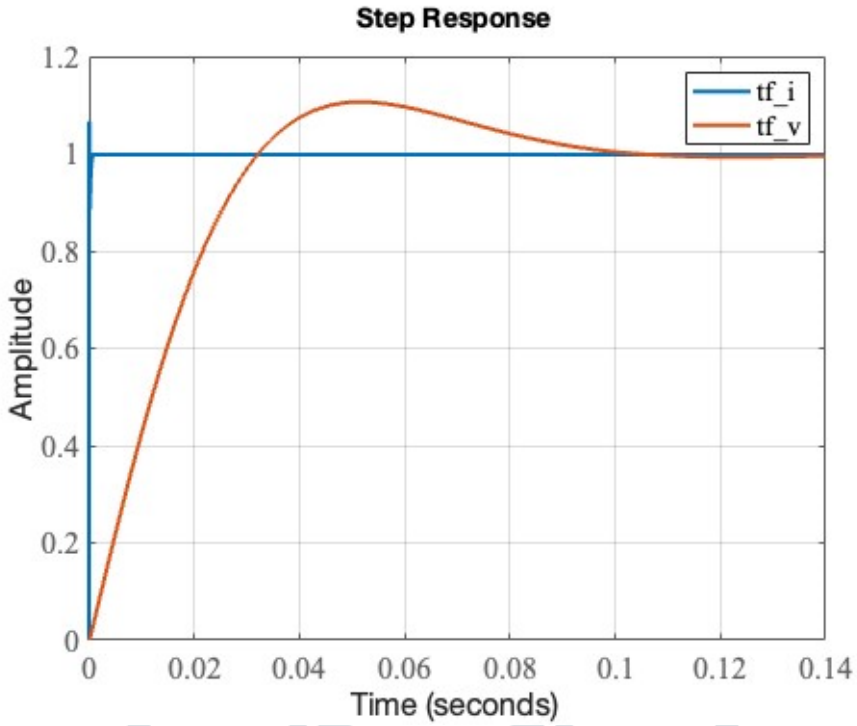

Figure 4.8 Step Response of the inner current and Outer Voltage Loop

The designed inner and outer loop compensators are fed to the closed loop of the PFC converter and the results are presented in this section.

Fig 4.9 presents the startup scheme of the PFC, where the output is seen to rising from 0V and finally reaching the reference of 360V. The settling time of the DC voltage is close to 0.15s which is in close agreement with the step response of the outer voltage loop. The corresponding Grid voltage and the grid current are also presented. It is seen that the grid voltage and grid current are totally in phase, and the grid current is sinusoidal. The THD spectrum for this case is presented in Fig 4.10. It is clear from THD spectrum that the grid current THD is just 3.10 % which is in total alignment with the IEEE Grid standards.

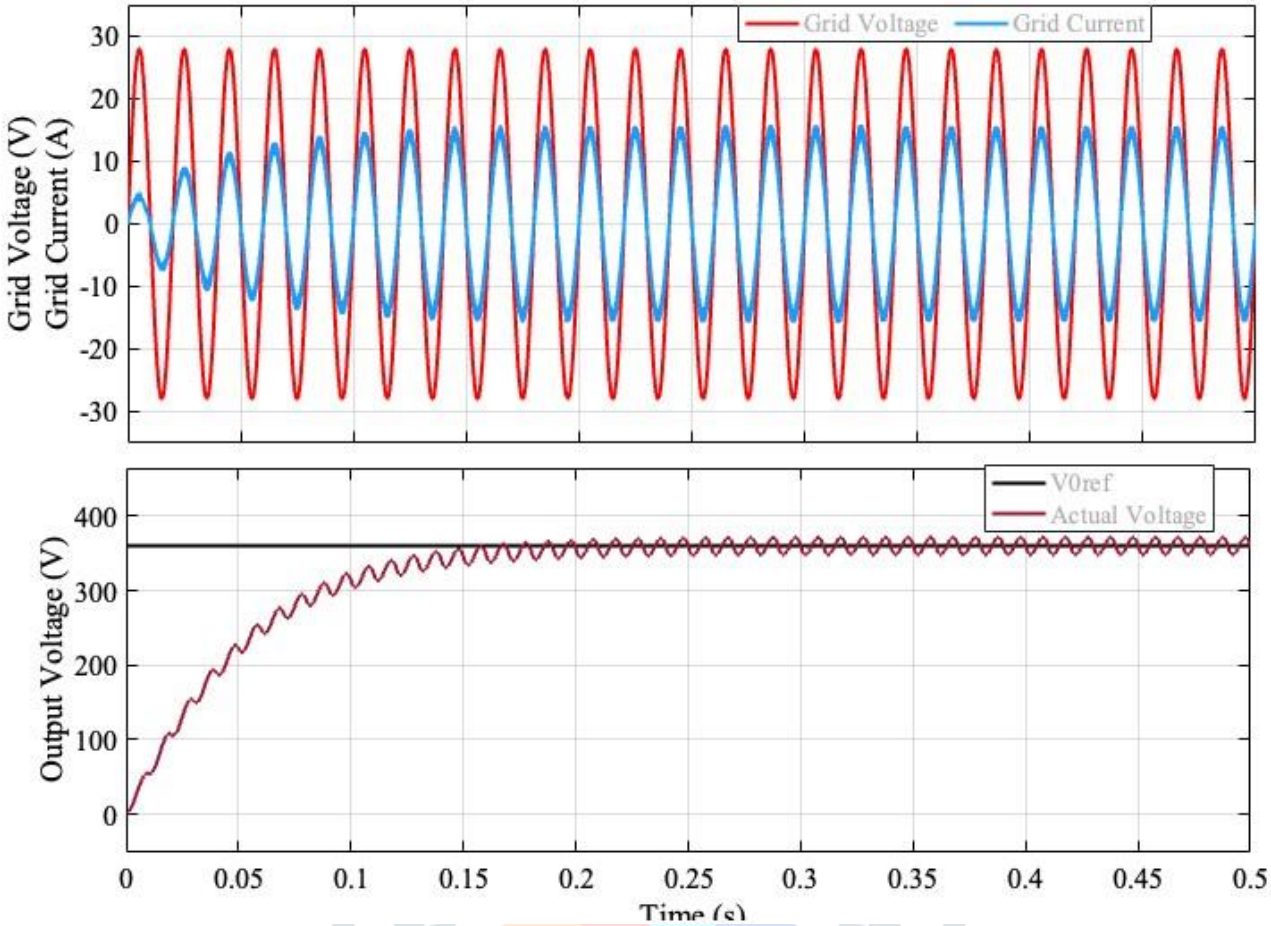

Figure 4.9Grid Voltage and Current along with output voltage waveforms for CBC

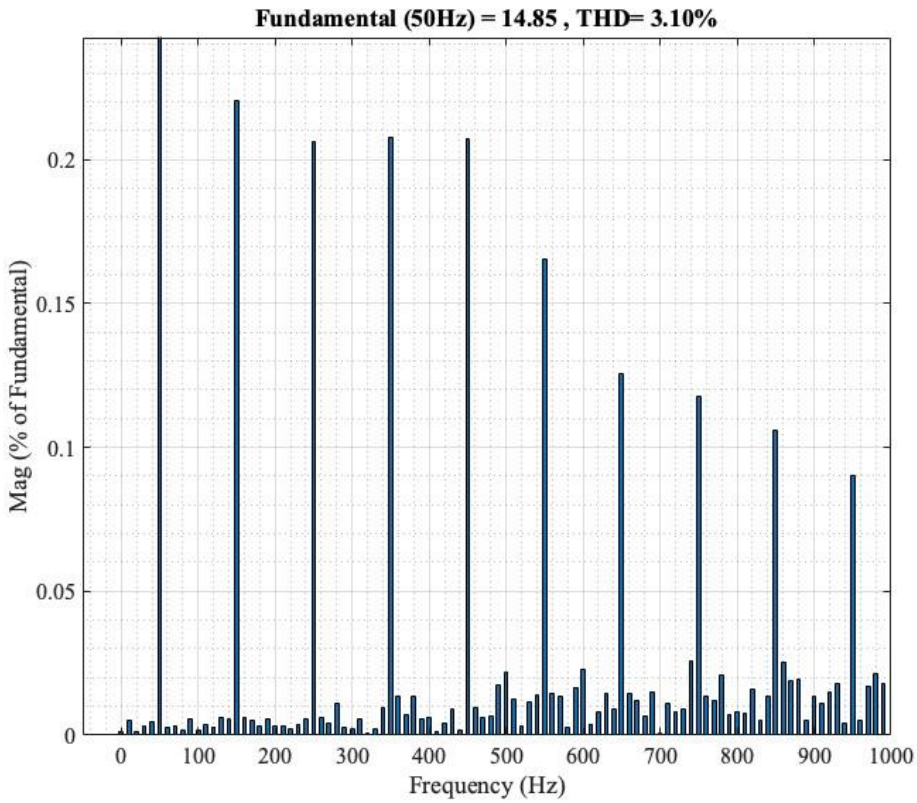

Figure 4.10FFT spectrum of AC Line Current for Resistance R=80 Ohms and Vref = 360 V

Further, the PFC converter is subjected to load changed, where the load is increased by 16.66% and the results are presented in Fig 4.11. The controller sets the voltage back to reference value of 360 V in a time of 0.2s. Since the load is increased, the power drawn from the source is also increased, which is reflected by higher peaks in grid current. The Power factor is again maintained to 1. The corresponding THD is presented in Fig 4.12.

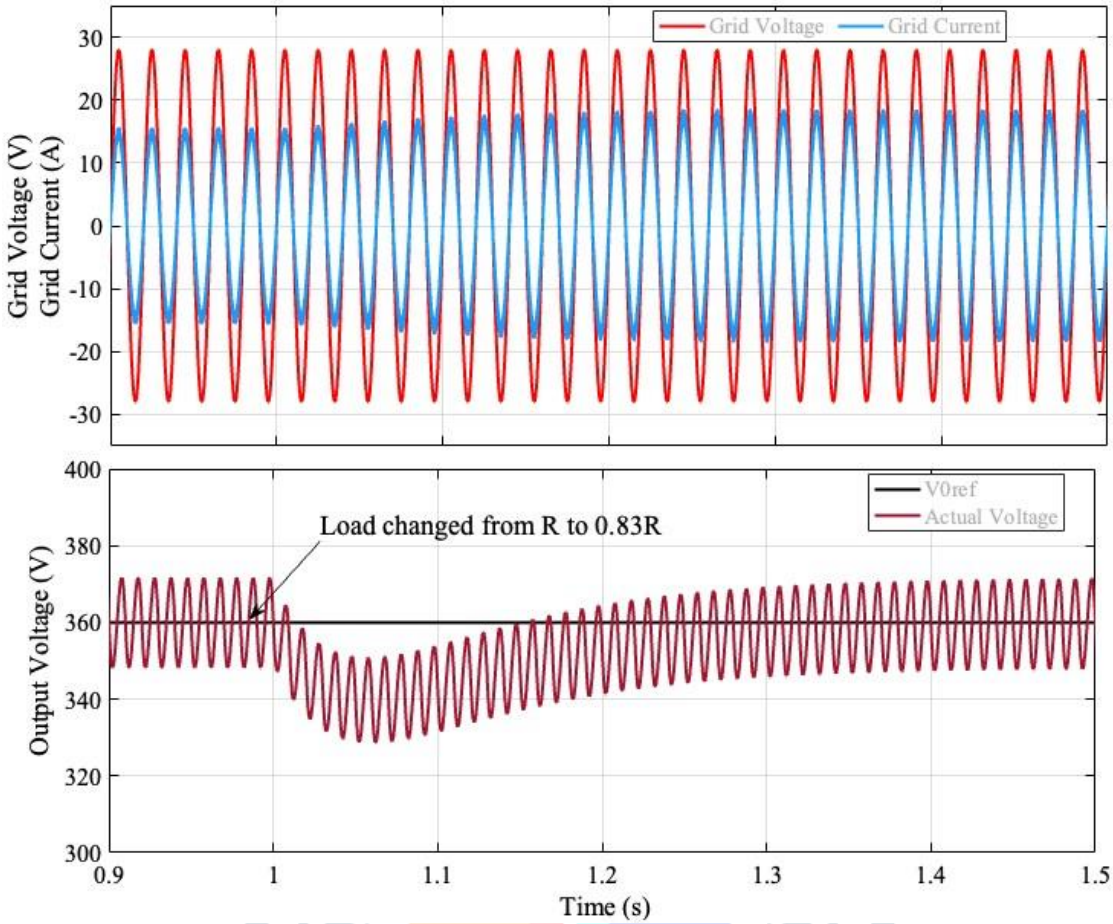

Figure 4.11 Response of PFC for step change in Load from R to 83% of R

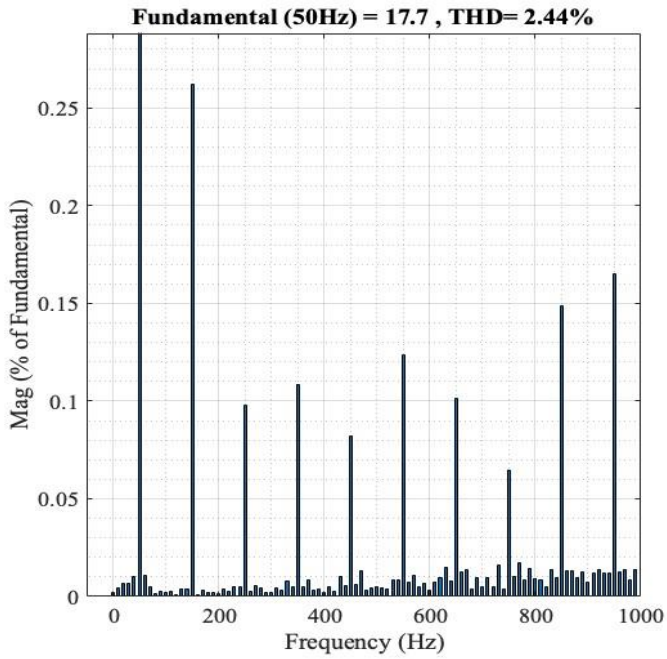

Figure 4.12 FFT spectrum of AC Line Current for Resistance R=66.66 Ohms and Vref = 360 V

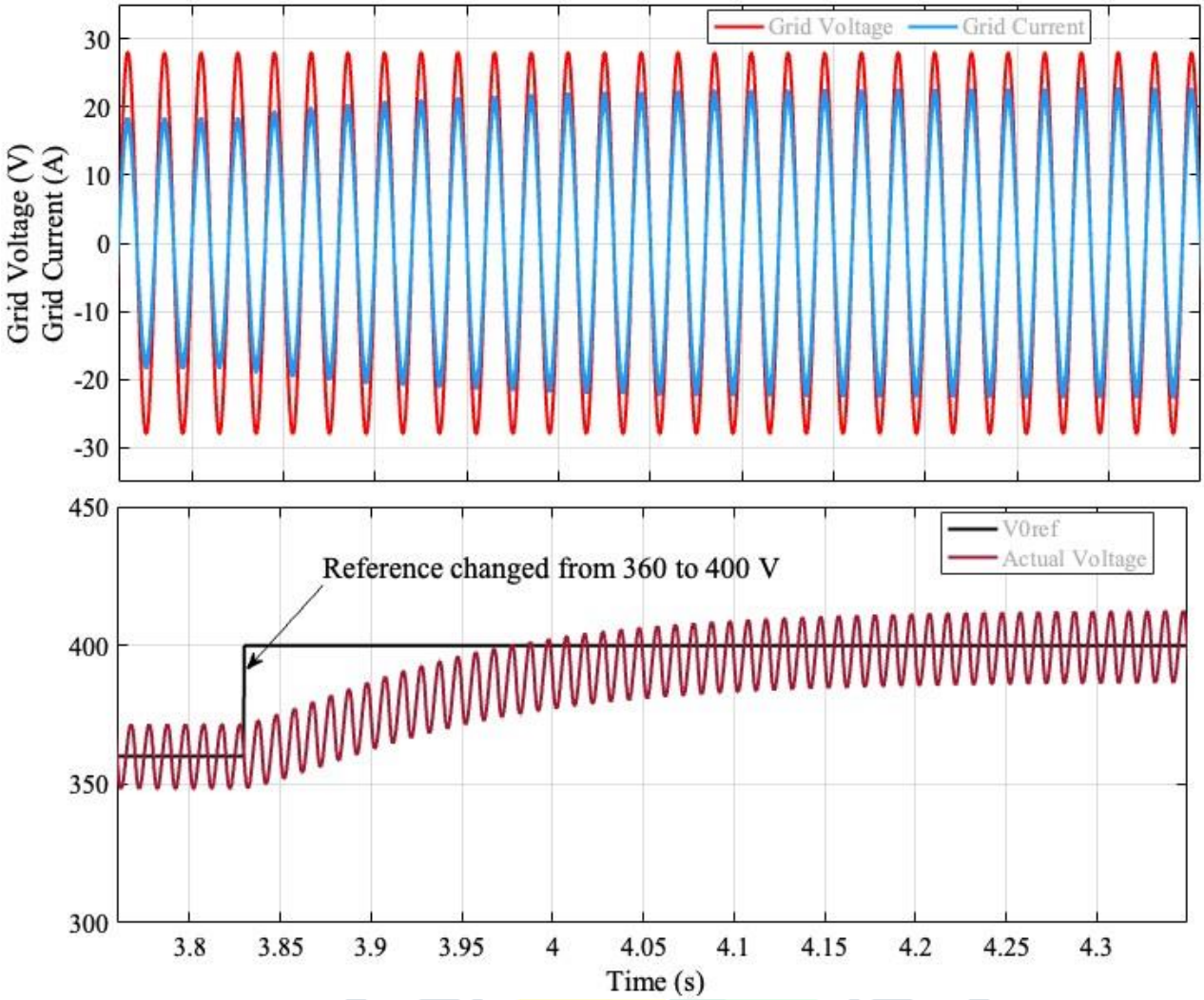

Figure 4.13 Response of PFC for step change in reference from 360 V to 400 V

To test the ruggedness of the controller, the reference command to the PFC is changed from 360 to 400V, and the results are presented in Fig 4.13. The controller is capable of tracking the reference within a time of 0.2s. Since the load is increased, the power drawn from the source is also increased, which is reflected by higher peaks in grid current. The Power factor is again maintained to 1. The corresponding THD is presented in Fig 4.14.

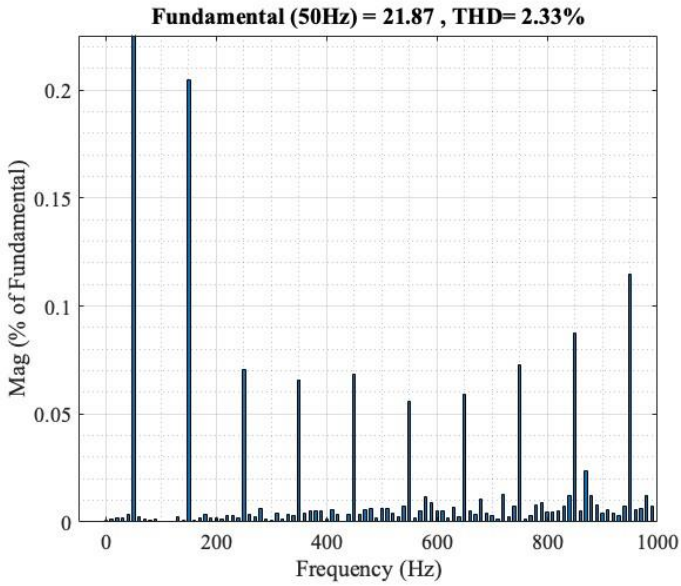

Figure 4.14 FFT spectrum of AC Line Current for Resistance R=66.66 Ohms and Vref = 400 V

4.2 IDBC Based Active PFC

In this section, the results from IDBC based PFC are discussed in detail. Since the controller design is very similar to CBC based converter, the controller design is exclusively not discussed.

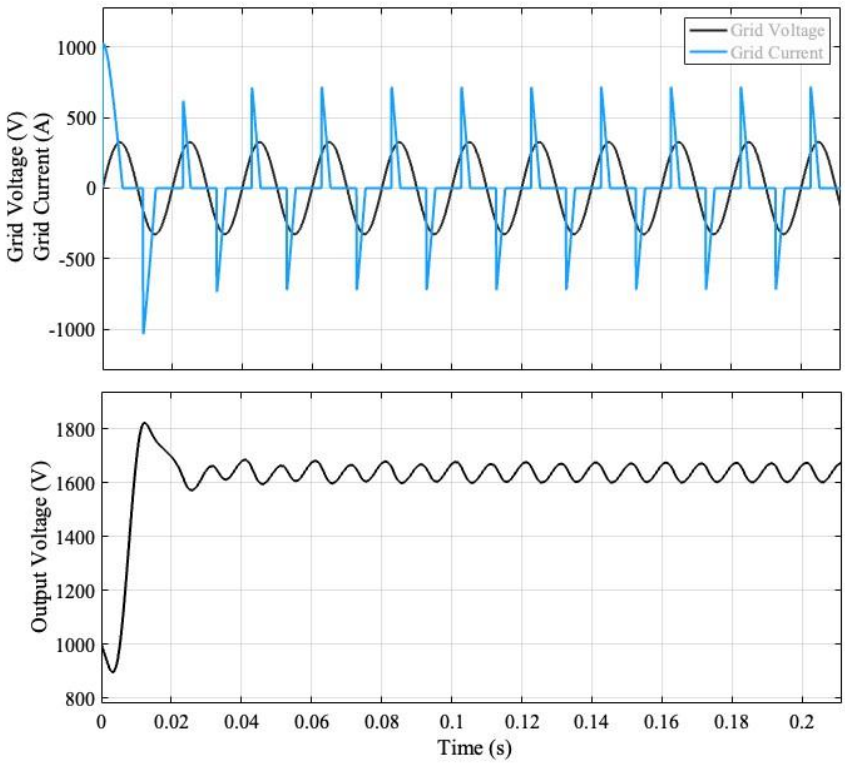

Figure 4.15 Open Loop Results for IDBC converter

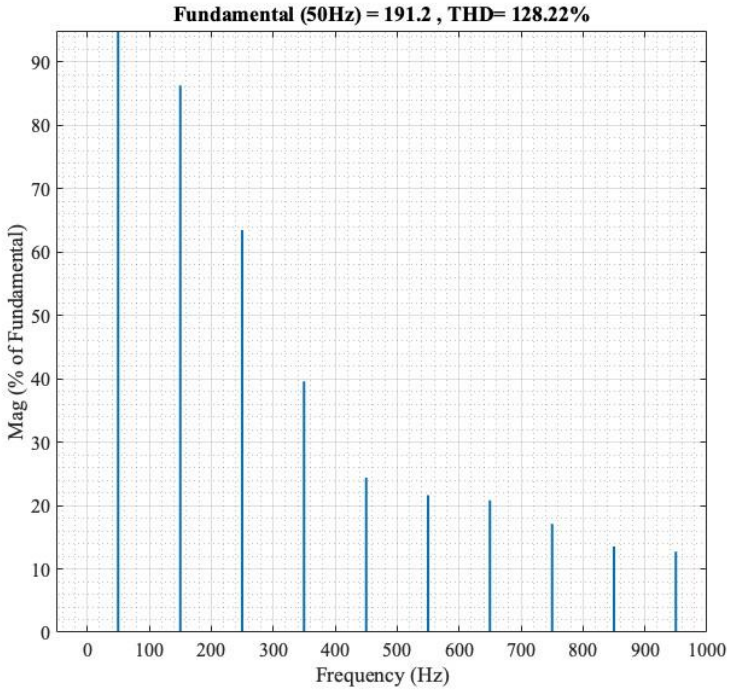

Figure 4.16 Line Current THD when IDBC is run in open loop mode

The open loop results for IDBC converter running in open loop is presented in Fig 4.15. Though the converter is boosting the voltage to as high as 1600V, the power converter is highly lossy. The AC line current is highly non-sinusoidal. This is since the diode rectifier is fitted with a capacitor of 10mF. The corresponding line current THD is also presented in Fig 4.16. The THD is as high as 128.22% which is much above the acceptance value.

The IDBC converter is further run in closed loop with the designed closed loop and the results are presented in Fig 4.17. The results present the startup scheme followed by a change in reference. It is seen that the output DC voltage reference set is 1500 V, and the actual voltage follows the reference voltage with an overshoot of 49% and settling time close to 0.4s. The higher settling time is due to the fact the outer voltage loop is very sluggish to remove 100Hz ripples from the diode rectifier. The controller is found to set duty cycles such that the actual voltage follows the reference. The grid voltages and currents are found to be in exact phase with each other with pf close to one. The THD corresponding to this case is presented in Fig 4.18. The THD is found to be 7.37%. Though the value is found to be slightly greater than regulatory standards, this can be bought down by tuning the design parameters.

At t=1s, a reference change in DC voltage of 1700V is initiated to the controller. The controller sets the new duty cycle to meet the new reference. The overshoots are well under control and the settling time is close to 0.4s. The THD corresponding to this case is presented in Fig 4.19. The THD is found to be 7.33%.

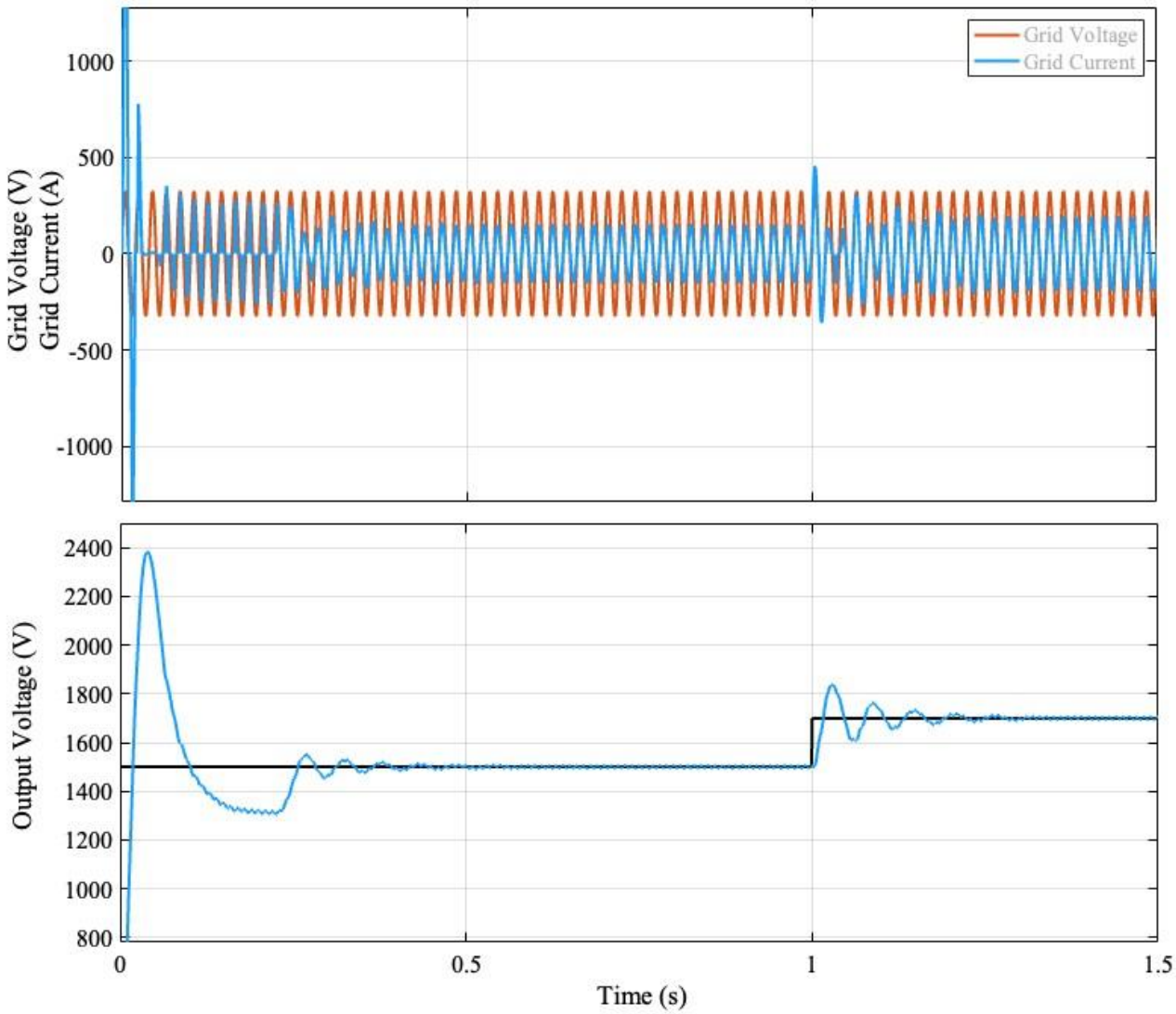

Figure 4.17 Grid Voltage and Current along with output voltage waveforms for IDBC showing start-up and Reference change

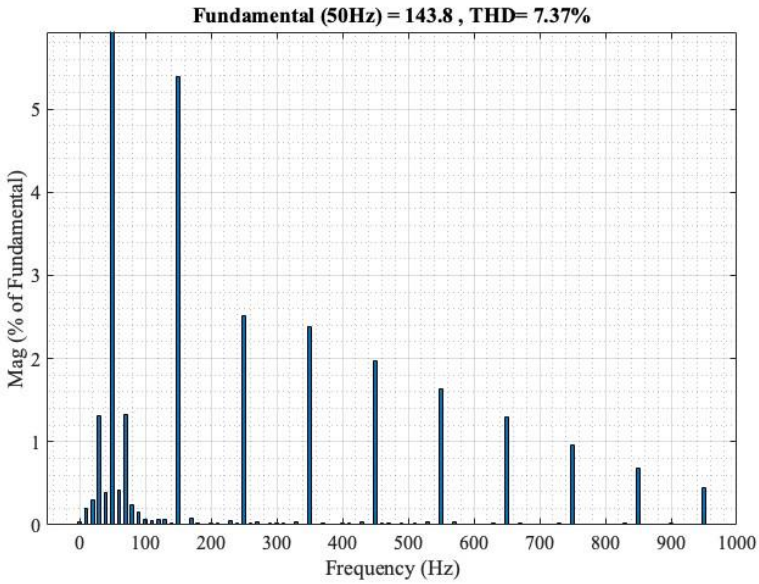

Figure 4.18 THD of AC Line current of IDBC based PFC for Vo =1500 V

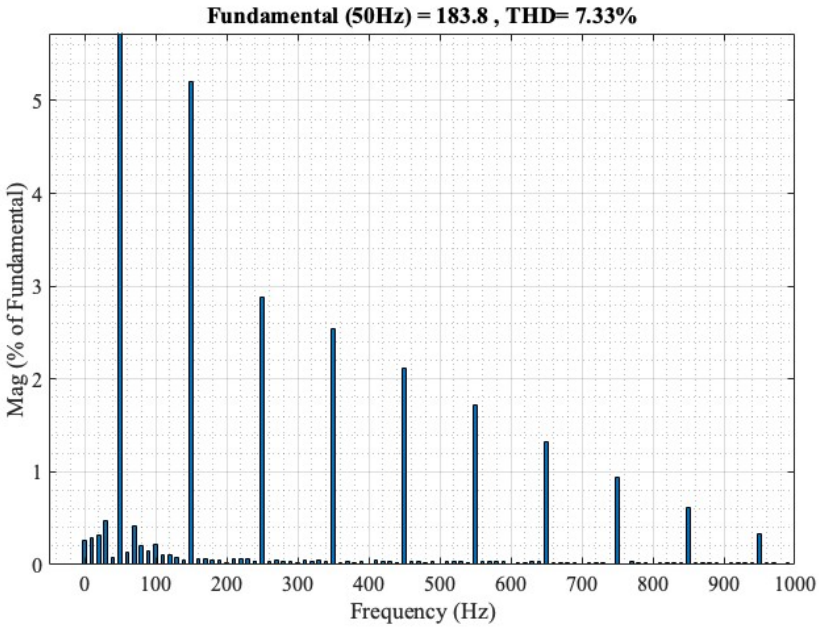

Figure 4.19 THD of AC Line current of IDBC based PFC for Vo =1700 V

V CONCLUSION

In this paper, diode rectifier based unidirectional power supplies are discussed in detail whose applications range from laboratory equipment to satellite/propulsion systems. One of the major problems with such rectifier systems is the non-linear AC current drawn from utilities due to charging and discharging of filter capacitors, connected to output terminals of diode rectifier. The analysis and results presented in the thesis reveal that such effects are so detrimental that, at times, the power factor is less than 0.5 and the THD drawn is greater than 170%. Possible solutions to such problems are also discussed, and they can be categorised as passive PFCs and active PFCs. One of the passive solutions is to connect an LC filter at the terminals of the diode rectifier. Since the filters are designed at 100 Hz, the sizes of such line reactors are very high and hence may not be a viable option.

Further, active solutions are designed using two converters: CBC and IDBC. The objective of active solution is to shape the duty cycle such that the input current to the converter is in exact alignment with the voltage across the terminals of the rectifier. The control scheme for the same is designed and results are presented in detail. The proposed control schemes can align grid current with the grid voltage such that the current is in sinusoidal shape and the power factor is unity. The THD for the same is also presented.

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