JETIR.ORG ISSN: 2349-5162 | ESTD Year : 2014 | Monthly Issue
JOURNAL OF EMERGING TECHNOLOGIES AND INNOVATIVE RESEARCH (JETIR)
An International Scholarly Open Access, Peer-reviewed, Refereed Journal

IMPLEMENTATION OF LOW POWER BASED CONDITIONAL BOOSTING AMPLIFICATION BY USING MILLER COMPENSATION TECHNIQUE

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ABSTRACT:

Power consumption is considered as one of the important challenge in modern VLSI design along with area and speed consideration. Flip-flop plays very important role in digital systems. In this paper comparative study of four different flip flops which includes pulse triggered as well as conditional technique flip flop such as IP-DCO, MHLFF, CPSFF, and CPFF topologies in sub threshold operation are examined. In recent years the ultra low power application can be possible using sub threshold technology. Using the advantage of this technology the power consumption of these flip flops is minimized. Sub threshold circuit consume less power than strong inversion circuit at the same frequency. Design is done using TANNER in TSMC 180nm technology. Conditional-boosting flip-flop is proposed for ultra-low voltage application where the supply voltage is scaled down to the near-threshold region. The proposed flip-flop adopts voltage boosting to provide low latency with reduced performance variability in the near threshold voltage region. It also adopts conditional capture to minimize the switching power consumption by eliminating redundant boosting operations. Further, this project is enhanced by implementing multi-bit flip-flop concepts for further reduction of power constraints.

KEYWORDS:

Amplifier, Miller compensation, flip flop, conditional boosting.

INTRODUCTION:

As stated by International Technology Roadmap for Semiconductor power consumption is considered as one of the important challenge in VLSI along with speed and area consideration. Different ways for reducing the power consumption have been proposed. In all these challenging methods minimizing power supply voltage gives direct and effect on reducing power consumption. Flip flops are major building blocks in digital VLSI system. The applications areas where flip flops are majorly used are in registers, pipelines, state machines for sequencing data. Flip flop have direct impact on power consumption and speed of VLSI system. Flip flop and latches consume more power because of redundant transitions & clocking system which is included in it. Thus our aim is to design high performance and also power efficient flip flop. The amplification can be observed from various papers. A 100-MHz 100-dB operational amplifier with multipath nested miller compensation structure. A cascode miller-compensated three-stage amplifier with local impedance attenuation for optimized complex-pole control in which

there is a high observed in the design [4]. The results of the comparison of representative master-slave latches and flip-flops illustrate the advantages of our approach and the suitability of different design styles for high-performance and low-power applications [9]. By removing the speed and power bottlenecks of the original true-single-phase clocking (TSPC) and the existing differential latches and flipflops, both delays and power consumptions are considerably reduced [3].

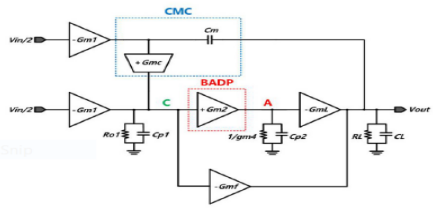

Fig. 1. Structure of the proposed buffered asymmetric dual-path with cascode Miller compensation.

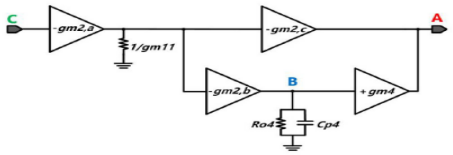

Fig. 2. Details of the transconductance from node C to node A.

The above design structure, as depicted in Fig. 1, comprises a BADP non-inverting gain stage, a CMC block, a feed-forward block, and two inverting gain stages. The CMC block integrates the Miller compensation capacitor Cm with the transconductance Gmc of transistor M5 to introduce a zero at approximately Gmc/Cm frequency, effectively canceling the BLP at minimal cost. While the three gain stages from Vin to Vout primarily contribute to DC gain, the feed-forward block's contribution is negligible compared to the product of the second and third gain stages. The first gain stage employs a folded cascade structure to achieve high DC gain and enable functionality of the CMC block. Finally, the third gain stage serves as a driver stage for the large capacitive load CL.

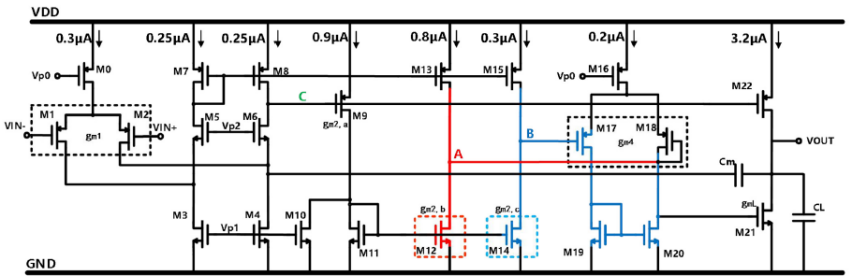

Fig 3 : Schematic of the existing three stage amplifier design

In a 65 nm CMOS technology, the compact three-stage amplifier occupies a mere 0.00107 mm2, inclusive of bias circuits and compensation capacitor. Operating at 1 V, it statically consumes only 6.62 µW. With a DC gain surpassing 100 dB, it accommodates loading capacitance CL from 0.6 nF to 2.1 nF (typical: 1.5 nF)

CONDITIONAL BOOSTING AMPLIFIER:

A conditional boosting flip-flop is a type of flip-flop circuit that incorporates conditional boosting techniques to enhance its performance in capturing input data. This flip-flop selectively applies boosting operations based on the logic states of both its input and output signals. By integrating output-dependent presetting and input-dependent boosting principles, the conditional boosting flip-flop optimizes its operation for different

input data scenarios. This approach allows for faster data capture when necessary while minimizing unnecessary power consumption during normal operation.

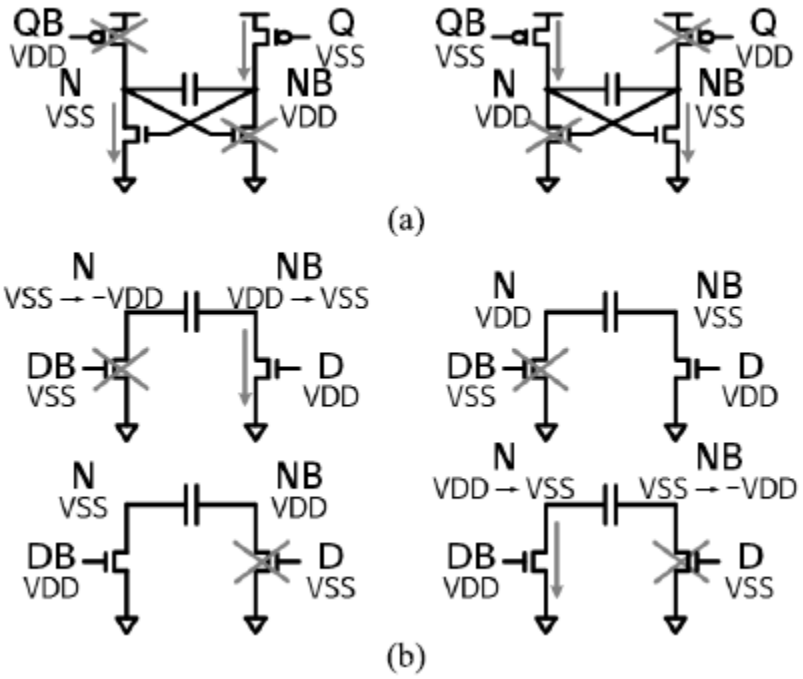

Fig 4: Conceptual circuit diagrams for (a) output data-dependent presetting (b) input data-dependent boosting

To facilitate output-dependent presetting, the preset voltages of capacitor terminals N and NB are determined by the outputs Q and QB, as depicted in Fig. 4(a). When Q is low and QB is high, N and NB are preset to low and high, respectively (left diagram in Fig. 4(a)). Conversely, when Q is high and QB is low, N and NB are preset to high and low, respectively (right diagram in Fig. 4(a)). For input-dependent boosting, the non-inverting input (D) is linked to NB via an nMOS transistor, while the inverting input (DB) is linked to N via another nMOS transistor, as shown in Fig. 4(b). Consider a scenario where a low data is stored in the flip-flop, resulting in capacitor presetting according to the left diagram in Fig. 4(a). In this case, a high input causes NB to be pulled down to ground, thereby boosting N toward –VDD due to capacitive coupling (upper left diagram in Fig. 4(b)). Conversely, a low input connects N to ground, but since the node is preset to VSS, no voltage change occurs at NB, leading to no boosting (lower left diagram in Fig. 4(b)). In the other scenario where a high data is stored in the flip-flop, resulting in capacitor presetting according to the right diagram in Fig. 4(a), a low input pulls N down to ground, allowing NB to be boosted toward –VDD due to capacitive coupling (lower right diagram in Fig. 4(b)).

	input (D)	output (Q)	boosting node (N)	boosting node (NB)
output-dependent presetting	-	VSS	VSS	VDD
		VDD	VDD	VSS
input-dependent boosting	D=VDD	VSS	VSS → −VDD	VDD → VSS
		VDD	VSS	VDD
	D=VSS	VSS	VDD	VSS
		VDD	VDD → VSS	VSS → −VDD

Fig 5: Results for different inputs of Q and QB

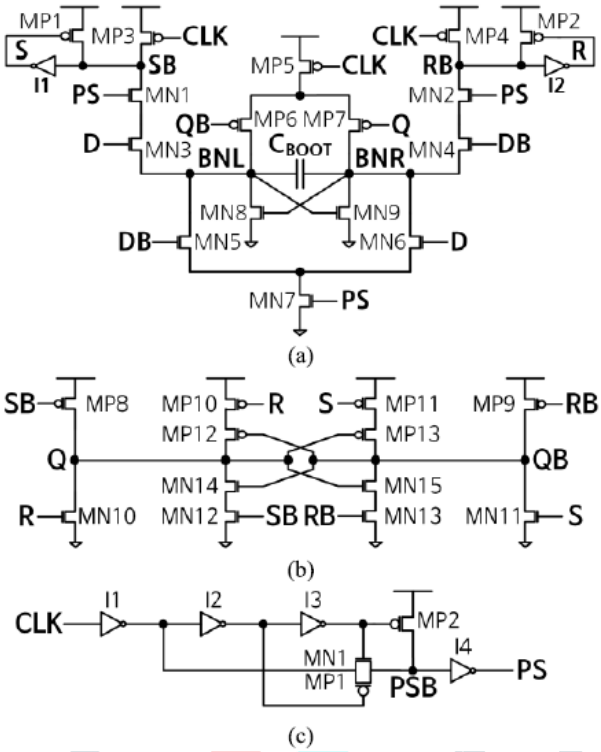

Fig 6: Schematic of the proposed circuit

The system comprises a conditional-boosting differential stage, a symmetric latch, and an explicit brief pulse generator. In the conditional-boosting differential stage depicted in Fig.6(a), MP5/MP6/MP7 and MN8/MN9 are utilized for output-dependent presetting, while MN5/MN6/MN7 with boosting capacitor CBOOT handle input-dependent boosting. The symmetric latch, illustrated in Fig.6(b), comprises MP8–MP13 and MN10–MN15. Certain transistors within the differential stage are activated by a brief pulsed signal PS generated by a novel explicit pulse generator shown in Fig.6(c). Differing from conventional pulse generators, the proposed pulse generator lacks a pMOS keeper, resulting in heightened speed and reduced power consumption by eliminating signal fighting during PSB's pull-down. MP1, added in parallel with MN1, fulfills the keeper's role in maintaining a high logic value of PSB and aids in swiftly pulling down PSB. At CLK's rising edge, PSB is rapidly discharged by MN1, MP1, and I1, causing PS to go high. Following the latency of I2 and I3, PSB is charged by MP2, resulting in PS returning to low, generating a brief positive pulse at PS with a width determined by the latency of I2 and I3. During CLK's low phase, PSB is held high by MP1, despite MP2 being inactive. Our assessment indicates energy savings of up to 9% for identical slew rates and pulse widths.

VERIFICATION RESULTS:

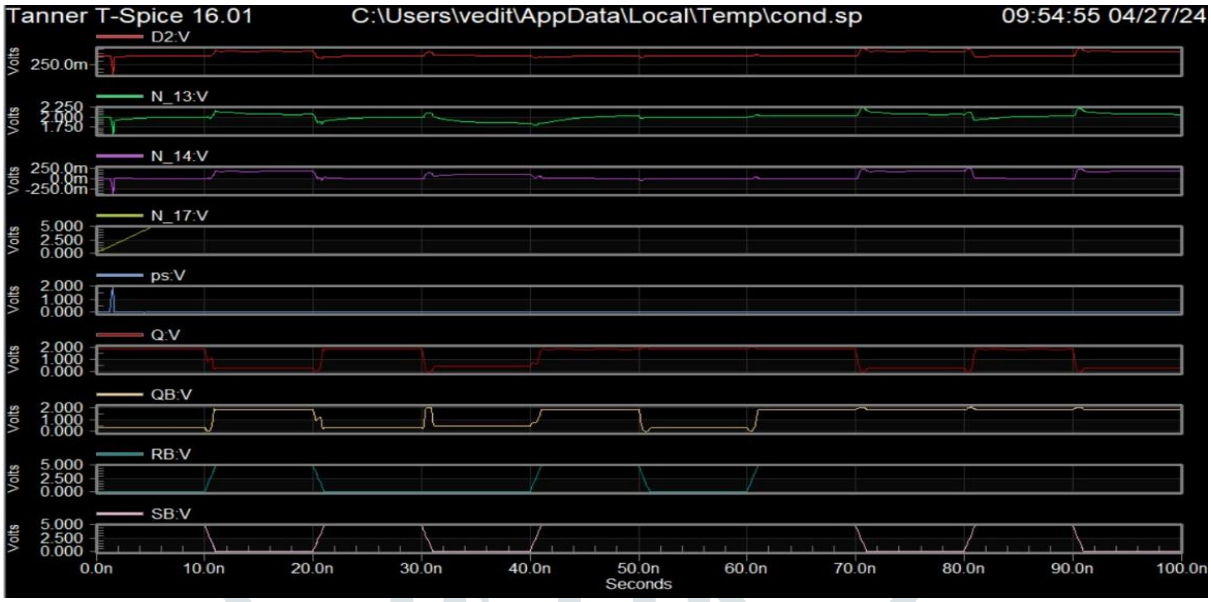

Fig 7: Amplified output waveform

The system exhibited varying power consumption dynamics, with an average power draw of 8.1984W. Notably, power consumption fluctuated between a minimum of 0.00000W and a maximum of 1.7371W during this period. The setup time required for the system to stabilize was recorded at 0.03 seconds, aligning closely with the DC operating point. Further analysis revealed a transient period lasting 0.39 seconds, indicating the time taken for the system to settle into a steady state.

PERFORMANCE COMPARISON:

	Existing	**Proposed**
Min Input Power	4.736 W	0.0000 W
Max Input power	7.6304 W	1.7371 W
Avg Input power	6.2587 W	8.1984 W
Delay	0.95 sec	0.82 sec

This comparative study demonstrates the efficiency benefits of the proposed conditional boosting flip-flop method compared to existing approaches. By consuming less input power while maintaining functionality, the proposed method offers a promising solution for energy-efficient digital circuit design.

CONCLUSION:

For aggressive voltage scaling down to the near-threshold voltage region without severe performance degradation, a novel CBFF has been proposed. A pulse triggered FF design for low power applications using boost body driven scheme is presented in this project. Finally, a multibit flipflop concept is introduced with conditional boosting flipflop for efficient improvement of power area and delay.

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