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DESIGN OF TWO INTERLEAVED ERROR DETECTION AND CORRECTION USING HSIAO CODE AND CRC

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Abstract: A radiation-induced single-event upset (SEU) is a major disruption to electronics operating in satellites. If not rectified, a single-bit-error can become uncorrectable. There are several methods like Forward Error Correction Codes, Error Correction Codes, hamming codes, and many more from these methods, individual HSIAO, CRC, Hamming, BCH are used for error correction & detection. This project, presents two interleaved Double-Adjacent-Error Corrections (DAECs) for Error Detection and Correction (EDAC), using the Hsiao Code and Cyclic Redundancy Code (CRC). In this design single-bit-error, double-adjacent-bit-errors can be corrected and double bit-errors up to four-adjacent-bit-errors can be detected and corrected. The Hsiao Code EDAC has the best performance for speed, hardware requirement, and three- and four-bit-error detection. Its higher three- and four-bit error detection rates reduce the probability of an erroneous EDAC correction. The Hsiao code EDAC encoder design requires less bit – weight than the CRC EDAC, in contrast, has a higher error detection rate for both three- and four-bit errors. We used Verilog HDL and Xilinx Vivado to create and simulate designs.

Index Terms **– Hsiao Code, CRC, Hamming Code, BCH, EDAC**

I. INTRODUCTION

As a semiconductor's geometry gets smaller, the probability of a bit inversion in memory devices induced by external influences, such as an electrical surge and ionizing radiation increases. These anomalies interrupt the regular operation of an electronic device, causing mission failures. An Error Detection and Correction (EDAC) design mitigates these anomalies by detecting and correcting any bit inversions in memory devices such as the static memory (SRAM and SSRAM), and dynamic memory (SDRAM and DRAM). A safety-critical, fault-tolerant system requires a stringent specification for its EDACs, with minimizing erroneous correction rate as the goal. There are several prominent single error correction and double error detection (SEC-DED) EDACs proposed, such as the Hamming, Bose– Chaudhuri– Hocquenghem (BCH), and Hsiao Codes.

Error correcting codes have been widely applied to computer memory systems to enhance reliability. In particular, single bit error correcting and double bit error detecting (SEC-DED) codes have been successfully used in semiconductor memory systems organized in a one-bit-per-chip manner. This is because any failure in one chip can corrupt, at most, one bit per codeword in such systems. Recently, some systems adopt a b-bit-per-chip organization, where b >= 2. A chip failure in these systems causes the word read-out to have a b-bit block, called b-bit byte or simply byte, in error. Therefore, single b-bit byte error correcting and double b bit byte error detecting (SbEC-DbED) codes, capable of correcting all single b-bit byte errors and detecting double b-bit byte errors, have found applications in this kind of systems.

Among the predominant errors, however, are soft errors induced by D particles, which are said to be apt to manifest themselves as random bit errors still in byte organized systems. Cell failures also result in random bit errors. Therefore, designers of error control codes for byte organized memory systems should take into account two types of errors, byte errors and bit errors. Strictly speaking, bit errors are a class of byte errors which corrupt exactly one bit within a 2 byte, but we refer to such errors as bit errors, and the others as byte errors here. Since the vast majority of the errors in these systems are random bit errors, which may be caused by D particles or cell failures, it is more likely that a random bit error occurs lined up in a codeword with another existing byte error due to a chip failure than the case where as many as two chips fail to yield a double byte error. We refer to such an error, i.e., an error which corrupts both one byte and one bit in another byte, as a single byte plus single bit error

hereafter. In other words, single byte plus single bit errors are double byte errors such that at least one of the two-byte errors has Hamming weight one.

To improve the reliability of computer memories error correcting and/or error detecting codes have been commonly used. As the LSI technology moves towards higher levels of integration and packaging density the current bit-per-card organization may not be practical from a packaging and memory capacity standpoint and byte-per-card organization may become the general practice. In circuits with such an organization, physical failures will lead to bit as well as byte errors. The general situation with memories using byte-per-card organization. Though each card or circuit is shown to be b bits wide it is possible to have cards of different sizes. However, in this correspondence, for the sake of simplicity, let assume that all cards are b bits wide and it will refer to the collection of b bits as a byte. Depending on the location of a fault, a fault in a card may affect a single bit (these are called failures bit errors) or more than one bit in a byte (these are called failures byte errors). Known codes do not exist for correction and/or detection of several classes of potential failures in byte-per card organized digital systems. For example, in one application (involving a memory system) codes to correct single bit errors and detect single byte errors were required.

Certain known codes which correct both the bit and the byte errors could have been used but these codes would have required higher redundancy. In this correspondence we will derive a class of linear binary error-correcting codes to correct single bit errors and simultaneously detect single byte errors and double bit errors. The research work carried out here provided an insight into the development of error detection and correction systems. The research area of the Internet of Things in recent years has experienced growth and development in an interdisciplinary manner.

II. LITERATURE SURVEY

Babitha and Divya's single error correction, double error detection, double adjacent error correction, and triple adjacent error detection (SEC-DED-DAEC-TAED) EDAC used a modified Hamming Code. The state of the EDAC could not be verified since no validation results were presented. Jun and Lee proposed an SEC-DED-DAEC EDAC that requires the least redundancy bits relative to the other EDACs in their work. One limitation of having reduced redundancy bits is that the percentage of erroneous corrections is very high for the three- and four-bit-errors-there was no data to support the three- and four-bit-error detection capabilities. Hsiao proposed a class of optimal minimum odd-weighted column SEC-DED code known as the Hsiao Code [1] in the 1970s to improve the speed, cost, and reliability of the decoding logic.

Although several proposed SEC-DED EDACs exist in the literature, the Hsiao Code remains the most optimized SEC-DED EDAC. Others proposed various classes of SEC-DED codes, that can detect any number of errors in a single byte. These codes are known as single-error-correction double-error detection single-byte-error-detection (SEC-DED-SBD) codes. An EDAC with a double-error-correction and triple error-detection code may be used, at the cost of higher overhead of check-bits and more sophisticated hardware to implement the error correction and detection. This type of implementation may result in a slower EDAC that is not suitable in a high-performance system.

III. EXISTING METHOLOGY

In the existing method, individual Hsiao Code, CRC, Hamming, BCH are used for error correction & detection. the three Hsiao Code's rules and show how we can use them to create our Hsiao Code's EDAC H-matrix:

1. Every column should have an odd number of 1's; i.e., all column vectors are of odd-weights.
2. The total number of 1's in the H-matrix should be at a minimum.
3. The number of 1's in each row of the H-matrix should be made equal, or as close as possible, to the average number, i.e., the total number of 1's in the H-matrix divided by the number of rows.

Cyclic Redundancy Codes (CRCs) are conventional methods for error detection in networking and other applications. For networking, the interest is the Hamming Distance (HD), which is the least possible number of bit inversions in a message that can create an error undetectable by that message's CRC-based Frame Check Sequence. For example, if a CRC polynomial has an HD of 6 for a given network, all possible combinations of 1- to 5-bit errors (where a bit error is an inversion of a bit value) will be detected. At least one combination of 6 bits that, when corrupted within a message, is undetectable by that CRC.

IV. DISADVANTAGES OF EXISTING METHOLOGY

- Area efficiency is very less
- Error correcting and detecting rate is very low
- Performance is low

V. PROPOSED METHOLOGY

A. DESIGN OF HSIAO CODE's ENCODER MATRIX

The Hsiao Code implementation is straightforward. However, balancing the Hsiao Code's encoder matrix (also called the H-matrix) rows' bit-weights by hand is not an easy task. Instead, we created a C++ program, a Hsiao Code's matrix generator, to generate the H-matrices compliant with the three Hsiao Code's rules. We also created

another C++ program, a code generator, to take the generated matrix as the input and produce the Verilog code for the EDAC's encoder.

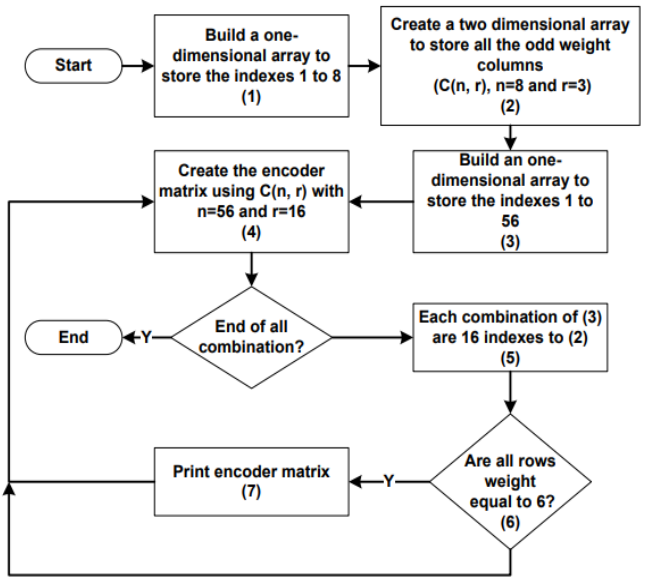

Fig. 1: Hsiao Code Encoder Matrix Generator

In the following, we introduce the three Hsiao Code's rules and show how we can use them to create our Hsiao Code's EDAC H-matrix:

1. Every column should have an odd number of 1's; i.e., all column vectors are of odd-weights. In the following, we use n to indicate the number of rows in the H-matrix, and r to indicate the number of 1's in each column, which must be an odd number.
   use the combination formula C (n, r) = ((n!)/ (r! (n-r)!)) to generate all possible odd-weighted columns.
2. The total number of 1's in the H-matrix should be at a minimum.
3. The number of 1's in each row of the H-matrix should be made equal, or as close as possible, to the average number, i.e., the total number of 1's in the H-matrix divided by the number of rows.

Based on the rules the rules above, we can design matrix generator in C++. Fig. 2 shows the flowchart of our generator.

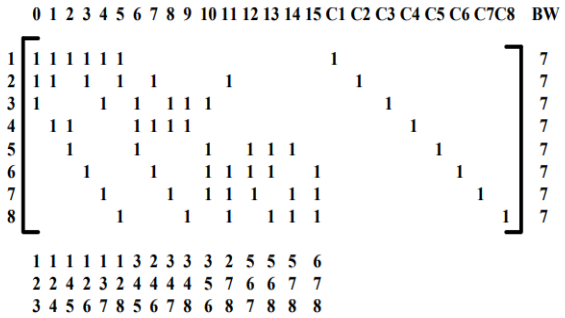

Fig. 2: This diagram shows the Hsiao Code's encoder matrix generated by the matrix generator.

B. DESIGN OF A CYCLIC REDUNDANCY CODE'S ENCODER MATRIX

Cyclic Redundancy Codes (CRCs) are conventional methods for error detection in networking and other applications. For networking, the interest is the Hamming Distance (HD), which is the least possible number of bit inversions in a message that can create an error undetectable by that message's CRC-based Frame Check Sequence. For example, if a CRC polynomial has an HD of 6 for a given network, all possible combinations of 1- to 5-bit errors (where a bit error is an inversion of a bit value) will be detected. At least one combination of 6 bits that, when corrupted within a message, is undetectable by that CRC.

We design our next EDAC based on a CRC polynomial to leverage the CRC detection capability. To increase the information rate, we compute the 16-bit message with an 8-bit CRC generator. To reduce the bit-weight in the encoder matrix, we set the CRC's seed value to zero. When a two-input XOR gate has an input equal to a logical zero, its output value is equal to the other input's value. Based on this Boolean state, we eliminate the XOR gates required for the seed value, thus reducing the bit-weight of our CRC matrix. We developed a CRC-based encoder matrix generator in C++ to generate our EDAC encoder matrix with these criteria.

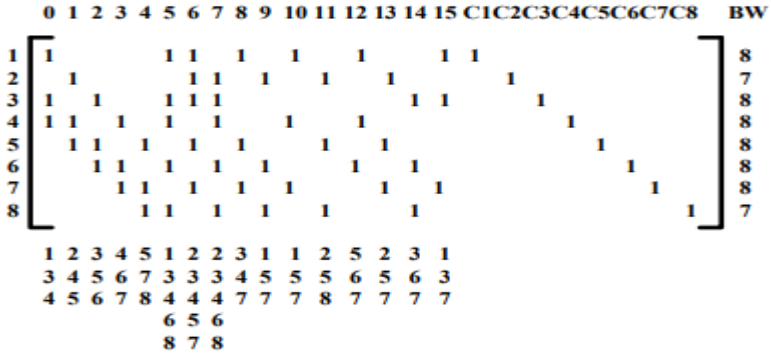

Fig. 3: this diagram shows the CRC's EDAC encoder matrix generated by our CRC matrix generator with polynomial = x^8 + x^3 + x^2 + 1.

C. Design an interleaved EDAC

Fig. 3 shows the architecture of our interleaved EDAC encoder design. Our EDAC uses two identical single error correction and double error detection (SEC-DED) EDACs configured as the even and odd encoders, syndromes, and decoders. For example, two Hsiao Code encoder matrices generated, or two CRC encoder matrices generated in can be used in Fig. 3. As the two identical encoders. This configuration improves the error correction and detection rates. For example, if a double-bit error has one error occurring on an even-bit, and the other on an odd-bit of a codeword, this error can be corrected. Verilog code of the interleaved even and odd encoders, an equivalent to the diagram shown in Fig. 3.

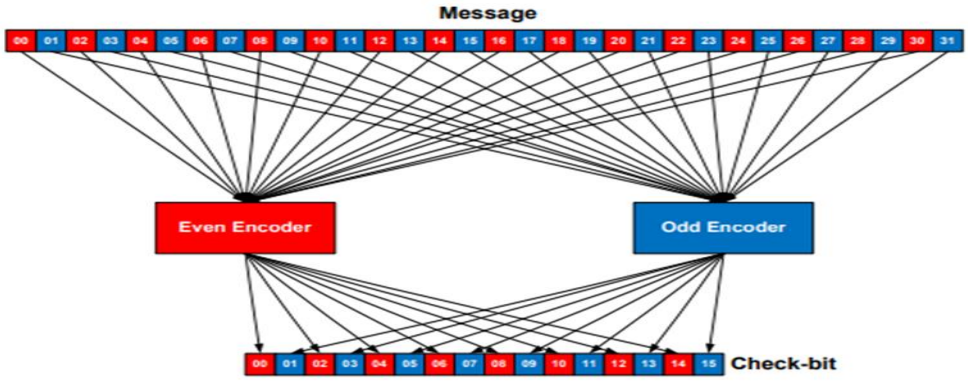

Fig. 4: Interleaved EDAC's encoder connection

EDAC uses two identical single error correction and double error detection (SEC-DED) EDACs configured as the even and odd encoders, syndromes, and decoders. For example, two Hsiao Code encoder matrices generated in existing, or two CRC encoder matrices generated in existing can be used in Fig. 8 as the two identical encoders. This configuration improves the error correction and detection rates. For example, if a double-bit error has one error occurring on an even-bit, and the other on an odd-bit of a codeword, this error can be corrected. In this proposed method is a combination of Hsiao code and CRC. By combining both the methods with the help of interleaving process. Fig. 12 shows the error detection and correction metrics of our EDAC designs (Hsiao Code and CRC). Our EDACs can correct all single-bit-errors. For double-bit-errors, our EDACs can correct all the double-adjacent-bit-errors. Additionally, double-bit-errors have one error occurring on an even-bit and the other on an odd-bit of a codeword (see Fig. 8, "Double bit-error 100% correctable) can be corrected. Since our EDAC is based on single-error-correction and double-error detection, our design can also detect all the remaining combinations of double-bit-errors (see Fig. 8, "Double-bit error 100% Detectable"). All three-bit-errors that are detectable, i.e., when two errors occur on two odd-bits and one on an even-bit of a codeword, and vice versa, are detected by our EDAC. Our EDAC can also detect up to four-adjacent-bit errors. For other detection rate capabilities, see Fig. 1

Types of Errors	Codeword		Description
	Even Bits	Odd Bits	
Single-bit Error	One Error Bits		100% Correctable
		One Error Bits	
Double-bit Errors	One Error Bits	One Error Bits	
	Two Error Bits		100% Detectable
		Two Error Bits	
Three-bit Errors	Two Error Bits	One Error Bits	
	One Error Bits	Two Error Bits	
	Three Error Bits		100% Detectable
		Three Error Bits	
Four-bit Errors	Two Error Bits	Two Error Bits	100% Detectable
	One Error Bits	Three Error Bit	100% Detectable
	Three Error Bits	One Error Bits	
	Four Error Bits		

		Four Error Bits	

Table. 1: The correctable and detectable errors of EDAC design

VI. RESULTS AND DISCUSSION

Simulation Results of Encoder

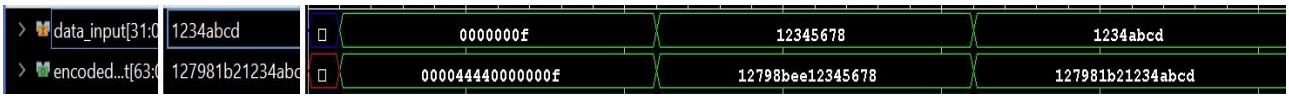

Fig. 5: Encoded Data

Simulation results of decoder

Fig. 6: Decoded Data

Schematic

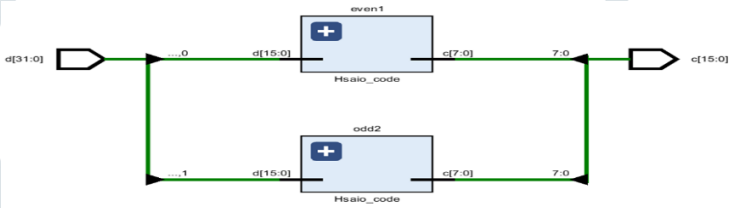

Fig. 7: RTL Schematic

Maximum Error Correcting Codes

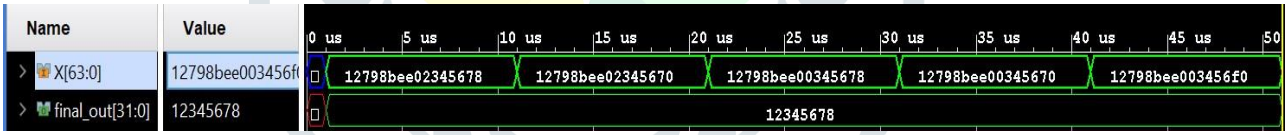

Fig. 8: Maximum Errors corrected

Reports of Area, Power, Delay

	Area (LUT's)	Power (W)	Delay (ns)
Interleaved_enc1	16	13.676	5.231
Interleaved_enc2	22	14.389	5.815

Table. 2: Area, Power, Report

Report of Utilization Board

Resource	Utilization	Available	Utilization %
LUT	16	20800	0.08
IO	48	106	45.28

Table. 3: Zed Board Utilization

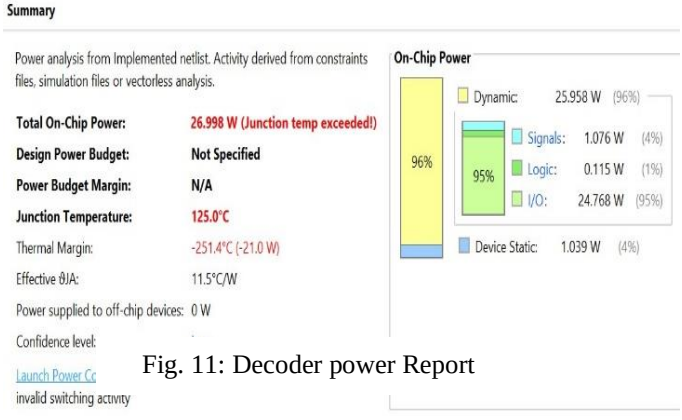

Fig. 11: Decoder power Report

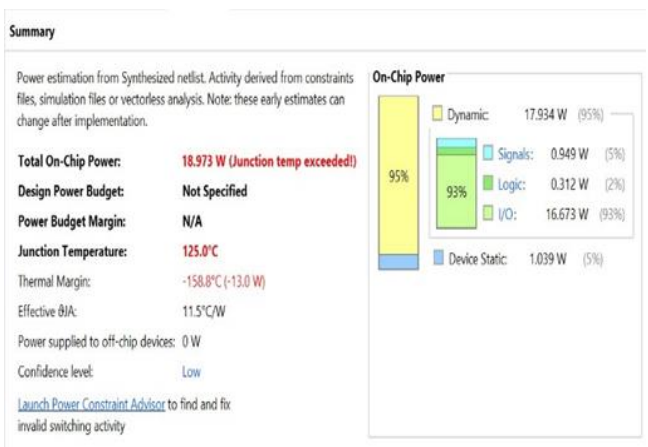

Fig. 9: Power Report of Encoder

Fig.10: Power Report of Decoder

VII. CONCLUSION

In this project, two interleaved Double-Adjacent-Error-Correction (DAEC) EDACs can correct single-bit-errors, double adjacent-bit-errors, and double-bit-errors that one error occurs on an even-bit and the other on an odd-bit of a codeword. For error detection, our EDACs can detect up to four-adjacent-bit errors. The detection rates of three-bit-errors are also improved compared to the individual (24,16) EDACs. Both the Hsiao Code and CRC-based EDAC approaches show promising results with minimum hardware requirements. The Hsiao code and CRC for both EDAC can correct 100% of the single-bit-error, double-Adjacent-bit-errors and up to four bits can detect and correct. The Hsiao Code EDAC encoder design requires Less bit weight than the CRC EDAC, which is an attribute of a high-speed EDAC Since the maximum bit-weight per row is low (six for Hsiao Code and seven for CRC), our EDACs are suitable in a high-performance computing system. Since commercial memory devices come in this format, our codeword-storage designs work well with such devices

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