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Low Power and Delay VLSI Architecture for Reversible Radix-2 FFT Algorithm using Folding Technique and Reversible Gates

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Abstract : The low power consumption and delay are essential parameter in implementing performance oriented VLSI Application .“ Low power and delay VLSI Architecture for Reversible Radix-2 FFT Algorithm using Folding Technique and Reversible Gate " introduces a new methodology for implementing the Fast Fourier Transform (FFT) algorithm . It is proposed to achieve low power delay by using FFT a Radix-2 Multi-way Delay commutate R2MDC FFT recurrence change method, created through the Exceptionally Large Scale Integration System structure condition This method is proposed to reduce power delay and increase efficiency, key parameters in VLSI design. The FFT algorithm is the crucial building block in this work. This technique concludes by stating that the proposed methodology can contribute to the creation of more efficient circuits, thereby helping to address the growing demand for power-efficient devices in today's electronic era. This results leads to significant improvements in the performance of various applications of VLSI.

1. INTRODUCTION

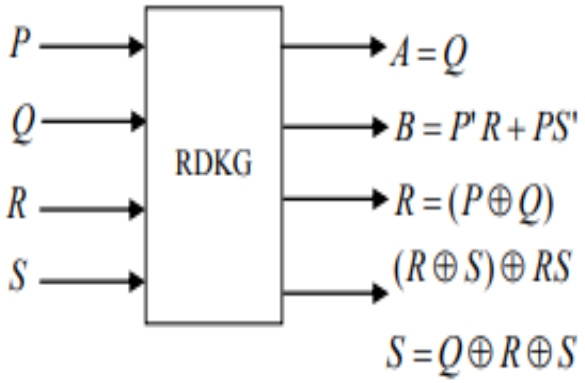
The field of digital signal processing (DSP) has become increasingly critical in modern communication systems, particularly in wireless communications. A fundamental technique used in DSP is the Fast Fourier Transform (FFT) algorithm, which transforms a sequence of complex numbers into magnitude and phase spectrum. The radix-2 FFT algorithm, due to its simplicity and efficiency, is widely used in digital signal processing. However, the implementation of radix-2 FFT in VLSI (Very Large Scale Integration) circuits faces challenges such as high hardware complexity and power consumption. To address these issues, we propose an area-efficient VLSI architecture for reversible radix-2 FFT algorithm using folding technique and reversible gate. Folding technique, proposed by Cooley and Tukey, is employed to further reduce hardware complexity. Recursively divides input data into smaller segments, reducing the number of multiplications required .Reversible logic gates offer the potential for substantial power savings in FFT implementations. Reduced hardware complexity contributes to more streamlined and efficient VLSI circuits. However, most of these studies focus on the use of different multiplication techniques or parallelism strategies, without considering the use of reversible logic gates. This paper aims to explore the use of reversible logic gates in the implementation of radix-2 FFT algorithm, which could potentially reduce both the hardware complexity and power consumption.

2. Literature review

The Fast Fourier Transform (FFT) algorithm is a fundamental technique in digital signal processing, widely used in wireless communications, image processing, and other areas where data needs to be transformed into frequency domain representation. However, the traditional FFT algorithms often suffer from high power consumption and area complexity, posing significant challenges for their implementation in VLSI circuits. Various approaches have been proposed to enhance the power efficiency and area efficiency of FFT algorithms. For instance, one strategy involves the use of decomposition techniques, which aim to minimize redundancies in intermediate stages of FFT. For instance, one strategy involves the use of decomposition techniques, which aim to minimize redundancies in intermediate stages of FFT.While various strategies have been proposed to enhance the power efficiency and area efficiency of FFT algorithms, a significant gap remains in integrating decomposition techniques and reconfigurable complex multipliers in a single FFT architecture

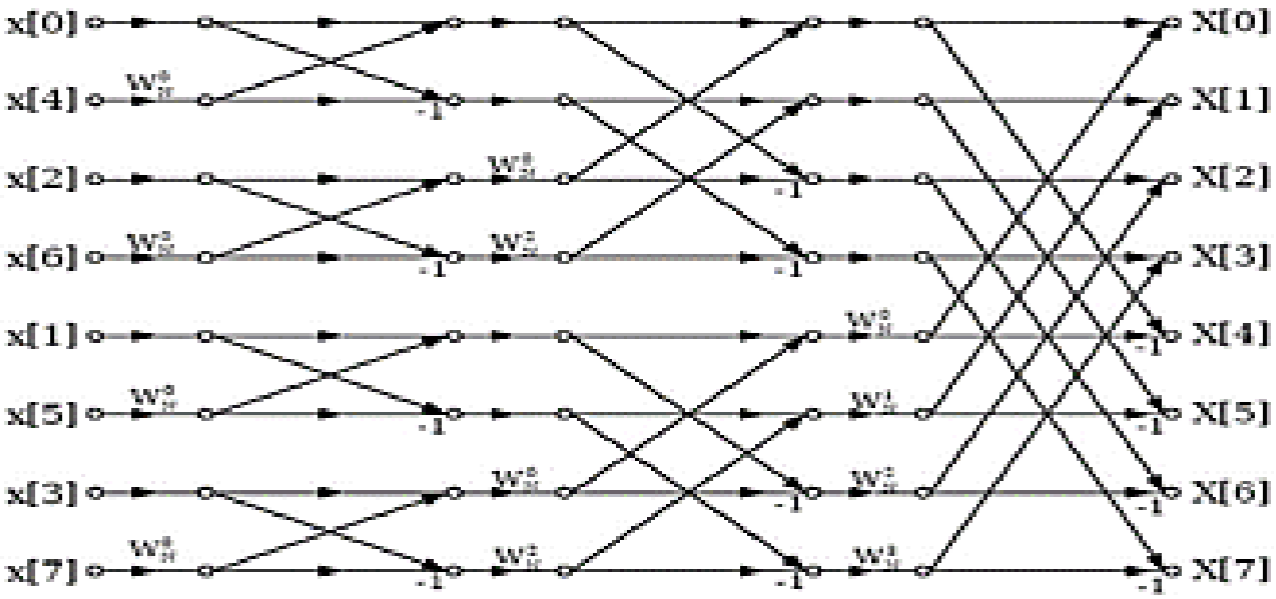
3. Existing method

The previous methods presents an innovative methodology for implementing the Fast Fourier Transform (FFT) algorithm using a Radix-2 Multi-way Delay commutate (R2MDC) FFT recurrence change method within the Exceptionally Large Scale Integration System structure condition. The aim is to reduce power consumption and enhance efficiency, critical parameters in VLSI design. The FFT algorithm is significant in digital signal processing and wireless communication frameworks, forming a fundamental role in many Digital Signal Processing (DSP) projects. It is a crucial building block for wireless communications, especially in symmetric frequency division multiplexing-based communication frameworks like 4G networks. A 4-bit full subtractor/adder is designed using a DKG Gate, where the fourth input determines whether the output is an adder or a subtraction. This design ensures versatility in computation for both addition and subtraction operations.



DKG Gate

The FFT algorithm implemented uses an 8-point FFT, which is crucial in converting signals between time/space domains and frequency domains. Proposal includes an 8-point Decimation In Time (DIT) FFT implementation using radix-2 termite approach.

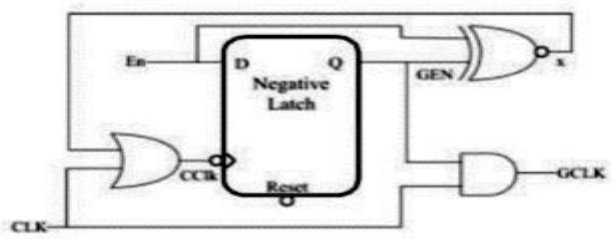


8-point DIT-FFT Radix-2 Termite

4. Proposed Method

The 32-bit FFT (Fast Fourier Transform) is an extension of the FFT algorithm capable of processing larger data sets, specifically 32-point sequences. It is a key component in digital signal processing and wireless communication systems, where it's used to transform signals between time or space domains and the frequency domain. The 32-bit FFT processor is designed to efficiently compute FFTs using a novel pipelined architecture that incorporates a Single-Path Delay Commutator Processing Element (SDC PE) to save on complex adders. The design is optimized for power efficiency and high performance, which are critical in VLSI systems. The 32-bit FFT algorithm follows the radix-2 Decimation-In-Frequency (DIF) approach, which recursively divides the input data into smaller DFTs and combines them. The algorithm is broken down into stages, each reducing the data size by half. The design includes efficient hardware for complex arithmetic operations and memory units for storing intermediate results. The 32-bit FFT processor uses Designated Karnaugh Gate (DKG Gate) and Peres and TR gates to implement the FFT algorithm. This ensures versatility in computation for both addition and subtraction operations. The processor is designed to handle the increased complexity of a 32-bit system, which requires careful control signal handling and synchronization.

The performance is compared with previous designs to evaluate its efficiency and power consumption. In addition to the 32-bit FFT, the methodology can be extended to even larger bit widths. This scalability demonstrates the versatility of the proposed methodology, which can be adapted to handle higher precision requirements and larger data sets.



Clock Gating

Clock gating is an important technique in the design of VLSI systems to reduce dynamic power consumption. It selectively turns off the clock to certain parts of the digital design when they are not needed, which minimizes the delay caused by the clock signal and reduces the power dissipation in the system.

5. Tools used

1. Verilog HDL
2. Xilinx Vivado Simulator

6. Results

1. FFT_32 Delay

Name	Slack ^1	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement
Path 1	∞	10	11	7	in12[0]	y_real_10_reg[7]/D	7.859	4.376	3.483	∞
Path 2	∞	10	11	7	in28[0]	y_real_12_reg[7]/D	7.859	4.376	3.483	∞
Path 3	∞	10	11	7	in4[0]	y_real_14_reg[7]/D	7.859	4.376	3.483	∞
Path 4	∞	10	11	7	in20[0]	y_real_8_reg[7]/D	7.859	4.376	3.483	∞
Path 5	∞	10	11	5	in29[1]	y_real_15_reg[7]/D	7.855	4.356	3.499	∞
Path 6	∞	10	11	5	in21[1]	y_real_1_reg[7]/D	7.855	4.356	3.499	∞
Path 7	∞	10	11	5	in5[1]	y_real_3_reg[7]/D	7.855	4.356	3.499	∞
Path 8	∞	10	11	5	in13[1]	y_real_5_reg[7]/D	7.855	4.356	3.499	∞
Path 9	∞	10	11	5	in21[0]	y_real_16_reg[7]/D	7.852	4.376	3.476	∞
Path 10	∞	10	11	5	in5[0]	y_real_18_reg[7]/D	7.852	4.376	3.476	∞

2. FFT_32 utilization:

Resource	Utilization	Available	Utilization %
LUT	1116	53200	2.10
FF	256	106400	0.24
IO	513	200	256.50

7. CONCLUSION

This technique presents a new methodology for implementing the Fast Fourier Transform (FFT) algorithm using a Radix-2 Multi-way Delay commutate (R2MDC) FFT recurrence change method. The highlight of the technique is optimizing the power consumption of complex design systems, focusing on heat dissipation and the reduction of power. This method concludes by comparing the performance of reversible-based FFT architectures with Peres and DKG gate, showing that the DKG gate-based design consumes less memory but the Peres and TR gate-based design offers better performance in terms of slices, LUTs, and power.

8. REFERENCES

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