



Investigation on mitigation of common mode voltage in three phase two level inverter

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Abstract— The abstract introduces a research paper that conducts a comparative analysis of three-phase two-level inverters, aiming to provide a comprehensive understanding of their characteristics and effects on common-mode voltage and common-mode current. The paper delves into a detailed examination of various three-phase two-level inverter configurations, specifically focusing on the conventional two-level inverter, the two-level H7 inverter, and the two-level H10 inverter. The analysis encompasses an in-depth exploration of how each inverter type influences common-mode voltage and common-mode current. These aspects are of paramount importance in power electronics, as they significantly impact the performance, efficiency, and reliability of electrical systems. To facilitate the comparative analysis, the paper employs simulation techniques for each inverter configuration. Simulation is a crucial tool in the realm of power systems research, enabling researchers to model and observe the dynamic behavior of different components under diverse operating conditions. By employing simulations, the study aims to validate and substantiate its findings, offering a robust foundation for the statistical comparison of the three-phase two-level inverters under consideration. The utilization of simulation data enhances the reliability and comprehensiveness of the analysis, contributing to a more nuanced understanding of the performance characteristics of each inverter type in practical applications.

Keywords— *Two-level inverter, Common mode voltage reduction, common mode current reduction.*

I. INTRODUCTION

In contemporary applications, multi-level inverters [1-5] are gaining traction in electric drives and renewable energy systems due to their numerous advantages over conventional two-level inverters. These advantages include lower dv/dt stress, decreased total harmonic distortion (THD), and reduced common mode current. Despite the plethora of proposed multi-level inverter designs in literature, three primary topologies have emerged as basic and popular

choices: (1) the neutral point clamped multi-level inverter, (2) the cascaded H bridge multi-level inverter, and (3) the flying capacitor multi-level inverter. However, each of these topologies presents its own set of limitations. The neutral point clamped multi-level inverter [6] is susceptible to issues such as neutral point fluctuations, while the cascaded H bridge multi-level inverter [7] necessitates independent DC sources. On the other hand, the flying capacitor multi-level inverter [8] encounters challenges related to the charging of the flying capacitor, adding complexity to its operation and control.

This research paper embarks on a comprehensive exploration of three-phase two-level inverters, aiming to provide a detailed comparative analysis that unveils their distinctive performance characteristics. Inverters are essential elements in power conversion systems, and understanding their behavior under different operating conditions is crucial for optimizing energy efficiency and system reliability.

The study delves into the intricacies of three specific types of three-phase two-level inverters: the conventional two-level inverter, the two-level H7 inverter, and the two-level H10 inverter. Each of these configurations represents a unique technological approach, offering a spectrum of advantages and challenges. Through a rigorous examination, this research endeavors to shed light on their individual merits, thereby aiding researchers, engineers, and practitioners in making informed decisions regarding their implementation in diverse applications.

The comparative analysis extends beyond a conventional investigation, encompassing an exploration of the impact of these inverters on common-mode voltage and common-mode current. These aspects are critical in assessing the overall electromagnetic compatibility and performance stability of power electronic systems.

To establish the credibility of our findings, extensive simulations are conducted for each inverter configuration. The use of simulation tools allows for a thorough evaluation of the inverters' dynamic behavior under varying load conditions, providing valuable insights into their transient and steady-state performance.

In conclusion, this research not only contributes to the current body of knowledge in power electronics but also serves as a practical guide for engineers and researchers seeking to optimize the performance of three-phase two-level inverters in real-world applications. As the demand for efficient and reliable power conversion systems continues to grow, a nuanced understanding of the comparative advantages and limitations of these inverters becomes indispensable for advancing the state-of-art in power electronics.

II. CONVENTIONAL TWO LEVEL INVERTER

The conventional 2-level inverter stands as a cornerstone in power electronics, representing a fundamental architecture for converting direct current (DC) into alternating current (AC). In the realm of electrical systems, this inverter configuration has long been a workhorse, providing a reliable and straightforward solution for a myriad of applications ranging from motor drives to renewable energy systems. At its core, the conventional two-level inverter employs a basic switching scheme, utilizing two voltage levels to generate the desired AC waveform. Despite its simplicity, this inverter design has proven to be robust and versatile, serving as a benchmark against which newer and more sophisticated technologies are often compared. In this introductory exploration, we delve into the key features, operational principles, and historical significance of the conventional two-level inverter, laying the foundation for a deeper understanding of its role in contemporary power electronics. Following figures Fig.1-4 are the schematic diagram of conventional 2-level inverter, pole voltages of 3 phase 2 level inverter, phase voltage of conventional 3 phase 2 level inverter and common mode voltage and common mode current CMC of conventional 3 phase 2 level inverter respectively.

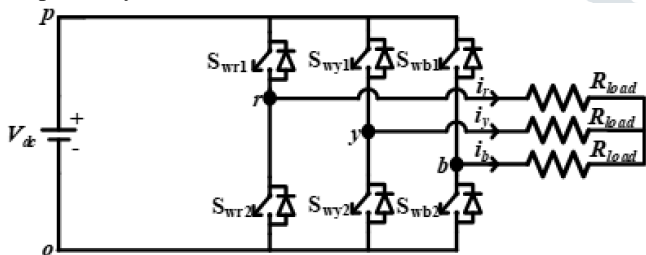


Fig.1 Schematic diagram of conventional three phase two level inverter

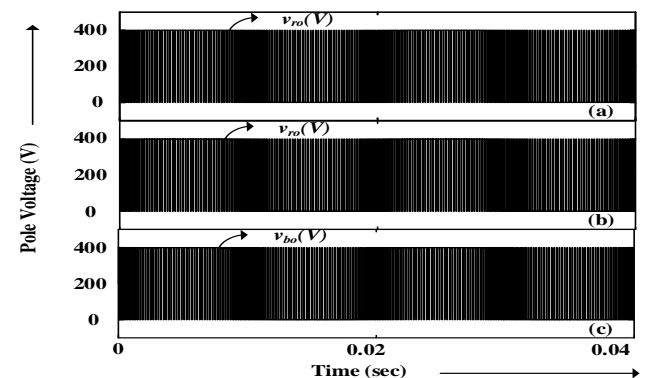


Fig.2 Pole voltages of conventional three phase two level inverter

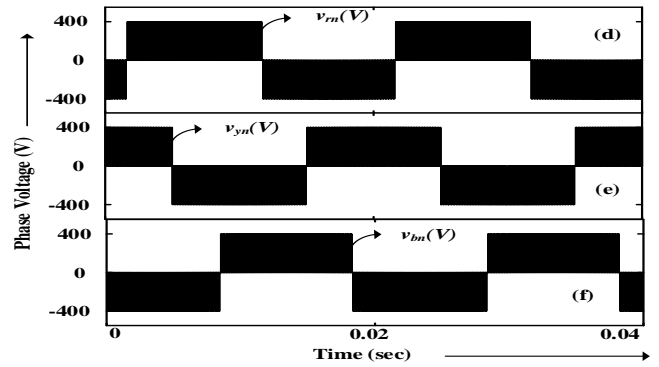


Fig.3 Phase voltages of conventional three phase two level inverter.

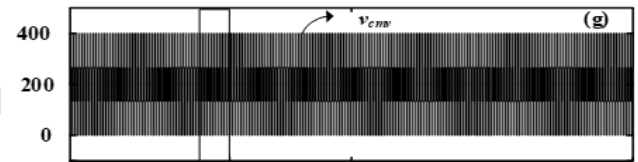


Fig.4a common mode voltage of conventional three phase two level inverter

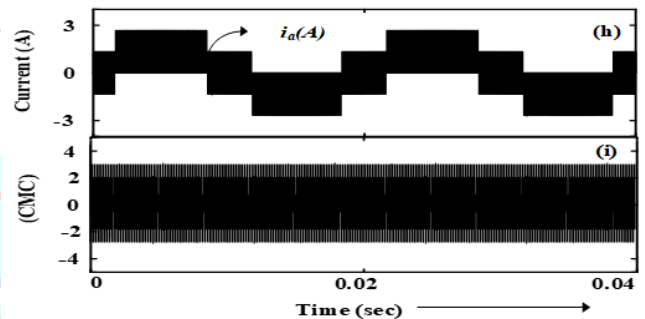


Fig.4b common mode current of conventional three phase two level inverter.

III. TWO LEVELH7 INVERTER

The two-level H7 inverter represents a notable advancement in power electronics, introducing a distinctive topology that addresses certain limitations of conventional two-level inverters. This innovative design, characterized by the integration of an H-bridge configuration with seven voltage levels, seeks to enhance the performance and efficiency of power conversion systems. Unlike its simpler counterpart, the H7 inverter leverages additional voltage levels to achieve improved waveform quality, reduced harmonic distortion, and enhanced control flexibility. In this introductory overview, we explore the underlying principles and unique features of the two-level H7 inverter, shedding light on its potential applications and contributions to the evolving landscape of modern power electronics.

Fig. 5-9 are the schematic diagram of two-level H7 inverter, pole voltages of three phase two level inverter, phase voltage of conventional three phase two level inverter and common mode voltage and common mode current of conventional three phase two level inverter respectively.

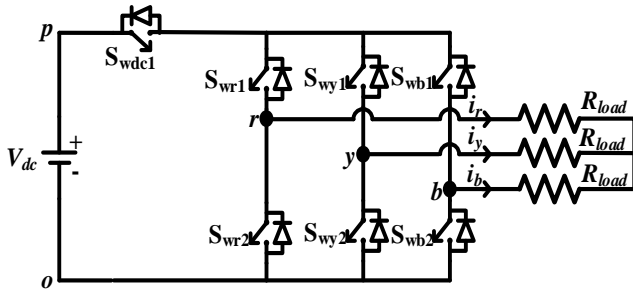


Fig.5 Schematic diagram of three phase two level H7 inverter

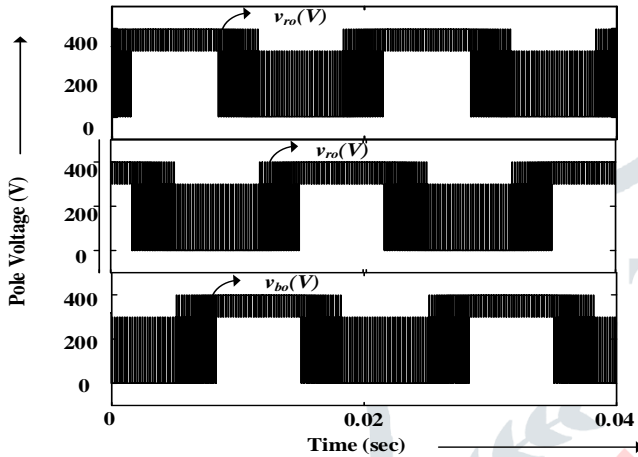


Fig.6 Pole voltages of three phase two level H7 inverter

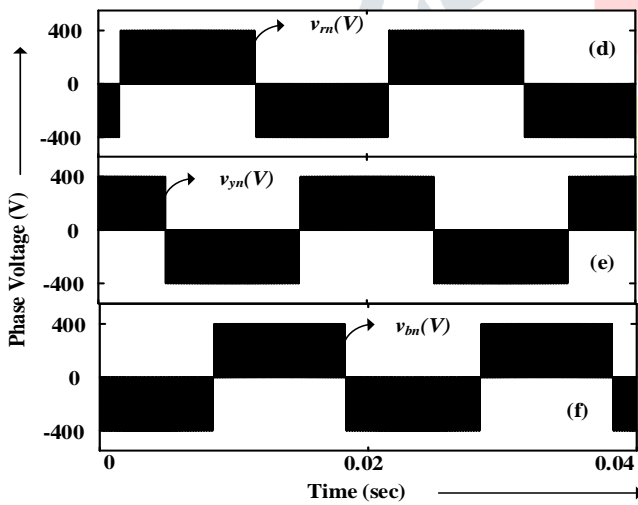


Fig.7 Phase voltages of three phase two level H7 inverter

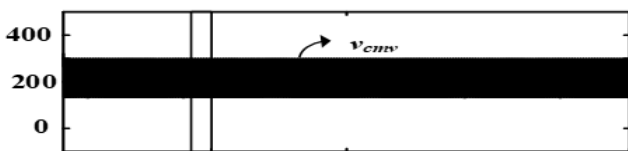


Fig.8 common mode voltage of three phase two level H7 inverter

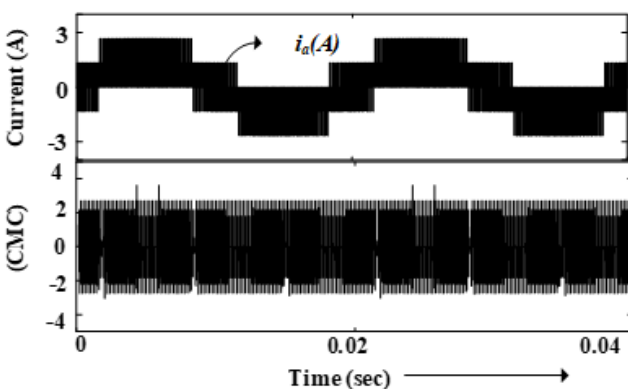


Fig.9 common mode Current of three phase two level H7 inverter

IV. HYBRID TWO LEVEL INVERTER

The diagram in Figure 10 outlines the circuit topology of the hybrid NPC inverter, which includes a flying capacitor (FC) leg along with three NPC legs. In this configuration, each leg is equipped with four switching devices, except for the FC leg, which is distinguished by its connection to a flying capacitor instead of two clamping diodes [3]. This setup introduces a novel tertiary component into the inverter design.

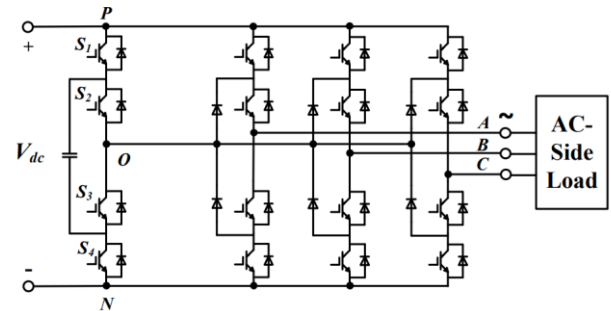


Fig.10 Schematic diagram of three phase two level Hybrid inverter

A. CMV MITIGATION IN FULL MODULATION RATIO

The common-mode voltage (CMV), symbolized as V_{cm} in equation (1), is a crucial parameter in a three-phase converter system, determined by the output terminal voltages V_a , V_b , and V_c of the three-phase NPC legs. CMV is a significant source of common-mode electromagnetic interference (EMI), leading to the generation of leakage current, also known as common-mode current (CMC), within a common-mode loop that often includes parasitic capacitances. To simplify, let's designate C_P as the lumped parasitic capacitance. The time-varying voltage across C_P triggers the formation of CMC through the parasitic capacitor, as outlined within the system [3]. Understanding and mitigating the effects of CMV and CMC are essential in designing robust and efficient converter systems for various applications.

$$V_{CM} = \frac{V_a + V_b + V_c}{3}$$

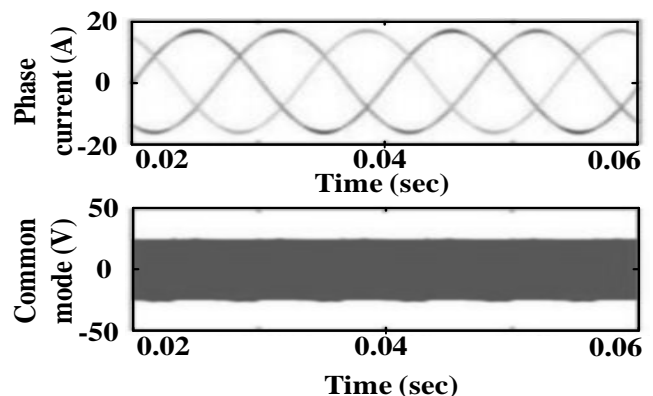


Fig.11 (a) phase current of three phase two level hybrid inverter (b) common mode voltage (CMV) of three phase two level hybrid inverter

Fig. 10-11 are the schematic diagram of two-level hybrid

inverter, 11(a) phase current of three phase two level hybrid inverter, 11(b) common mode voltage of three phase two level hybrid inverter and Fig.2 represent common mode current of three phase two level hybrid inverter.

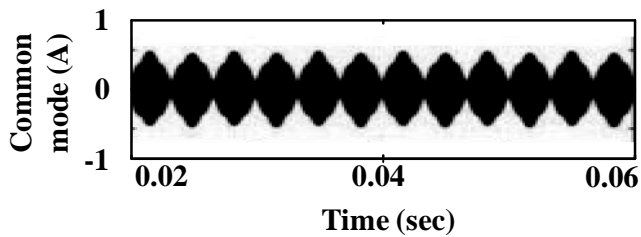


Fig. 12 common mode current (CMC) of three phase two level hybrid inverter

V. CONCLUSION

In conclusion, this research paper conducted a comprehensive comparative analysis of three-phase two-level inverters featuring distinct topologies. The study juxtaposed three different models, namely the conventional two-level inverter, the three-phase two-level H7 inverter, and the hybrid two-level inverter. The findings, derived from simulation results, shed light on the relative performance and characteristics of each inverter model. This comparative analysis contributes valuable insights to the understanding of the strengths and limitations of various two-level inverter configurations, thereby aiding researchers and practitioners in making informed decisions regarding the optimal choice for specific applications in power systems.

c	Conventional 2-level inverter	2 level H7 inverter	Hybrid 2 level inverter
No of switches used	6	7	16
number of voltage source	1	1	1
Passive components count	0	0	3
Input DC Voltage	400V	400V	150
Switching frequency	2Khz	2Khz	20Khz
Rload	100 ohms	100 ohms	5 ohms
Frequency of operation	50Hz	50Hz	50Hz
Common mode voltage range	400V	166.66V	60V
Common mode voltage percentage	0%	41.50%	40.00%
Common mode current	3.0A	2.15A	0.5A

Based on the above topologies discussed and verification of their analytical waveform, in summary, the choice of inverter depends on specific application requirements. The Conventional and H7 inverters provide simplicity and low common mode voltage, while the Hybrid Inverter, with its higher complexity, offers advantages in terms of reduced input voltage, higher switching frequency, and lower common mode current. The selection should be based on a careful consideration of the trade-offs between simplicity and performance.

REFERENCES

- [1] J. Huang and H. Shi, "Reducing the Common-Mode Voltage through Carrier Peak Position Modulation in an SPWM Three-Phase Inverter," in *IEEE Transactions on Power Electronics*, vol. 29, no. 9, pp. 4490-4495, Sept. 2014, doi: 10.1109/TPEL.2014.2303897.
- [2] V. Anand, V. Singh and J. S. Mohamed Ali, "Dual Boost Five-Level Switched-Capacitor Inverter With Common Ground," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 70, no. 2, pp. 556-560, Feb. 2023.
- [3] X. Zhao, D. Jiang, W. Sun and J. Gao, "Common-Mode Voltage Mitigation for Three-Phase Hybrid NPC Inverter with Flying-Capacitor Leg," 2022 International Power Electronics Conference (IPEC-Himeji 2022- ECCE Asia), Himeji, Japan, 2022, pp. 1070-1075, doi: 10.23919/IPEC-Himeji2022-ECCE53331.2022.9807117.
- [4] A. J. Passos Nascimento et al., "Bidirectional Isolated Asymmetrical Multilevel Inverter," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 70, no. 1, pp. 151-155, Jan. 2023.
- [5] M. Sarebanzadeh et al., "A 15-Level Switched-Capacitor Multilevel Inverter Structure With Self-Balancing Capacitor," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 69, no. 3, pp. 1477-1481, March 2022.
- [6] B. S. Naik, Y. Suresh, J. Venkataramanaiah and A. K. Panda, "A Hybrid Nine-Level Inverter Topology With Boosting Capability and Reduced Component Count," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 68, no. 1, pp. 316-320, Jan. 2021.
- [7] T. Roy, M. W. Tesfay, B. Nayak and C. K. Panigrahi, "A 7-Level Switched Capacitor Multilevel Inverter With Reduced Switches and Voltage Stresses," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 68, no. 12, pp. 3587-3591, Dec. 2021.
- [8] N. Celanovic and D. Boroyevich, "A comprehensive study of neutral-point voltage balancing problem in three-level neutral-point-clamped voltage source PWM inverters," *IEEE Transactions on Power Electronics*, vol. 15, no. 2, pp. 242-249, March 2000.
- [9] P. Cortés, A. Wilson, S. Kouro, J. Rodriguez and H. Abu-Rub, "Model Predictive Control of Multilevel Cascaded H-Bridge Inverters," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 8, pp. 2691-2699, Aug. 2010.
- [10] A. Abdelhakim, P. Mattavelli and G. Spiazzi, "Three-Phase Three-Level Flying Capacitors Split-Source Inverters: Analysis and Modulation," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 6, pp. 4571-4580, June 2017.
- [11] T. K. S. Freddy, N. A. Rahim, W. -P. Hew and H. S. Che, "Modulation Techniques to Reduce Leakage Current in Three-Phase Transformerless H7 Photovoltaic Inverter," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 1, pp. 322-331, Jan. 2015.
- [12] Z. Dong, H. Wen, T. Wang, B. Zhang, Z. Song and C. Liu, "Common-Mode Voltage Reduction-Based Space Vector Modulation Strategy for Three-Phase Two-Level Inverter with Delta-Connected Loads," 2023 IEEE 32nd International Symposium on Industrial Electronics (ISIE), Helsinki, Finland, 2023, pp. 1-6, doi: 10.1109/ISIE51358.2023.10228124.
- [13] A. Promyoo and S. Suwankawin, "A Common-Mode Voltage Reduction for Two-Stage Three-Phase Transformerless PV Inverters," 2018 International Power Electronics Conference (IPEC-Niigata 2018-ECCE Asia), Niigata, Japan, 2018, pp. 2871-2876.
- [14] T. Kato, K. Inoue, K. Takano and A. Aki, "Common-mode voltage reduction with two-phase modulation in three-level PWM inverter," 2013 IEEE Energy Conversion Congress and Exposition, Denver, CO, USA, 2013, pp. 5349-5354, doi: 10.1109/ECCE.2013.6647426.
- [15] A. Videt, M. Messaoudi, N. Idir, H. Boulharts and H. Vang, "PWM strategy for common-mode voltage reduction in three-phase variable-speed drives with active front end," 2015 5th International Electric Drives Production Conference (EDPC), Nuremberg, Germany, 2015, pp. 1-7, doi: 10.1109/EDPC.2015.7323208.

- [16] Sibi Raj P. M. and Rashmi M.R., "Reduction of common mode voltage in three phase inverter," 2015 International Conference on Technological Advancements in Power and Energy (TAP Energy), Kollam, India, 2015, pp. 244-248, doi: 10.1109/TAPENERGY.2015.7229625.
- [17] S. -H. Lee, J. -H. Jung, S. -I. Hwnag, J. -M. Kim and H. Cho, "Common Mode Voltage Reduction Method for H7 Inverter Using DPWM Offset Based Modulation Technique," 2018 IEEE Energy Conversion Congress and Exposition (ECCE), Portland, OR, USA, 2018, pp. 1790-1795, doi: 10.1109/ECCE.2018.8557811.
- [18] Narendra Kumar G and S. Srinivas, "Carrier phase shifted SPWM for CMV reduction in a three-level inverter using open-end winding induction motor drive," 2016 IEEE Region 10 Conference (TENCON), Singapore, 2016, pp. 707-712, doi: 10.1109/TENCON.2016.7848094.
- [19] X. Deng, H. Wang, X. Zhu, H. Wang, W. Zhang and X. Yue, "Common-Mode Voltage Reduction and Neutral-Point Voltage Control Using Space Vector Modulation for Coupled Ten-Switch Three-Phase Three-Level Inverter," in IEEE Transactions on Power Electronics, vol. 37, no. 6, pp. 6397-6411, June 2022, doi: 10.1109/TPEL.2021.3133714.
- [20] S. M. Maaz and D. -C. Lee, "Common-Mode Voltage Mitigation for Dual Three-Phase Three-Level ANPC Inverters Using Dynamic Phase-Shift PWM," in IEEE Access, vol. 11, pp. 104234-104243, 2023, doi: 10.1109/ACCESS.2023.3318124.
- T. -T. Tran, M. -K. Nguyen, T. -D. Duong, J. -H. Choi, Y. -C. Lim and F. Zare, "A Switched-Capacitor-Voltage-Doubler Based Boost Inverter for Common-Mode Voltage Reduction," in IEEE Access, vol. 7, pp. 98618-98629, 2019, doi: 10.1109/ACCESS.2019.2930122.

