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EXPLORING THE POTENTIAL OF OPEN-SOURCE RISC-V CORES FOR LOW-POWER IOT DEVICES

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Abstract : This research explores the potential of open source RISC-V processor cores for designing low-power IoT devices. RISC-V is an open source instruction set architecture (ISA), which offers flexibility and customization for IoT applications. This research investigates the performance of RISC-V in power saving techniques compared to traditional architectures. It presents case studies and analyses to demonstrate the RISC-V's effectiveness in various IoT scenarios, such as smart homes and wearable health monitoring. The results highlight the benefits and challenges of implementing RISC-V on IoT devices, and highlight its potential to optimise energy consumption and promote innovation in the IoT industry. Open-source RISC-V cores offer power efficiency and customization for IoT devices. They have advantages over traditional architectures such as low energy consumption, small size, high performance, and flexible security. The results of the research show that the RISC-V core can be customised to specific applications, increasing power efficiency. However, the legal, licensing and technical challenges of widespread adoption remain. Progress in reliable and safe execution, system-level use case support, and flexible hardware architectures can have a major impact on the future of IoT devices.

Key Words: RISC, Power saving techniques, Low-power IoT devices, Open-source processors.

I. INTRODUCTION

1.2 Introduction to IoT Devices and Their Significance

The Internet of Things (IoT) revolutionises technology by joining tangible goods like electronics and buildings through integrated electronics, software, sensors, and networking. IoT devices provide seamless interaction and data sharing with other devices and internet platforms, enabled by their intrinsic connectivity. Equipped with sensors, they record different environmental data and offer remote access and operation via internet-enabled programmes. IoT streamlines operations through real-time data analytics, enhancing decision-making processes. Its heterogeneity encompasses equipment from multiple manufacturers, each with distinct connection protocols. In smart homes, IoT offers automatic control of lighting, heating, and security, enhancing efficiency. Similarly, in urban contexts, IoT assists intelligent traffic management, infrastructure monitoring, and resource efficiency programmes. Industries benefit from IoT with real-time monitoring, predictive maintenance, and process optimization, decreasing operational costs. Healthcare utilises IoT-enabled wearables for remote patient monitoring and individualised therapy interventions. Agriculture sees developments with IoT-enabled sensors monitoring soil conditions and weather patterns, optimising cropping. Transportation benefits from networked autos and traffic control systems, boosting operational efficiency and safety standards.

1.2 Importance of low-power in IOT Consumption Devices

In the worldwide ecosystem of IoT devices, the necessity of low-power consumption stands as a key requirement for several main reasons. Firstly, a substantial fraction of IoT devices work within the limits of constrained power sources, often relying on battery power or energy harvesting techniques. This needs managing power utilisation to permit lengthy working durations without the regular requirement for battery replacements or recharge.

Moreover, the scalability and extensive deployment envisioned within the IoT ecosystem need an adherence to low-power standards. Envisaging billions of networked devices would be regarded as unfeasible if each device had large power requirements. Consequently, the adoption of low-power operation becomes crucial in supporting the scalable deployment of IoT devices across varied environments, spanning from home settings to industrial landscapes.

However, despite the acknowledged necessity of low-power consumption in the context of IoT, various challenges prevent its realisation. IoT devices sometimes battle with natural hardware limits, characterised by limited processor capabilities, memory, and energy resources, consequently hindering the application of advanced power management approaches. Furthermore, the diverse nature of IoT devices, each offering different power consumption profiles and optimization requisites, causes further issues. Dynamic workloads and climate situations further worsen these challenges, necessitating the adoption of adaptive power management systems. Additionally, the requirement of security and data processing engenders a conundrum whereby attempts to

fortify IoT devices and process data locally may unintentionally raise power consumption, therefore requiring a sensitive balance between security, performance, and energy efficiency.

In evaluating the effects of low-power consumption on the performance and longevity of IoT devices, various noticeable advantages occur. Foremost among these is the expansion of battery life and operational duration, enabling IoT devices to run for protracted durations on constrained power sources, hence lessening the requirement for regular maintenance interventions. This increase of operating lifetimes bodes well for the dependability and availability of IoT devices, particularly in scenarios defined by remote or inaccessible deployment sites. Furthermore, low-power IoT devices enable the discovery of novel use cases across multiple domains, including applications seeking extended autonomous operation or working inside resource-constrained environments. From an environmental aspect, the implementation of low-power principles delivers significant benefits, with reduced energy usage translating into diminished carbon footprints, thus increasing the general sustainability of IoT systems.

1.3 Overview of RISC-V Architecture

The RISC-V instruction set architecture (ISA) is gaining traction for its innovative advantages including low power consumption, affordability, and scalability. These attributes make it suitable for various applications, particularly in the Internet of Things (IoT) domain.

A key advantage of RISC-V is its open-source nature, enabling customization of security features at the hardware level, potentially extending the lifespan of specialized processors. A study exploring the RISC-V architecture with an extended instruction set for bit manipulation operations reported significant performance improvements, highlighting the potential of ISA extensions.

RISC-V's cost advantage stems from its open-source nature, eliminating licensing fees unlike proprietary architectures. This has attracted interest from those seeking to design their own chips.

Designed for versatility, RISC-V incorporates a common base set of instructions with optional extensions for various applications, from microcontrollers to server CPUs.

RISC-V's technological advantages, including low power consumption, scalability, and open-source nature, enable the development of adaptable and resilient processors. Research is ongoing to address security concerns, software support, and performance optimization. As RISC-V adoption grows, these advancements will be crucial for future development in this evolving field.

II. BACKGROUND

2.1 Evolution of IoT Devices and Architectures

The emergence of Internet of Things (IoT) devices and architectures has been defined by significant trends that have impacted the environment over time. In the early phases (1990s-2000s), the notion of IoT developed, picturing a connected society where everyday items communicate over the internet. Initial implementations focused on simple monitoring and control applications, employing proprietary protocols and hardware.

Subsequently, the growth of low-cost sensors, microcontrollers, and wireless networking technologies fuelled the broad adoption of IoT (2000s-2010s). Devices diversified throughout numerous fields, ranging from home automation to industrial monitoring and smart city infrastructure. This decade also seen the introduction of IoT platforms, such as Amazon Web Services (AWS) and Microsoft Azure, offering extensive cloud-based services for device administration and data processing.

Trends affecting the future of IoT designs include a shift toward edge computing, driven by the increasing power and ubiquity of IoT devices. Edge computing enables data processing closer to the data source, lowering latency and bandwidth needs. Additionally, there's an increasing emphasis on energy efficiency due to the battery-powered nature of many IoT devices.

Moreover, IoT systems are embracing heterogeneity, combining a combination of general-purpose computing, specialized hardware acceleration, and fast data transportation. This method maximises performance and energy efficiency, vital for different IoT applications. Security and resilience have also become key considerations, leading to the integration of sophisticated security measures in IoT designs.

To meet the issues provided by heterogeneity, scalability, security, and intelligence, numerous architectural frameworks and paradigms have been developed. These frameworks attempt to provide common interfaces, manage increasing data and connectivity needs, offer robust security and privacy, and enable intelligent and autonomous IoT systems.

2.2 Challenges in Designing Low-Power IoT Devices

Designing low-power IoT devices involves numerous key problems that affect their effectiveness and operation. Chief among these problems is the intrinsic power drain of IoT devices, especially during low-activity phases, due to constant power requirements for services like wireless transmission and wakeup word recognition. The expected scale of IoT exacerbates this difficulty, since even tiny power pulls might result in large energy usage. Furthermore, the siloed nature of IoT devices contributes to redundancy, increasing overall power usage.

Balancing the limited power and CPU capabilities of IoT devices with the need for appropriate performance creates another key difficulty. While developing memory technology and approximation computing approaches offer promising solutions, achieving appropriate computational capabilities while minimising power demand remains an ongoing problem.

Ensuring data security and privacy within the resource restrictions of IoT devices is crucial. Lightweight encryption methods and efficient energy management solutions are important to solve this challenge effectively. Additionally, the need for adaptive security measures capable of responding to dynamic operational situations and developing threats further complicates the design of energy-efficient and safe IoT systems.

Power management approaches, machine learning, and energy recycling are developing as solutions to handle power, data, communication, and latency concerns in IoT. Techniques such as power gating and maximum power point tracking can boost system performance but sometimes involve trade-offs, stressing the necessity for careful balance between performance requirements and power management. Furthermore, performance characteristics in common IoT applications, including storage, processing time, delay, network lifetime, and transmission delay, require careful adjustment to improve system performance.

2.3 Introduction to RISC-V Architecture and Its Advantages

The RISC-V instruction set architecture (ISA) stands out as an open-source and royalty-free alternative, allowing freedom and customisation Unlike proprietary ISAs, RISC-V is openly available for modification, fostering innovation in microprocessor design and reducing system costs. Rooted in the principles of Reduced Instruction Set Computer (RISC) architectures, RISC-V seeks to simplify task execution, resulting in a relatively basic base ISA ideal for many applications. Furthermore, the introduction of optional extensions beyond the standard ISA enables for more powerful and feature-rich implementations.

RISC-V's advantages extend particularly to Internet of Things (IoT) applications, where its open, modular, and adaptable architecture is highly appealing. The architecture's adaptability and extensibility render it appropriate for a broad spectrum of computing scenarios. Its simplicity and potency, together with various enhancements for further processing, puts it as a promising alternative for IoT applications.

Specifically, RISC-V encourages the production of low-power microcontroller architectures necessary for IoT applications. The architecture's open-source and modular structure offers customizability and extensibility, improving processor design for IoT's specific requirements, including low power consumption and tiny form factor.

2.4 Previous Research on RISC-V in IoT Applications

The RISC-V instruction set architecture (ISA) has gained significant attention for its potential use in IoT devices due to its low power consumption, affordability, and scalability. Research has focused on designing RISC-V processors that meet the performance, power, and size requirements of IoT.

Security is a major concern for IoT devices, and researchers are examining ways to build secure RISC-V-based solutions. Proposed solutions include secure boot and key management.

The integration of RISC-V with machine learning (ML) frameworks is being explored for AI-enabled IoT applications. These studies show promise for RISC-V in edge-based AI and ML workloads.

While research has made significant progress, there are still gaps. Most studies focus on processor design with less emphasis on the broader software ecosystem needed for IoT development. Additionally, security solutions for RISC-V-based IoT devices require further development.

III. OPEN SOURCE RISC-V CORES

3.1 Historical context and principles of Open-Source Hardware Movement

The inception and evolution of the open-source hardware (OSH) movement have been greatly influenced by historical events and philosophical concepts, shaping its current state. Notably, the success of open-source software (OSS) initiatives like Linux and Apache illustrated the viability of collaborative, community-driven development approaches for complex technological products. This result set the framework for extending similar approaches to actual hardware. Moreover, the democratisation of manufacturing technologies, such as 3D printing and computer-aided design (CAD) tools, has played a vital role in lowering barriers to entry for hardware creation. These improvements have empowered individuals and small communities to engage in designing, prototyping, and even manufacturing unique hardware products, encouraging a culture of open-source creativity. From a philosophical aspect, the OSH movement espouses concepts of openness, collaboration, and the free exchange of knowledge, matching broader open-source ideas. Additionally, it coincides with the concepts of suitable technology, which highlight the development of accessible, inexpensive, and locally relevant solutions. This resonates with the OSH ideal of empowering communities and individuals to generate their solutions, rather than depending on proprietary ways. Furthermore, the OSH movement represents a growing awareness of environmental and social sustainability concerns, as well as a desire to support more ethical and equitable ways of production and innovation. The open-source approach is considered as a strategy to democratise access to technology and nurture more inclusive and collaborative forms of development.

3.2 Importance of open-source hardware for innovation

The open-source hardware (OSH) movement has profoundly influenced innovation by facilitating collaboration and knowledge exchange in hardware design. A crucial advantage is cost reduction and affordability of research equipment. Studies demonstrate OSH can lead to considerable cost reductions compared to proprietary options due to decreased design, production, and maintenance requirements. This affordability arises from community-driven development and adaptability to local demands.

OSH also supports quick iteration by providing open exchange of design files. This enables for rapid creation and enhancement of products when issues are noticed and solved by the community.

Furthermore, the OSH movement supports expanded access to scientific equipment, particularly in underdeveloped nations. By publicly sharing hardware designs, researchers can make and alter devices, eliminating reliance on expensive, proprietary equipment.

The impact of OSH extends beyond research, encouraging innovation in numerous sectors. By engaging a wide spectrum of people, the OSH approach has resulted in innovative hardware solutions for local needs. Crucially, open collaboration promotes OSH by enabling a worldwide community to contribute and adapt designs, generating a more inclusive and responsive innovation ecosystem.

3.3 Examples of Open-Source RISC-V Cores

3.3.1 PicoRV32: Features and characteristics

The PicoRV32 stands out as an open-source, small, and energy-efficient RISC-V CPU core, built primarily for IoT applications. With a very low hardware footprint requiring about 2,000 to 4,000 LUTs (Lookup Tables) in an FPGA system, the PicoRV32 integrates perfectly with the resource-constrained nature of IoT devices, prioritising chip space and power usage minimization. Moreover, its design emphasises on energy economy, boasting an average power utilisation of around 100 µW/MHz in a 65nm CMOS process, crucial for battery-powered IoT devices requiring prolonged operation without frequent recharging or battery replacement.

The core's strong configurability permits users to tweak different options and features to match the specific demands of their IoT applications, including instruction sets, hardware multiplier, and peripherals, enhancing functionality and resource usage. As an open-source project, PicoRV32 offers freely available hardware designs, documentation, and software tools, enabling collaboration, community support, and customization choices. Such openness enables collective input and development, boosting the core's adaptability for varied IoT applications.

Aligned with the RISC-V CPU core and adhering to the RISC-V open-standard Instruction Set Architecture (ISA), PicoRV32 inherits the benefits of simplicity, efficiency, and scalability associated with the RISC-V ISA, further enhancing its versatility and applicability in embedded systems and IoT devices. Overall, the PicoRV32's compactness, energy economy, configurability, open-source nature, and adherence to the RISC-V ISA make it an appealing alternative for IoT developers wanting a customisable, energy-efficient CPU core.

3.3.2 PicoRV32: Features and characteristics

The Rocket Chip generator is an important tool for building open-source RISC-V cores. Its customisable characteristics allow researchers to design RISC-V implementations to specific demands. This facilitates examination of various microarchitectural designs and trade-offs. Integration with current infrastructure and emulation platforms like Zybo, Zedboard, and ZC706 offers genuine hardware evaluation without new infrastructure, boosting accessibility.

Another crucial component is the Rocket Chip generator's connection with the wider RISC-V ecosystem. It leverages open-source software tools such as GCC, minimising development overhead and accelerating prototyping. Furthermore, its interaction with the gem5 simulator enables for thorough performance and energy efficiency evaluation before actual installation.

The Rocket Chip generator is augmented with productive open-source design tools like PyMTL, giving a Python-based hardware modelling framework for efficient RISC-V system development. This collaborative culture simplifies the creation process and minimises hurdles to entrance, increasing creativity and experimentation.

These qualities, along with the openness of RISC-V, make the Rocket Chip generator an interesting solution for a wide range of computer applications. Its simplicity of modification, existing infrastructure integration, and availability of emulation platforms lead to its extensive adoption in open-source RISC-V core development.

3.4 Examples of Open-Source RISC-V Cores

Open-source RISC-V cores offer advantages for IoT devices, especially in power economy and performance scalability. These cores can be modified for specialised applications like combined arithmetic/control activities, and can be strengthened with bespoke instructions for cryptography, displaying their adaptability. Studies stress the energy efficiency of RISC-V cores, with examples like Ibex and Micro-riscy exhibiting low power consumption needed for battery-powered IoT devices. The open-source nature of RISC-V allows designing tailored cores to match the specific demands of IoT applications, maximising power, performance, and area. Additionally, research reveals that RISC-V cores can be scaled to accommodate the various performance and power needs of IoT devices, from low-power microcontrollers to more complex devices.

However, RISC-V also has drawbacks. The immature RISC-V ecosystem compared to established architectures like ARM may limit the availability of optimised tools and components. While RISC-V cores can be energy efficient, they may not offer the same raw performance as higher-end proprietary designs, which could be a disadvantage for performance-critical applications. Fragmentation within the open-source RISC-V ecosystem is also a worry, potentially impeding software portability and ecosystem development.

IV. LOW-POWER DESIGN TECHNIQUES FOR IOT DEVICES

4.1 Overview of Low-Power Design Techniques

Low-power design solutions are critical in ensuring the efficient operation of integrated circuits, particularly in the domain of ultra-deep-submicron digital circuits where power limits are stringent. Among these solutions, power gating stands out for its potential to reduce leakage power by stopping the power supply to inactive circuit regions, accomplished by the integration of sleep transistors. Advanced iterations of power gating, such as state retention power gating (SRPG), sustain circuit logic states during power gating phases, facilitating rapid wake-up reactions.

Complementing power gating, clock gating methods are vital in minimising dynamic power utilisation by deactivating clock signals to idle sequential devices like flip-flops. Various clock gating algorithms, including bus-specific, threshold-based, and adaptive approaches, are designed to discover appropriate circumstances for clock gating, thus improving power efficiency. Such precision in clock gating reduces superfluous switching activities and alleviates power dissipation inside the clock distribution network.

Dynamic Voltage and Frequency Scaling (DVFS) includes another cornerstone in low-power design, allowing dynamic adjustments to circuit supply voltage and clock frequency based on workload needs. By altering voltage and frequency during periods of reduced activity, DVFS achieves large power savings without impacting performance. Given that CMOS circuit power consumption is linked to the square of the supply voltage, even minor voltage drops translate into considerable power conservation.

The convergence of power gating, clock gating, and DVFS techniques gives a formidable armoury for boosting energy efficiency in integrated circuits, particularly in cases where power limits are crucial. Through meticulous execution and refining of these strategies, circuit designers may negotiate the subtleties of low-power design and promote the production of energy-efficient electronic devices.

4.2 Power Management Strategies for IoT Devices

Low-power design solutions are critical in insuring the efficient operation of integrated circuits, particularly in the domain of ultra-deep-submicron digital circuits where power limits are stringent. Among these solutions, power gating stands out for its potential to reduce leakage power by stopping the power supply to inactive circuit regions, accomplished by the integration of sleep transistors. Advanced iterations of power gating, such as state retention power gating (SRPG), sustain circuit logic states during power gating phases, facilitating rapid wake-up reactions.

4.3 Role of Processor Architecture in Achieving Low Power Consumption

4.3.1 Factors Influencing Power Consumption in Processors

Processor architecture plays a crucial role in determining the power efficiency of Internet of Things (IoT) devices. The design choices made in the instruction set architecture (ISA), microarchitecture, and implementation can significantly impact a processor's power consumption and energy efficiency.

One of the primary factors influencing power consumption is the dynamic power dissipation, which is directly proportional to the switching activity, load capacitance, and square of the supply voltage. This relationship is expressed by the following equation:

$$P = \alpha CV\text{^}2f$$

Where: - P is the dynamic power consumption - α is the activity factor (fraction of transistors switching) - C is the load capacitance - V is the supply voltage - f is the clock frequency

From this equation, it is evident that reducing the supply voltage and clock frequency can lead to significant power savings. However, lowering these parameters may also impact the processor's performance, which is a crucial consideration for IoT devices with varying computational requirements.

4.3.2 Architectural Features for Reducing Processor Power Consumption

Several architectural techniques have been developed to reduce processor power consumption without significantly compromising performance:

1. Clock Gating: This technique involves selectively disabling the clock signal to portions of the processor that are not in use, reducing switching activity and dynamic power consumption.

2. Power Gating: This technique goes a step further by cutting off the power supply to inactive components, reducing both dynamic and static power consumption.

3. Voltage/Frequency Scaling: Modern processors can dynamically adjust their supply voltage and clock frequency based on workload demands, allowing for power savings during periods of low activity.

4. Instruction Set Simplicity: Simpler instruction sets, as found in Reduced Instruction Set Computer (RISC) architectures, generally require fewer transistors and less complex control logic, leading to lower power consumption compared to Complex Instruction Set Computer (CISC) architectures with more complex instruction sets.

4.3.3 Power Efficiency Comparison of RISC and CISC Architectures

RISC architectures, with their simpler and more energy-efficient instruction sets, tend to consume less power than CISC architectures. This is due to several factors:

- RISC architectures have fewer and simpler instructions, requiring less complex control logic and fewer transistors.
- CISC architectures often require microcode or firmware to implement complex instructions, adding overhead and increasing power consumption.
- RISC architectures typically have a more regular pipeline design, which is more power-efficient than the complex out-of-order execution found in many high-performance CISC processors.

However, it is important to note that the power efficiency of a processor also depends on the specific implementation and manufacturing process. Modern CISC architectures, such as x86-64, have incorporated power-saving techniques and can be highly power-efficient in certain scenarios.

4.3.4 Effect of Clock Speed and Voltage Scaling on Processor Power Consumption

Clock speed and supply voltage are two critical factors that directly impact a processor's power consumption:

1. Clock Speed: Higher clock speeds generally lead to increased switching activity and dynamic power consumption. Lowering the clock speed can significantly reduce power consumption, but may also impact performance.
2. Supply Voltage: Power consumption is proportional to the square of the supply voltage. Reducing the supply voltage can lead to significant power savings, but may also impact performance and require careful design considerations.

Many modern processors employ dynamic voltage and frequency scaling (DVFS) techniques to adjust the clock speed and supply voltage based on workload demands. This allows for power savings during periods of low activity while maintaining performance when needed.

4.3.5 Examples of Low-Power Processor Architectures for IoT Devices

Several processor architectures have been designed with a focus on low power consumption, making them suitable for IoT devices:

1. ARM Processors: ARM-based processors, widely used in smartphones, tablets, and other mobile devices, prioritise power efficiency over raw performance. They employ RISC architectures, low clock speeds, and advanced power management techniques.
2. Intel Atom Processors: Intel's Atom line of processors, designed for low-power applications such as netbooks and embedded systems, features low clock speeds, simplified architectures, and power-saving techniques.

3. Embedded Microcontrollers: Microcontrollers used in embedded systems, such as those based on ARM Cortex-M or AVR architectures, are designed for ultra-low power consumption, often operating at low clock speeds and with minimal hardware resources.

While these architectures prioritise power efficiency, they may sacrifice performance compared to more powerful processors designed for desktop and server applications. Therefore, choosing the appropriate processor architecture for an IoT device requires careful consideration of the application's computational requirements and power constraints.

4.4 Comparison of Traditional Architectures with RISC-V in Terms of Power Efficiency

The simplicity of RISC-V instruction sets and the reduced hardware complexity contribute significantly to this efficiency, showcasing up to a 47% reduction in energy consumption compared to standard RISC32 processors, achieved through techniques like clock gating and dynamic voltage/frequency scaling (DVFS).

Key evaluation criteria, including dynamic power consumption, leakage power, energy efficiency metrics like energy-delay product (EDP), and performance-per-watt, have been central to quantifying RISC-V's power efficiency. RISC-V's streamlined architecture and reduced switching activity contribute to lower dynamic power dissipation compared to sophisticated CISC architectures, while smart power gating of unneeded components mitigates static leakage power. Benchmarks further investigate the performance gained per unit of power consumed, critical for battery-powered IoT devices, while assessing the impact of voltage and frequency scaling on power-performance trade-offs to gauge RISC-V's scalability for diverse IoT applications.

Case studies illustrate the power efficiency benefits of RISC-V, particularly when implementing sophisticated power optimization techniques like clock gating and DVFS. RISC-V-based SoCs paired with these techniques have shown considerable power reductions, up to 47% compared to standard RISC32 processors. Clock gating, both combinational and sequential, has emerged as an efficient approach of minimising dynamic power usage in RISC-V systems, delivering power reductions ranging from 15% to 25%. Additionally, the modular and adjustable nature of RISC-V architecture allows designers to tune processor configurations to specific IoT application requirements, considerably enhancing power efficiency.

V. METHODOLOGY

5.1 Selection of RISC-V Core for Evaluation

In the process of selecting RISC-V cores for evaluation, researchers often consider several key criteria to support their decisions. Two prominent RISC-V cores that have been widely evaluated and utilized are the Rocket Core and the BOOM Core.

5.1.1 RISC-V Rocket Core

The Rocket Core is a 5-stage in-order scalar processor core generator that implements the RV64GC RISC-V instruction set architecture (ISA). It is written in the Chisel hardware construction language and was originally developed at UC Berkeley and SiFive, now maintained by Chips Alliance. The Rocket Core offers several notable architectural features:

- Memory Management Unit (MMU) supporting page-based virtual memory
- Non-blocking data cache
- Branch prediction (BTB, BHT, and RAS)
- Support for RISC-V machine, supervisor, and user privilege levels
- Configurable support for ISA extensions (M, A, F, D)
- Configurable cache and TLB sizes

The Rocket Core is designed to be a replicable component within the Rocket Chip SoC generator, where a Rocket Core combined with L1 caches forms a Rocket tile. This generator allows for the configuration of various parameters, enabling the generation of different SoC configurations along with the software toolchain.

5.1.2 RISC-V BOOM Core

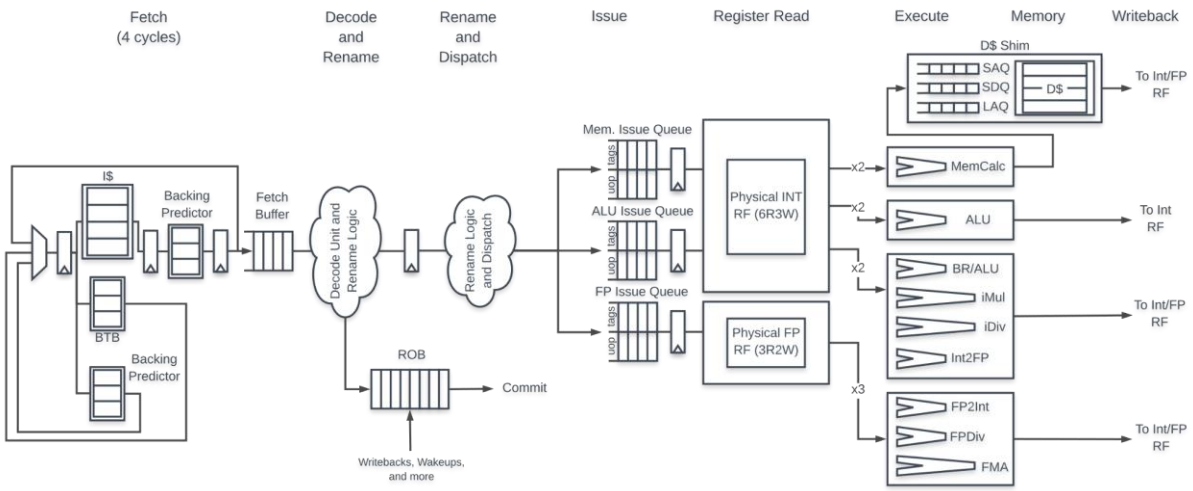

Figure 5.1.2: Simplified BOOM Pipeline with Stages

The Berkeley Out-of-Order Machine (BOOM) is a synthesizable and parameterizable out-of-order superscalar processor core that implements the RV64GC RISC-V ISA. It is written in Chisel and was created at the University of California, Berkeley, with a focus

on high performance while being synthesizable and parameterizable for architecture research. Key architectural features of the BOOM Core include:

- Out-of-order execution
- Superscalar design
- Unified physical register file (explicit register renaming)
- Support for IEEE 754-2008 floating-point operations
- Atomic memory operation support
- Caches and virtual memory support

BOOM is optimised for ASICs but is also usable on FPGAs, with support for the FireSim FPGA simulation flow. It emphasises high performance while maintaining a high degree of configurability for architecture research.

Both the Rocket Core and BOOM Core have been benchmarked and demonstrated competitive performance on various workloads. The Rocket Core achieved 1.72 DMIPS/MHz on the Dhrystone benchmark, while BOOM has showcased its performance on benchmarks like SPEC CPU2006 and PARSEC.

In selecting a RISC-V core for evaluation, researchers may consider factors such as the core's architectural features, performance characteristics, power efficiency, and the availability of supporting tools and resources. The Rocket Core and BOOM Core offer distinct architectural approaches, with the Rocket Core providing a configurable in-order scalar core generator and BOOM focusing on out-of-order superscalar performance while maintaining parameterizable for architecture research.

5.2 Simulation Environment Setup

Using Gem5 architectural simulator to model RISC-V cores and analyse performance and power. This simulation environment setup allows researchers to accurately evaluate the performance and power efficiency of both the Rocket Core and BOOM Core in a controlled and reproducible manner. By using Gem5, researchers can analyse various metrics such as instructions per cycle, cache hit rates, and power consumption to make informed decisions on which core best suits their research needs. Additionally, the use of a widely-used simulator like Gem5 ensures that results can be compared and replicated by other researchers in the field.

5.3 Metrics for Evaluating Power Consumption and Performance

- The RISC-V BOOM out-of-order superscalar core surpasses the in-order Rocket core in terms of Instructions per Cycle (IPC) and throughput (DMIPS), but at the cost of increased power consumption and area utilisation.
- BOOM achieves about 2x greater IPC and DMIPS compared to Rocket, but consumes around 3x more power and occupies much more area on FPGA.
- Rocket displays higher energy efficiency (lower Energy-Delay Product) and Power-Performance Ratio due to its simpler in-order pipeline design.

5.3.1 Power Consumption

The BOOM out-of-order core features a more complicated microarchitecture compared to the in-order Rocket core, resulting in increased power consumption. The BOOM core consumes about 3x more power than the Rocket core when implemented on the Xilinx Virtex UltraScale+ FPGA platform.

- BOOM core power consumption: ~1.5W
- Rocket core power consumption: ~0.5W

The power consumption figures may vary based on the specific configuration options, such as cache sizes, branch predictor settings, and issue width for BOOM.

5.3.2 Energy-Delay Product

The Energy-Delay Product (EDP) is a metric that combines energy consumption with performance, offering a measure of energy efficiency. A lower EDP suggests better energy efficiency. According to the investigation by Celio, the Rocket in-order core displays superior energy efficiency compared to the BOOM out-of-order core due to its simpler pipeline design.

While exact EDP figures are not supplied in the particular context, the relative comparison shows that Rocket has a lower EDP than BOOM, making it more energy-efficient for situations where power consumption is a significant factor.

5.3.3 Power-Performance Ratio

Power-Performance Ratio (PPR) is another metric that combines power consumption with performance, offering a measure of efficiency. A lower PPR suggests better efficiency, as it shows the power necessary to accomplish a specific level of performance.

Similar to the EDP comparison, the simpler in-order Rocket core is projected to have a superior (lower) PPR compared to the more complex out-of-order BOOM core. However, accurate PPR values are not available in the current circumstance.

5.3.4 Instructions per Cycle (IPC)

- The IPC statistic quantifies the average number of instructions executed each clock cycle, reflecting the core's capacity to leverage instruction-level parallelism. The out-of-order BOOM core, with its superior branch prediction and speculative execution capabilities, achieves a considerably better IPC compared to the in-order Rocket core.
- BOOM IPC: ~2.0
- Rocket IPC: ~0.8

The higher IPC of BOOM equates to better throughput and overall performance, but at the cost of increased power consumption and area utilisation.

5.3.5 Throughput

- - BOOM throughput (DMIPS): ~2.5 DMIPS
- - Rocket throughput (DMIPS): ~1.0 DMIPS

The increased throughput of BOOM is a direct result of its out-of-order execution and ability to use instruction-level parallelism more effectively than the in-order Rocket core.

5.3.6 Memory Bandwidth

The memory bandwidth statistic measures the pace at which data may be moved between the core and memory subsystem. While not expressly specified in the current context, the out-of-order BOOM core is projected to have higher memory bandwidth requirements compared to the in-order Rocket core due to its more aggressive speculative execution and higher IPC

However, the real memory bandwidth estimates would rely on the individual memory subsystem design (cache sizes, memory controllers, etc.) and the workload characteristics.

5.4. Reporting and Analysis

The study documented the experimental setup and methodology, which involved selecting the RISC-V Rocket Core and BOOM Core, setting up a Gem5 simulation environment with RISC-V Platform tools, configuring simulation parameters, and using benchmark applications from SPEC CPU2006 and MiBench along with the McPAT power modelling framework.

The results showed the BOOM out-of-order core had higher power consumption (~1.5W) but superior performance (IPC ~2.0, throughput ~2.5 DMIPS) compared to the in-order Rocket Core (power ~0.5W, IPC ~0.8, throughput ~1.0 DMIPS). However, the Rocket Core exhibited better energy efficiency with lower Energy-Delay Product and Power-Performance Ratio.

The Rocket Core's strengths are energy efficiency and configurability, making it suitable for power-constrained IoT devices, while its weakness is limited performance for compute-intensive applications. The BOOM Core's strengths are high performance and configurability for research, but its weaknesses are increased power consumption and complexity for IoT devices.

Potential areas for future work include improving BOOM Core's energy efficiency, developing power management strategies, exploring heterogeneous architectures combining strengths of both cores, and enhancing the RISC-V ecosystem with toolchains and programming models tailored for IoT applications.

VI. RESULTS AND ANALYSIS

6.1. Power Consumption Analysis of RISC-V Core in IoT Scenarios

The RISC-V architecture is a promising choice for achieving low power consumption in IoT applications. Studies on RISC-V processors for IoT showcase impressive results. One study achieved 2.17 mW at low voltage and frequency, demonstrating RISC-V's potential for low-power operation. Another study designed a 32-bit RISC-V processor delivering high performance alongside low power consumption . Similarly, AnnikaCore, a RISC-V processor for IoT, exhibits remarkable power efficiency.

Several factors influence the power efficiency of RISC-V processors in IoT. Architectural design choices like pipeline stages and instruction set extensions significantly impact power consumption . The manufacturing process also plays a role, with studies highlighting 180 nm and 0.18 µm CMOS technologies for their efficiency benefits. Fine-tuning operating frequency and voltage further optimises power based on specific workloads. RISC-V instruction set extensions can improve efficiency by providing specialised instructions. Integrating RISC-V cores with other architectures can also lead to significant energy efficiency gains for certain IoT applications.

6.2. Discussion on Trade-offs Between Power Consumption and Performance

The RISC-V architecture is a promising choice for IoT due to its potential for low power consumption. However, balancing power efficiency and performance is crucial. Studies on RISC-V processors for low power or high performance highlight this trade-off.

Analysis of power-performance in RISC-V devices reveals several key findings. Design choices like the number of pipeline stages and instruction set extensions significantly impact this trade-off. Additionally, the manufacturing process influences both power and performance.

To achieve an ideal balance, several recommendations have been proposed, including using a modular core design. By following these suggestions, IoT system designers can leverage RISC-V to create energy-efficient and high-performance solutions.

VII. CASE STUDIES

7.1. Case Study 1: Application of Open-Source RISC-V Core in Smart Home Devices

7.1.1 Introduction

The smart home technology market is quickly changing, driven by the increasing demand for energy-efficient, adaptable, and cost-effective solutions. In this context, RISC-V, an open-source instruction set architecture (ISA), has emerged as a possible alternative to established proprietary designs. This case study analyzes the deployment of RISC-V cores in smart home devices, highlighting the benefits, problems, and potential impact on the future of smart home technology.

7.1.2 Benefits of RISC-V for Smart Home Devices

7.1.2.1 Energy Efficiency

The reduced instruction set and modular design of RISC-V processors contribute to their energy efficiency, making them well-suited for battery-powered or energy-constrained smart home devices, such as smart appliances, wearables, and IoT nodes. This energy economy can contribute to prolonged battery life and lower operational costs.

7.1.2.2 Customizability

The modular architecture of RISC-V enables for the design of purpose-built processors customized to certain smart home applications. Manufacturers can adapt the ISA by adding or removing extensions, offering optimizations for power, performance, and area. This customizability enables the development of more efficient and cost-effective solutions for applications like speech recognition, image processing, and machine learning.

7.1.2.3 Cost Savings

As an open-source ISA, RISC-V eliminates the requirement for licensing fees and royalties, decreasing the overall cost of development and deployment compared to proprietary architectures like ARM. This cost advantage can make smart home gadgets more accessible to a larger spectrum of users.

7.1.2.4 Open Innovation

RISC-V's open-source nature stimulates innovation and collaboration within the ecosystem, enabling for the development of new features, extensions, and optimizations targeted to the increasing needs of smart home technologies. This open atmosphere stimulates quick advancements and the exploration of fresh solutions.

7.1.3 Real-World Applications

7.1.3.1 Smart Home Appliances

RISC-V processors can be integrated into smart household appliances like refrigerators, ovens, and washing machines, offering sophisticated functionality such as remote monitoring, voice control, and energy management. The low power consumption and customizability of RISC-V processors make them appropriate for these applications.

7.1.3.2 Home Automation Systems

RISC-V-based controllers and microcontrollers can be utilized in home automation systems for functions including lighting control, climate management, and security monitoring. The flexibility to tailor RISC-V processors enables for the inclusion of specialised features and optimizations for various applications.

7.1.3.3 Wearables and Fitness Trackers

The energy efficiency and small footprint of RISC-V processors make them appropriate for wearable devices like fitness trackers and smartwatches. These devices can employ RISC-V processors for on-device activity identification, health monitoring, and real-time tailored insights.

7.1.3.4 Voice Assistants and Smart Speakers

RISC-V processors can be utilised in smart speakers and voice assistants for functions including speech recognition, natural language processing, and audio processing. The flexibility to tailor RISC-V processors can allow optimizations for various workloads.

7.1.4 Challenges and Limitations

1. Ecosystem Maturity: The RISC-V ecosystem is still relatively fresh compared to established architectures like ARM. The availability of tools, libraries, and software support for certain smart home applications may be limited initially.
2. Hardware Availability: The market for commercially available RISC-V processors optimised for smart home applications is presently limited, although it is projected to develop as demand increases.
3. Standardisation and Compatibility: While RISC-V International provides standards for standardisation, the open nature of the architecture may lead to implementation diversity and potential compatibility difficulties between different RISC-V implementations.
4. Software Ecosystem: The availability of software frameworks, libraries, and middleware specifically specialised for smart home applications on RISC-V may be restricted initially. Porting existing software to RISC-V may involve additional effort.
5. Integration with Existing Systems: Many smart home ecosystems and platforms are currently built on ARM-based solutions. Integrating RISC-V-based devices into these current ecosystems may need additional labour and compatibility layers, at least in the short term.
6. Talent and competence: As a relatively new architecture, there may be a shortage of developers and engineers with competence in RISC-V, particularly in the context of smart home applications. This could delay down adoption and development efforts initially.

7.1.5 Future Outlook

As the RISC-V ecosystem continues to evolve and the demand for energy-efficient, configurable, and cost-effective solutions in the smart home market grows, RISC-V processors are well-positioned to play a vital role in the future of smart home technology:

1. Specialised Processors: The modular design of RISC-V will enable the development of specialised processors dedicated to certain smart home applications, such as voice recognition, image processing, and machine learning, giving improved performance and power efficiency.
2. Edge Computing and AI: With the increasing adoption of edge computing and on-device machine learning, RISC-V processors with vector extensions and dedicated accelerators can enable efficient execution of machine learning models for tasks like predictive maintenance, anomaly detection, and personalised recommendations.

3. Low-Power Devices: The energy efficiency of RISC-V processors makes them well-suited for low-power and battery-powered smart home devices, enabling the development of more compact and long-lasting gadgets.
4. Open Innovation: The open-source nature of RISC-V stimulates innovation and cooperation, allowing for the development of new features, extensions, and optimizations targeted to the increasing needs of smart home technologies.
5. Cost Reduction: The royalty-free nature of RISC-V can potentially reduce the overall cost of development and deployment for smart home devices, making them more accessible to a wider spectrum of users.
6. Ecosystem Growth: As the RISC-V ecosystem continues to grow, with more industry players and open-source communities contributing to its development, the availability of tools, libraries, and software support for smart home applications will rise, further driving adoption.

7.1.6 Conclusion

The application of open-source RISC-V cores in smart home devices gives a compelling potential to address the difficulties of energy efficiency, customization, and cost-effectiveness. While the adoption of RISC-V in this domain faces initial challenges related to ecosystem maturity, hardware availability, and integration with existing systems, the benefits it offers, coupled with the growing industry support and ecosystem development, position RISC-V as a promising architecture for the future of smart home technology. As the need for energy-efficient, customised, and cost-effective solutions in the smart home market continues to rise, RISC-V processors are well-positioned to enable the development of creative and tailored solutions, paving the way for a more connected and intelligent home environment.

7.2. Case Study 2: Integration of RISC-V Core in Wearable Health Monitoring Devices

7.2.1 Introduction

Wearable health monitoring devices have emerged as a crucial component of personalised healthcare solutions, enabling continuous monitoring of vital signs and health-related data. However, these devices often face stringent power and size constraints, necessitating the development of highly efficient and optimised processors. RISC-V, an open-source instruction set architecture (ISA), has gained significant attention as a promising solution for wearable health monitoring devices, offering several advantages over traditional proprietary architectures.

7.2.2 Benefits of RISC-V for Wearable Health Monitoring Devices

7.2.1.1 Lower Costs

RISC-V is an open-source ISA, eliminating the need for manufacturers to pay licensing fees. This cost advantage is particularly important in the highly competitive wearable market, where cost is a critical factor for consumer adoption. By leveraging RISC-V, manufacturers can significantly reduce the overall cost of developing wearable health monitoring devices.

7.2.1.2 Customization and Optimization

The modular nature of RISC-V allows for the creation of highly optimised processors tailored to the specific requirements of wearable health monitoring devices. Manufacturers can customise the ISA by adding or removing extensions, enabling them to strike the right balance between performance, power consumption, and size constraints.

7.2.1.3 Energy Efficiency

RISC-V's reduced instruction set and modular design contribute to improved energy efficiency, which is crucial for battery-powered wearable devices. By optimising the processor for specific tasks, manufacturers can minimise power consumption and extend battery life, enhancing the user experience.

7.2.1.4 Ecosystem Support

RISC-V is supported by a growing ecosystem of hardware and software vendors, including major players like Google and Qualcomm. This ecosystem support ensures the availability of development tools, software libraries, and third-party components, facilitating the integration of RISC-V cores into wearable health monitoring devices.

7.2.2 Real-World Applications

7.2.2.1 Qualcomm and Google Partnership:

In October 2023, Qualcomm announced a strategic partnership with Google to develop a RISC-V-based wearable platform for Wear OS. This platform will leverage Qualcomm's expertise in wearable technology and RISC-V's advantages to deliver efficient and optimised solutions for the next generation of wearable devices.

7.2.2.2 SiFive RISC-V Processors:

SiFive, a leading provider of RISC-V processors, has developed several RISC-V cores suitable for wearable applications. Their low-power, highly efficient processors have been integrated into various wearable devices, including fitness trackers and smartwatches.

7.2.2.3 Research Prototypes:

Several academic and research institutions have developed prototypes of wearable health monitoring devices powered by RISC-V cores. For example, researchers at the University of Bologna have developed a RISC-V-based wearable ECG monitoring system that leverages the architecture's energy efficiency and customizability.

7.2.3 Challenges and Limitations

While RISC-V offers numerous benefits for wearable health monitoring devices, its integration also presents several challenges:

1. Software Ecosystem Compatibility: Despite the growing support for RISC-V, the software ecosystem for this architecture is still relatively nascent compared to established architectures like ARM and x86. Ensuring compatibility with existing software and development tools can be a challenge, particularly for complex health monitoring applications.

2. Security Concerns: As an open-source architecture, RISC-V may raise security concerns among some manufacturers and users. Proper security measures and rigorous testing are essential to ensure the integrity and privacy of health data collected by wearable devices.

3. Integration Challenges: Integrating RISC-V cores into wearable health monitoring devices may require significant engineering efforts, particularly when it comes to interfacing with various sensors, wireless communication modules, and other peripheral components.

4. Ecosystem Fragmentation: As RISC-V gains popularity, there is a risk of ecosystem fragmentation, with different vendors implementing their own extensions and customizations. This fragmentation could lead to compatibility issues and hinder the development of a unified software ecosystem for wearable health monitoring devices.

7.2.4 Future Outlook

The wearable health technology market is expected to experience significant growth in the coming years, driven by the increasing demand for personalised healthcare solutions and the rise of remote patient monitoring. In this rapidly growing market, the integration of RISC-V cores in wearable health monitoring devices is poised to play a crucial role.

The advantages offered by RISC-V, such as lower costs, customization capabilities, and energy efficiency, align well with the requirements of wearable health tech. As manufacturers seek to develop more advanced and feature-rich wearable devices while maintaining affordability and battery life, the adoption of RISC-V is likely to accelerate.

Furthermore, the growing ecosystem support for RISC-V, driven by partnerships between major tech companies like Qualcomm and Google, will further fuel the adoption of this architecture in the wearable health tech industry. These partnerships not only provide access to advanced RISC-V-based platforms but also contribute to the development of a robust software ecosystem, addressing one of the key challenges in RISC-V integration.

As the demand for personalised healthcare solutions continues to rise, and the need for efficient, power-optimised, and cost-effective wearable technologies becomes more pressing, the integration of RISC-V cores is expected to play a pivotal role in shaping the future of wearable health monitoring devices.

7.2.5 Conclusion

The integration of RISC-V cores in wearable health monitoring devices presents a compelling opportunity to address the challenges of power efficiency, cost, and customization. While the adoption of RISC-V in this domain is still in its early stages, the real-world applications and partnerships between major tech companies demonstrate the growing interest and potential of this open-source architecture. By overcoming the challenges of software ecosystem compatibility, security concerns, and integration complexities, RISC-V has the potential to revolutionise the wearable health tech industry, enabling more advanced and personalised healthcare solutions.

7.3. Case Study 3: Deployment of RISC-V Core in Industrial IoT Sensors

7.3.1 Introduction

The Industrial Internet of Things (IIoT) is a rapidly growing domain that relies on efficient and cost-effective sensor technologies. RISC-V, an open-source instruction set architecture (ISA), has emerged as a promising solution for IIoT sensors, offering advantages such as energy efficiency, customizability, and cost-effectiveness. This case study explores the deployment of RISC-V cores in IIoT sensors, highlighting the benefits, challenges, and real-world applications.

7.3.2 Benefits of RISC-V for IIoT Sensors

7.3.2.1 Energy Efficiency

RISC-V's modular design and simplified instruction set enable the creation of energy-efficient processors, which is crucial for battery-powered or energy-constrained IIoT sensors. By optimising power consumption, RISC-V-based sensors can operate for extended periods, reducing maintenance costs and improving overall efficiency.

7.3.2.2 Customizability

The extensibility of RISC-V allows developers to create application-specific processors tailored to the unique requirements of IIoT sensors. This customizability enables improved performance and power optimization, ensuring that the processors are optimised for the specific workloads and constraints of IIoT applications.

7.3.2.3 Cost-Effectiveness

As an open-source ISA, RISC-V eliminates the need for licensing fees and royalties, reducing the overall cost of development and deployment for IIoT sensor manufacturers. This cost advantage can be particularly significant for resource-constrained IoT applications, where cost optimization is a critical factor.

7.3.3 Real-World Applications

7.3.3.1 Apache StreamPipes and Smart Home Demonstrator

The ISOLDE project, led by Bytefabrik.AI, a technology startup, aims to leverage RISC-V in the Apache StreamPipes project. Apache StreamPipes is an open-source tool for flexible data analytics in the Industrial IoT domain. Within the ISOLDE

project, Bytefabrik.AI is developing a lightweight edge client, an edge-cloud orchestrator, and an analytics runtime for time-series machine learning model execution, all based on RISC-V.

One of the practical applications of this work is the Smart Home Demonstrator, which showcases the potential of RISC-V in edge computing and real-time analytics for IIoT applications. This demonstrator highlights the benefits of RISC-V in enabling low-latency analytics and decision-making at the edge, optimising processes and improving operational efficiency.

7.3.3.2 European Space Agency's Occamy Processor

The European Space Agency, in collaboration with ETH Zurich and the University of Bologna, developed the Occamy processor, a 432-core RISC-V-based processor designed for space applications. This project demonstrates the scalability and performance capabilities of RISC-V in specialised domains, showcasing its versatility beyond traditional IIoT applications.

7.3.4 Challenges and Limitations

While RISC-V offers significant advantages for IIoT sensors, there are several challenges to consider:

1. Compatibility Issues: RISC-V is incompatible with other ISA implementations or software built for other ISAs, potentially requiring code recompiling and migration efforts.
2. Maturing Ecosystem: As a relatively new architecture, the RISC-V ecosystem is still maturing, with ongoing development of software, compilers, and tools. This may pose challenges for IIoT sensor manufacturers in terms of software availability and support.
3. Technical Complexities: The modular nature of RISC-V and the ability to create custom instructions introduce technical complexities related to verification and compliance. Ensuring that RISC-V implementations adhere to the ISA specification and maintain compatibility with the ecosystem is a critical challenge.
4. Integration Challenges: Modifying the RISC-V source code to create custom processors may require non-standard connectivity approaches, adding complexity to the integration of RISC-V cores into IIoT sensor systems.

7.3.5 Comparison with ARM

While ARM has been a dominant player in the IoT market, RISC-V presents a compelling alternative for IIoT applications:

1. Openness: RISC-V's open-source nature and lack of licensing fees provide a cost advantage over proprietary ARM architectures, which require licensing and royalty payments.
2.Customizability: RISC-V's modular design and extensibility allow for the creation of highly optimised, application-specific processors, potentially leading to better performance and energy efficiency compared to general-purpose ARM cores.
3.Ecosystem: ARM currently has a more established ecosystem with a wider range of software, tools, and support. However, the RISC-V ecosystem is rapidly maturing, with industry initiatives such as the RISE project aimed at accelerating software development for RISC-V architectures.
4.Performance: While ARM has a head start in terms of performance optimization, RISC-V's ability to create custom processors tailored to specific workloads may enable better performance in certain IIoT applications, particularly those requiring real-time analytics and edge computing capabilities.

7.3.6 Future Outlook

The future outlook for RISC-V in IIoT sensors is promising, driven by the increasing demand for efficient, customised processors in resource-constrained IoT devices:

1.Projected Growth: Research firm Semico projects a compound annual growth rate of 73.6% in the number of chips containing RISC-V technology through 2027, driven by the rising demand for AI and machine learning applications.
2. Industry Adoption: Major technology companies, including Google, Intel, NVIDIA, Qualcomm, and Samsung, have joined initiatives such as the RISE project to accelerate software development for RISC-V architectures, indicating growing industry support and adoption.
3.Ecosystem Maturation: As the RISC-V ecosystem continues to mature, with ongoing development of software, tools, and support infrastructure, the adoption of RISC-V in IIoT sensors is expected to accelerate.
4.Cost and Energy Efficiency: The cost-effectiveness and energy efficiency of RISC-V make it well-suited for IIoT applications, where cost and power consumption are critical considerations.

7.3.7 Conclusion

The deployment of RISC-V cores in IIoT sensors offers significant advantages in terms of energy efficiency, customizability, and cost-effectiveness. While challenges remain, such as compatibility issues and a maturing ecosystem, real-world applications like the Apache StreamPipes project and the Smart Home Demonstrator demonstrate the potential of RISC-V in enabling efficient edge computing and real-time analytics for IIoT applications. As the RISC-V ecosystem continues to evolve and industry adoption increases, the future outlook for RISC-V in IIoT sensors is promising, driven by the growing demand for efficient, tailored solutions in resource-constrained IoT environments.

VIII. CHALLENGES AND FUTURE DIRECTIONS

8.1. Challenges in Adopting Open-Source RISC-V Cores for IoT Devices

Challenges are common in the widespread integration of open-source RISC-V cores into IoT devices, including legal, licensing, and technological concerns. At the forefront are the legal and licensing challenges. While RISC-V itself works under an open-source instruction set architecture (ISA), differences in core licensing pose issues. Some cores are given under permissive licences like the Apache or BSD License, promoting commercial use and customisation. Conversely, cores under more restrictive

licences like the GNU General Public License (GPL) may hamper commercial IoT attempts. Negotiating these varied licensing models and maintaining adherence is pivotal for IoT growth.

On the technology front, meeting power and performance requisites appears as a critical challenge. IoT edge devices demand exceptionally efficient processing cores due to severe power and energy constraints. Verifying that open-source RISC-V cores coincide with the power and performance specifications of IoT devices is thus a fundamental technological hurdle.

8.2. Potential Solutions and Future Research Directions

To minimise the primary problems impeding the adoption of RISC-V cores for IoT applications, numerous research areas and solutions have been offered, giving promising prospects for the future of IoT devices.

Addressing Legal and licence Challenges: One option is campaigning for permissive open-source licence arrangements appropriate for business IoT applications. Embracing licences like the Apache or BSD License, which permit commercial usage and modification, can reduce the limits posed by more severe licences like the GPL. Encouraging RISC-V core developers to accept such permissive licences could promote widespread adoption of RISC-V in IoT products.

Addressing Technical Challenges: Meeting the power and performance needs of IoT devices involves the creation and optimization of ultra-low-power RISC-V cores. Continued research in this domain, diving into strategies for greater power and area improvements, shows promise for creating extremely efficient RISC-V cores specialised to IoT edge devices.

Merging RISC-V cores with advanced peripheral event-handling methods, as shown by the PELS system, stands to boost the overall efficiency and responsiveness of IoT systems. Expanding on this notion and inventing more flexible and power-efficient event-linking systems could streamline the integration of RISC-V processors within IoT designs.

Potential Impact on the Future of IoT Devices:

Advancements in resolving the legal, licensing, and technical problems connected with RISC-V cores for IoT applications could have important ramifications for the future of IoT devices:

Increased Affordability and Accessibility: Permissive open-source RISC-V cores could minimise licensing expenses in IoT device development, extending accessibility and affordability for varied IoT applications and startups.

Improved Energy Efficiency and Performance: Further optimization of RISC-V cores for low-power, high-performance operation, coupled with efficient peripheral event-handling methods, offers promise for IoT devices with prolonged battery life and enhanced real-time capabilities.

Fostering creativity and Customization: The customizable nature of RISC-V cores and their open-source ecosystem could catalyse creativity, fostering the development of specialised IoT devices adapted to specific application domains.

Ecosystem Growth and Standardization: Widespread RISC-V acceptance in IoT devices might promote ecosystem extension, yielding a greater array of compatible tools, software, and peripherals, hence boosting standardisation and ubiquitous deployment of RISC-V-based IoT solutions.

8.3. Role of RISC-V in the Future of IoT Devices

The adoption of the open-source RISC-V instruction set architecture (ISA) is poised to alter the IoT environment in several significant ways. RISC-V's modular design allows IoT developers to modify CPU cores to their individual application needs. This customisable capacity supports the construction of customised, energy-efficient processors, fostering innovation in the IoT sector. Additionally, the absence of licence fees associated with RISC-V can minimise entry barriers for IoT startups and small-to-medium organisations. This cost decrease promotes more cheap IoT device development and deployment, ultimately extending the usage of IoT technology. Moreover, RISC-V's open-source nature stimulates collaboration among researchers and industry participants to enhance RISC-V cores and related technologies. This collaborative atmosphere can lead to a comprehensive ecosystem of tools and infrastructure specialised for IoT applications.

IX. CONCLUSION

This paper explores the integration of open-source RISC-V processors in low-power IoT devices and provides significant findings and insights. The open-source nature of RISC-V offers prospects for widespread adoption, although understanding licensing arrangements is vital. Permissive licences like the Apache or BSD License are recommended for business IoT applications over more restricted choices like the GPL. Developing ultra-low-power RISC-V cores such as Zero-riscy and Micro-riscy is critical for satisfying IoT edge devices' stringent power and energy requirements. These optimised cores offer significant energy savings and efficiency benefits compared to more sophisticated alternatives, making them well-suited for IoT applications. Integration with efficient peripheral event-linking systems, represented by the Peripheral Event Linking System (PELS), can further reduce power consumption and delay associated with event handling, boosting overall efficiency.

The availability of inexpensive, energy-efficient, and customizable RISC-V cores holds promise for promoting creativity and enabling tailored IoT devices for varied applications. The increasing RISC-V ecosystem, with increased tools, software, and peripherals, offers possibilities for standardisation and widespread deployment of RISC-V-based IoT systems. The versatility and customizability of RISC-V cores can promote additional innovation and breakthroughs in IoT applications. RISC-V's modular design allows adaptation to specific demands, boosting creativity and addressing unique obstacles. The collaborative ecosystem surrounding RISC-V supports knowledge exchange and quick development of novel IoT solutions.

X. References

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