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Two-Loop Controlled SEPIC Type PCSC – Buck Boost Converter for Input Source Power Management

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Abstract : **The paper reviews the application of two-loop control for input source power management in Pulsating current source cell (PCSC) type Single-Ended Primary Inductor Converters (SEPIC) buck-boost converters. Because the SEPIC converter may step-up or step-down input voltage. This converter is employed in many different application including renewable energy system and portable electronics. Several capacitors are used in parallel by the PCSC topology Boost power density and efficiency. While the second loop manages input current to enhance performance under changing loads, the first loop modifies switch duty cycles to regulate output voltage. When it comes to dynamic reaction and strategy outperforms single loop techniques. This paper highlights the advantages and disadvantages of several control systems, including fuzzy logic, model predictive control, and proportional-integral-derivative (PID). This paper shows how component choice affects performance the efficiency transient, responsiveness and overall performance can be improved by two-loop control, as shown by comparative studies and experimental results. Future directions for this field of study are suggested in the paper's conclusion.**

IndexTerms **- SEPIC Converter, Buck Boost Converter, PCSC, PID, MIC's.**

I. INTRODUCTION

Due to the rapid development of renewable energy sources and the increasing demand for efficient power management systems, power electronics has advanced significantly. This is a input source power management option, the Pulsating current source cell (PCSC) type Single-Ended Primary Inductor Converter (SEPIC) buck-boost converter has demonstrated potential. This converter topology's capacity to step-up or step-down input voltages is a unique attribute that makes it suitable for a range of applications, such as renewable energy systems and portable electronic devices.

To develop SEPIC-type PCSC buck-boost converters, one of the primary challenges is to achieve steady and effective control over the input current and output voltage. Under fluctuating load conditions, traditional single-loop control techniques frequently fail to deliver the necessary dynamic response and stability. A two-loop control methodology, in which one loop controls the input current and the other the output voltage, has been offered as a solution to this problem. This paper aims to provide a comprehensive overview of the uses of two-loop regulated SEPIC-type PCSC buck-boost converters for input source power management. This will cover the use of the two-loop control approach, the advantages of the PCSC topology, and the operation of the converter. Additionally, a variety of control approaches, such as proportional-integral-derivative (PID) control, model predictive control, and fuzzy logic control, will be covered and their effectiveness in enhancing converter performance demonstrated. In the end, the study will present experimental results and comparative analysis to illustrate the benefits of the two-loop control strategy and provide suggestions for more research in this area.

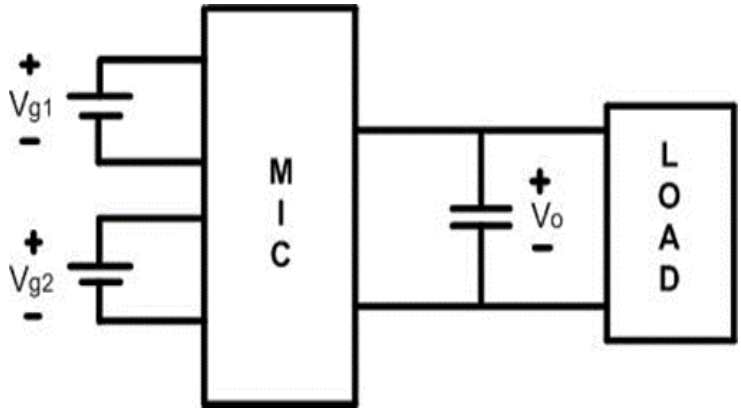

Fig.1. Diagram of n-input of DC-DC Converter

The rules for synthesizing MICs based on PCSC are-

Rule 1 – Voltage buffer section should be connected with PCSC parallelly while the connection of PCSC should be with the outgoing terminal serially.

Rule 2 – PCSC should be connected parallel to the voltage sink (the positive end of the voltage sink should be connected to the outgoing terminal of the PCSC) in order to connect it to the output section of the primary PWM dc-dc converter.

Rule 3 – A mesh Should be created between PCSC and output sink.

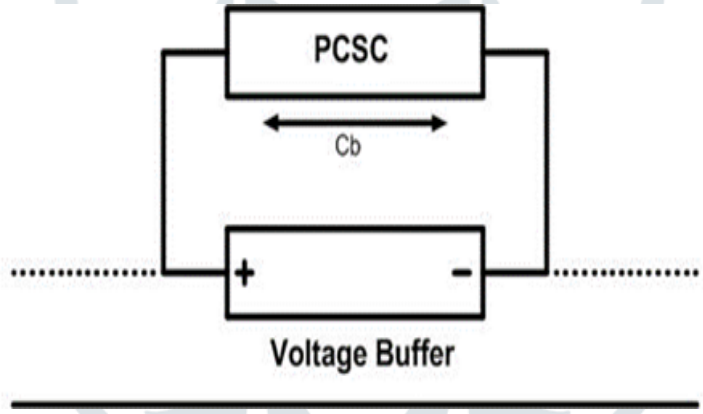

Fig.2. PCSC Connected to a partial energy buffer

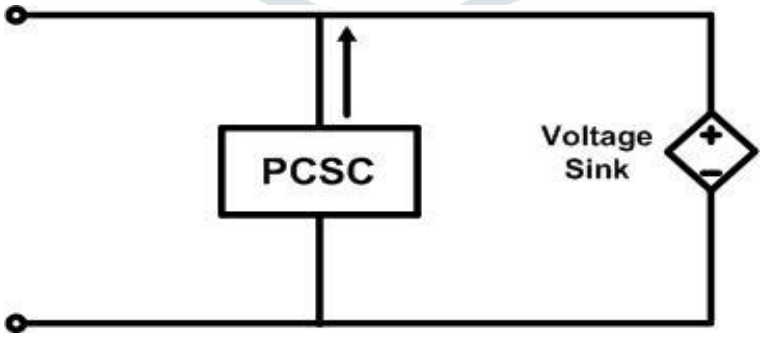

Fig.3. PCSC Connected to output source

II.MODELING AND ANALYSIS OF INTEGRATED SEPIC (PCSC) BUCK–BOOST CONVERTER.

A parallel combination of the SEPIC (PCSC)-Buck Boost converter is the suggested SEPIC-Buck Boost converter. The circuit of the SEPIC (PCSC) Buck Boost Converter is shown in Fig.4:

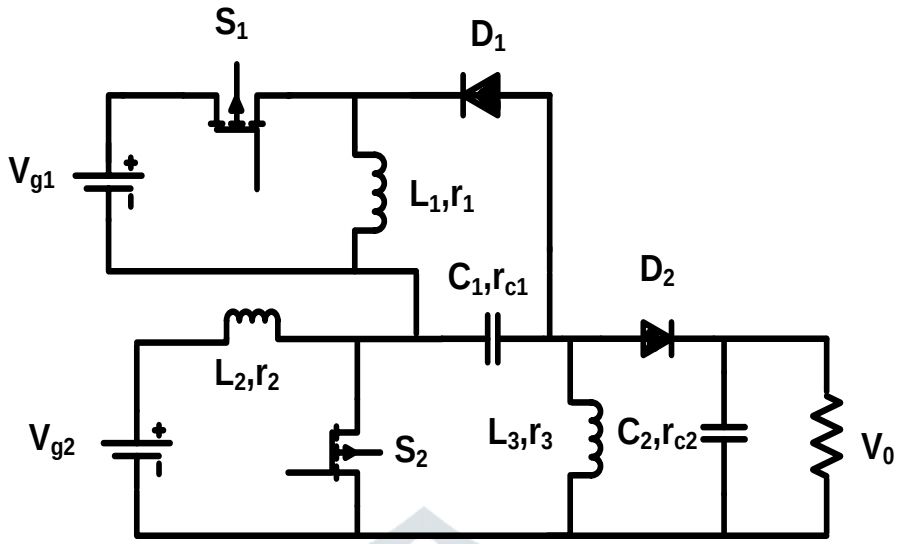

Fig.4. Proposed MIC

The inductor mode of the circuit can run continuously or intermittently. For DC-DC conversion, the two-input SEPIC-Boost converter distributes power via decoupled single-loops on DC voltage DC source current regulation.

The design of this converter distributes the total load demand between the two voltage sources, Vg_1 and Vg_2. The converter functions in a way that allows the LVS to run at maximum capacity, with the remaining load being drawn from a primary source or high voltage source. In order for the SEPIC-Buck Boost converter to function, the duty ratio is crucial.

Duty ratios d_1 and d_2 are selected for the MIC under consideration in order to control the boost converter and SEPIC (PCSC) switches, respectively. With the suggested converter, the duty ratio d_2 is greater than d_1. Fig.5 shows the pulse width modulation gate signals that are applied to the switches.

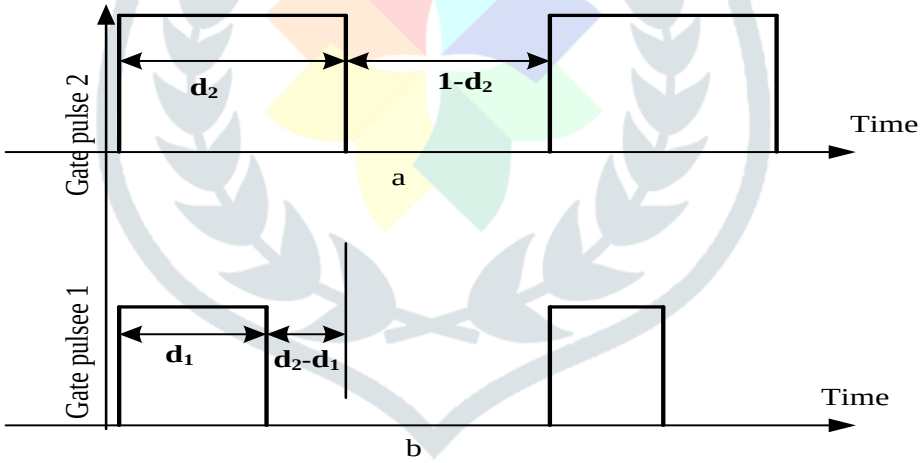

Fig.5. PWM gating signals and off-Time sampling process.

Three different modes of operation are conceivable depending on the gate pulse that is applied to the gate terminal of both switches. The table below provides the mode of operation, device status, and mode durations:

Table.1. SWITCH AND DIODE ON/OFF CONDITION DURING DIFFERENT MODES

S.NO	MODES	DEVICE ON	DEVICE OFF	MODES OF DURATION
1	Mode 1	S_1, S_2	D_1, D_2	$[0<t<(d_1*T_S)]$
2	Mode 2	S_2, D_1	S_1, D_2	$[d_{1*}T_S<t<(d_2-d_1)*T_S]$
3	Mode 3	D_2	S_1, S_2, D_1	$[(d_2-d_1)*T_S<t<T_S]$

II. STATE SPACE ANALYSIS AND DISCRETE TIME MODELLING.

On the basis of different modes of operation of two-input SEPIC (PCSC) – Buck Boost converter, steady space analysis is done. In a single switching cycle, this converter has three modes of operation that is described by a set of state space equation.

$$\frac{dy}{dx} = A_K X + B_K U \quad (1)$$

$$V_O = E_K X + F_K U \quad (2)$$

Where,

$$[X] = [i_{L1} \;\; i_{L2} \;\; i_{L3} \; V_{C1} \; V_{C2}]^T \quad (3)$$

$$[U] = \left[V_{g1} \;\; V_{g2}\right]^T \quad (4)$$

K = 1, 2, and 3 (depending on the modes of operation);

A_K= State matrix of mode k,

B_K = Input matrix of mode k,

E_K = Output matrix of mode k,

F_K= Feed through matrix of mode k.

ANALYSIS OF MODE -1 [0<t<(d_1*T_s)]

MODE – 1: The duration period of this mode is given as the [0 < t < (d_1*T_s)]. In this operating mode of converter, the switch S_1 and the switch S_2 is ON while the diode D_1 and the diode D_2 is OFF. The voltage sources Vg_1 and Vg_2 charge the inductors L_1 and L_2 linearly when they are directly connected to the dc sources. Capacitor C_1 charges inductor L_3 linearly in contrast. In contrast, the load voltage applied to capacitor C_2 stays constant. Fig.6 displays the Integrated SEPIC-Buck Boost Converter's operational circuit diagram.

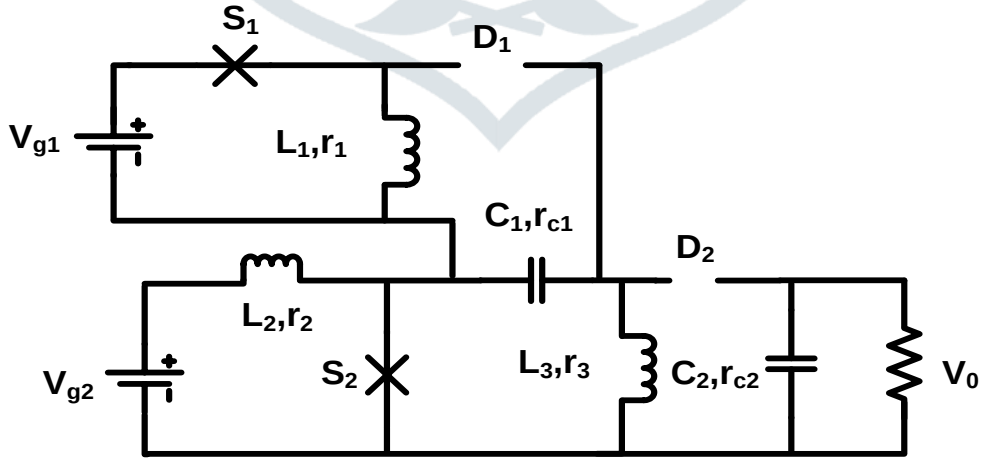

Fig.6. Equivalent circuit diagram of mode-1

State space matrix of mode-1

$$A_1 = \begin{bmatrix} -\frac{r_1}{L_1} & 0 & 0 & 0 & 0 \\ 0 & \frac{r_2}{L_2} & 0 & 0 & 0 \\ 0 & 0 & -\frac{r_{C1}+r_3}{L_3} & -\frac{1}{L_3} & 0 \\ 0 & 0 & \frac{1}{C_1} & 0 & 0 \\ 0 & 0 & 0 & 0 & -\frac{1}{C_2(R_L+r_{C2})} \end{bmatrix}$$

(5)

The mode-1 input matrix B_1 can be written as follows:

$$B_1 = \begin{bmatrix} \frac{1}{L_1} & 0 \\ 0 & \frac{1}{L_2} \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix}$$

(6)

Input current matrix P_1 for mode -1 as:

$$P_1 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \end{bmatrix}$$

(7)

Output matrix E_1 can be expressed as:

$$E_1 = \begin{bmatrix} 0 & 0 & 0 & 0 & \frac{R_L}{r_{C2}+R_L} \end{bmatrix}$$

(8)

Feed through matrix F_1 for mode -1 is expressed as:

$$F_1 = [0]$$

(9)

ANALYSIS OF MODE-2[(d_1*Ts)<t<(d_2-d_1)*T_s]:

MODE-2: The duration period of this mode is given as the $[(d_1*T_s)<t<(d_2-d_1)*T_s]$. In this operating mode of converter, the switch S_2 and the diode D_1 is ON while the switch S_1 and the diode D_2 is OFF.
The current of inductor L_1increase linearly while the current in inductor L_2 decreases linearly. The operating circuit diagram of Mode-2 of the integrated SEPIC- Buck Boost Converter is shown in Fig.7:

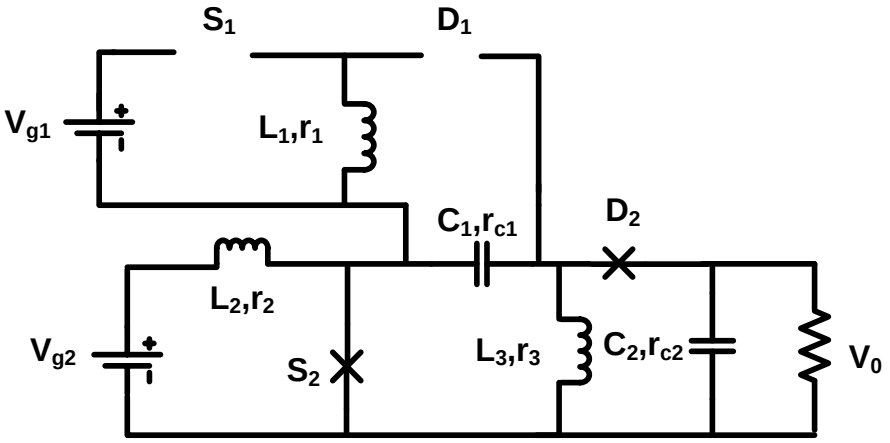

Fig.7. Equivalent circuit diagram of mode-2

State space matrix of mode-2:

$$A_2 = \begin{bmatrix} -(r_1 + r_{c1})/L_1 & 0 & 0 & -1/L_1 & 0 \\ 0 & -r_2/L_2 & 0 & 0 & 0 \\ -r_{c1}/L_3 & 0 & -\frac{r_3}{L_3} & 0 & 0 \\ -1/c_1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -\frac{1}{C_2(r_{C2}+R_L)} \end{bmatrix}$$

(10)

The mode-2 input matrix B_2 can be written as follows:

$$B_2 = \begin{bmatrix} 0 & 0 \\ 0 & \frac{1}{L_2} \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix}$$

(11)

Output matrix E_2 can be expressed as

$$E_2 = \begin{bmatrix} 0 & 0 & 0 & 0 & \frac{R_L}{r_{C2}+R_L} \end{bmatrix}$$

(12)

Input current matrix P_2 for mode -2 is :

$$P_2 = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \end{bmatrix}$$

(13)

Feed through matrix F_2 for mode - is expressed as:

$$F_2 = [0]$$

(14)

ANALYSIS OF MODE-3[(d_2-d_1)*T_s<t<T_S]:

MODE-3: The duration period of this mode is given as the [(d_2 -d_1)*T_s< t < T_s. In this operating mode of converter, the diode D_2 is ON and D_1 is off while the switch S_1 and the switch S_2 is OFF. This mode enables both the dc source transfer energy to the load at the same period of time. The operating circuit diagram of Mode-3 of the integrated SEPIC– Boost converter is shown in Fig.8:

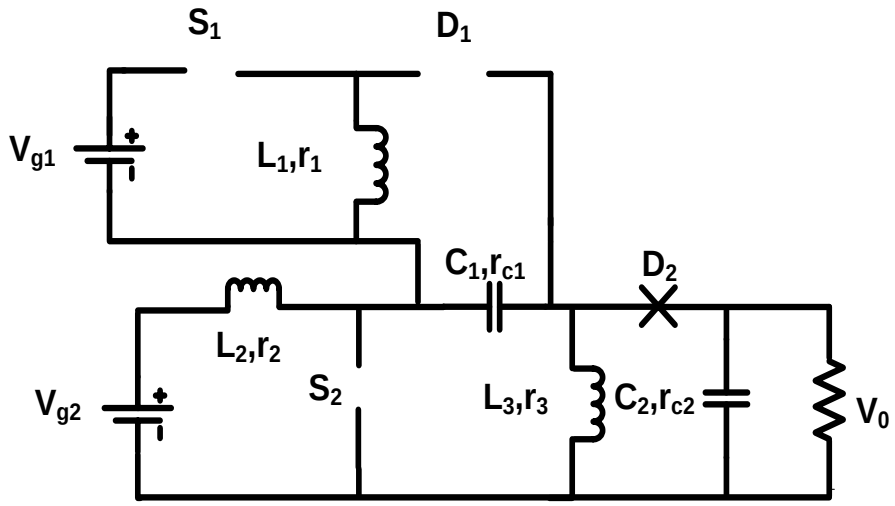

Fig.8 Equivalent circuit diagram of mode-3

State space matrix of mode-3

$A_3 =$

$$\begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & -(r_2 + rc1 + \frac{R_L r_{C2}}{R_L + r_{C2}})\frac{1}{L_2} & \left(\frac{R_L r_{C2}}{R_L + r_{C2}}\right)\frac{1}{L_2} & -\frac{1}{L2} & \left(\frac{-R_L}{R_L + r_{C2}}\right)\frac{1}{L_2} \\ 0 & \frac{1}{L_3}\left(\frac{R_L r_{C2}}{R_L + r_{C2}}\right) & -\left(r_3 + \frac{R_L r_{C2}}{R_L + r_{C2}}\right)\frac{1}{L_3} & 0 & \left(\frac{R_L}{R_L + r_{C2}}\right)\frac{1}{L_3} \\ 0 & \frac{1}{c1} & 0 & 0 & 0 \\ 0 & \frac{R_L}{C_2(R_L + r_{C2})} & \frac{-R_L}{C_2(R_L + r_{C2})} & 0 & \frac{-1}{C_2(R_L + r_{C2})} \end{bmatrix}$$

(15)

The mode-3 input matrix B_3 can be written as follows:

$$B_3 = \begin{bmatrix} 0 & 0 \\ 0 & \frac{1}{L_2} \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix}$$

(16)

Output matrix E_3 can be expressed as:

$$E_3 = \begin{bmatrix} 0 & \frac{R_L r_{C2}}{r_{C2} + R_L} & \frac{-R_L r_{C2}}{r_{C2} + R_L} & 0 & \frac{R_L}{r_{C2} + R_L} \end{bmatrix}$$

(17)

Input current matrix P_3 for mode -3 as:

$$P_3 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \end{bmatrix}$$

(18)

Feed through matrix F_3 for mode -3 is expressed as:

$$F_3 = [0]$$

(19)

IV. VOLTAGE SECOND BALANCE EQUATION

The volt-second balance equation, the average value of inductor voltage across inductor should be equal to zero.

For the Inductor L_1:

$$d_1 T_S V_{g1} + V_{c1}(d_1 - d_2)T_S = 0$$

(20)

For the inductor L_2:

$$d_1 T_s V_{g2} + (V_{g2})(d_2 - d_1)T_s + (1 - d_2)(V_{g2} - Vc1 - V_O)T_s = 0$$

(21)

$$V_0 = \frac{V_{C1} d_2}{1 - d_2}$$

(22)

For the inductor L_3:

$$d_1 T_S(-V_{C1}) + (d_1 - d_2)(-V_{C1})T_S + T_S V_O(1 - d_2) = 0$$

(23)

From equation (21) and (23):

$$V_O = \frac{V_{g1} d_1}{d1 - d_2} + \frac{V_{g2}}{1 - d_2}$$
(24)

Equation (24) provides the load voltage expression. This equation shows that the converter is providing boosting action with regard to source 2 and bucking action with respect to source 1. The voltage gain expression of the MIC is dependent on the duty ratio of both switches and the amplitude of both input DC sources, as may be inferred from equation (24).

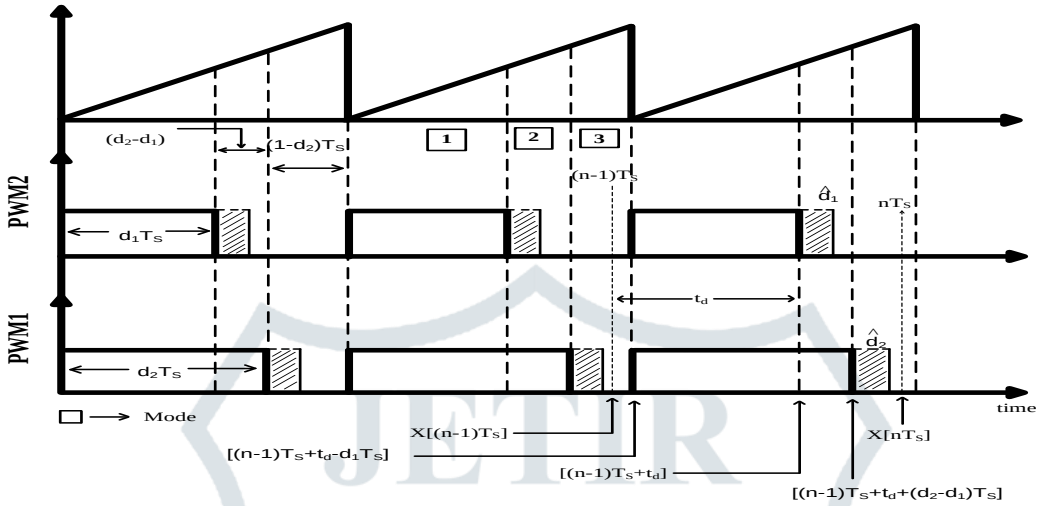

Fig.9. Waveforms for trailing-edge OFF-Time sampling.

Detailed Discrete-time modelling of the converter in detail has been already covered in ref [10].
The suggested two input converter is modelled in discrete time , and taken from one full sample period ($[(n-1)T_S]$ to $[(nT_S)]$. Below is list of each time interval;

For Interval 1: $(n\text{-}1)T_S < t < [(n-1)T_S + t_d - d_1T_S]$
(25)

For Interval 2 : $[(n-1)T_S + t_d - d_1T_S] < t < [(n-1)T_S t_d]$
(26)

For Interval 3: $[(n-1)T_S + t_d] < t < [(n-1)T_S + t_d + (d_2 - d_1)T_S]$
(27)

For Interval 4: $[(n\text{-}1)T_S + t_d + (d_2 - d_1)T_S] < t < [nT_S]$
(28)

The small – signal model for the converter that is being studied in the discrete – time domain takes the following typical form:

$X[nT_S] = \emptyset X[(n\text{-}1)Ts] + \gamma 2 d1\ [(n\text{-}1)Ts] + \gamma 1 d2[(n\text{-}1)Ts]$
(29)

Where;

$\emptyset = e^{ATs}$
(30)

$Y_1 = k_1 T_s e^{[A1(d1-d2)Ts + A2(Ts - td - d2Ts)]}$
(31)

$Y_2 = k_2 T_s e^{[A3(Ts - td - d1Ts + d2Ts)]}$
(32)

V. CONVERTER SPECIFICATIONS

For designing the converter in open loop simulation, there should be a specified value of the use parameters. The respective value of each parameter is mentioned below:

Table.2.DESIGN EXPRESSION AND PARAMETER VALUES

DESIGN PARAMETER	EXPRESSION	VALUE OF PARAMETER
L_1	$\frac{Vg1 * d_1}{fs * (\Delta iL_2)}$	100 µH
L_2	$\frac{Vo * d_1}{fs * (\Delta iL_2)}$	100 µH
L_3	$\frac{Vo * (1 - d1)}{fs * (\Delta iL_3)}$	100 µH
C_1	$\frac{iL_3 * d1}{fs * (\Delta vc1)}$	60 µF
C_2	$\frac{i_0 * (d_2 - d_1)}{fs * (\Delta vc2)}$	60 µF

Table.3.CONVERTER SPECIFICATION

PARAMETERS	NUMERICAL VALUES
Power rating	P ≈ 177 W
DC Load voltage	Vo = 48 V
DC source voltage	Vg2 = 36 V, Vg2 = 24
Current ripple	Less than 10%
Voltage ripple	Less than 5%
Switching Frequency	50khz

VI. SIMULATION STUDIES AND EXPERIMENTAL RESULT

Observe the stable voltage and current waveform and use PSIM software to simulate it. Use PSIM software to analyze stable and current waveform. Stable inductor current load voltage and load current waveform.

The stability study of the converter can be completed after the transfer function of the plant and controller are determined (Fig.10.) displays the converter's pole-zero map, where every pole and zero is located inside a unit circle, producing a stable closed-loop structure.

$$Gt_1 = \frac{-0.5927Z^4+1.692Z^3-1.269Z^2-0.1413Z+0.3109}{Z^5-4.026Z^4-4.446Z^2+1.38Z-0.1137} \quad (33)$$

$$Gt_2 = \frac{0.006139Z^4-0.06029Z^3+0.06213Z^2+.006995Z-0.01236}{Z^5-4.026Z^4+6.025Z^3-4.446Z^2+1.38Z-0.1137} \quad (34)$$

$$Gt_3 = \frac{8.23Z^4-24.79Z^3+25.87Z^2-10.23Z+.916}{Z^5-4.026Z^4+6.205Z^3-4.446Z^2+1.38Z-0.1137} \quad (35)$$

$$Gt_4 = \frac{0.5071Z^4-1.488Z^3+1.4Z^2-0.3645Z-0.05451}{Z^5-4.026Z^4+6.205Z^3-4.446Z^2+1.38Z-0.1137} \quad (36)$$

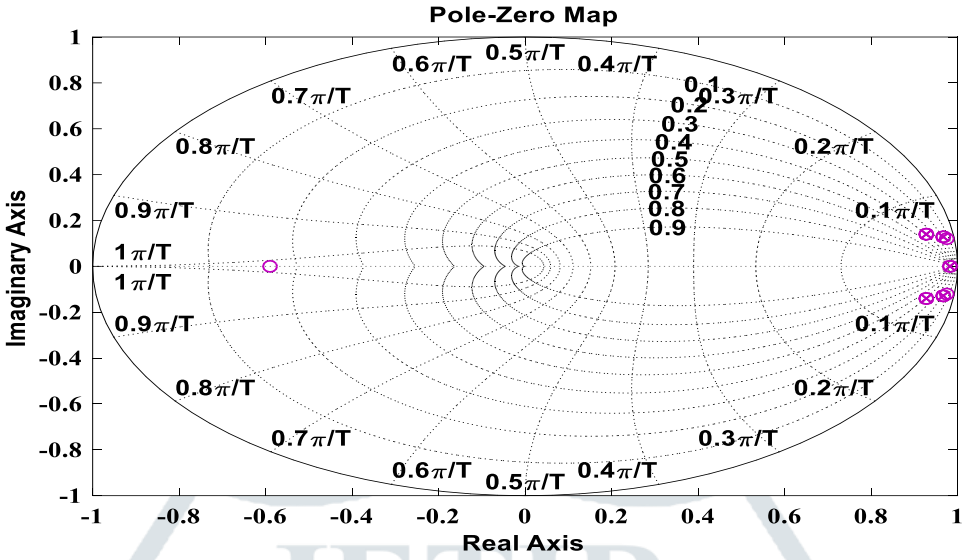

Fig.10. Pole Zero plot of the transfer function

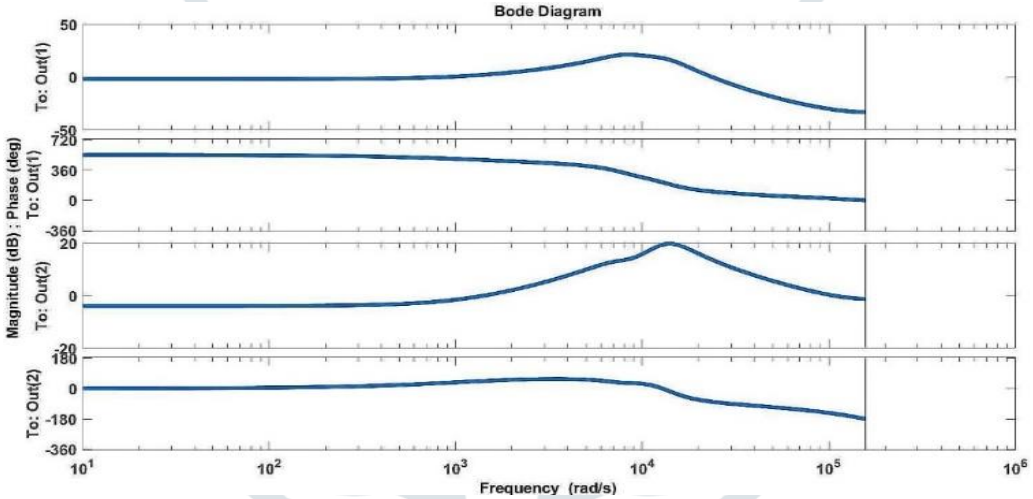

Fig.11 Step response of output voltage Vo

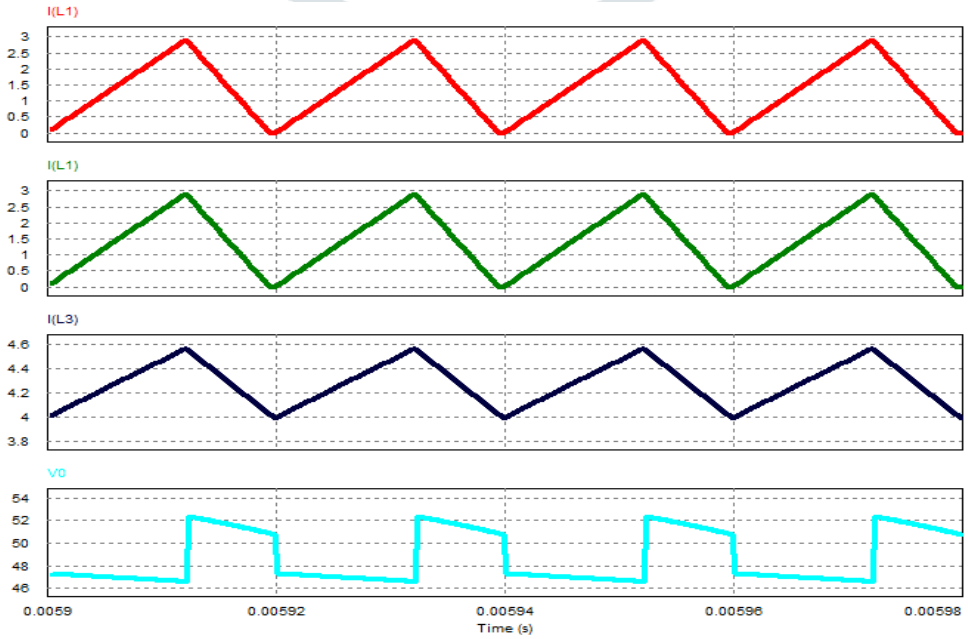

Fig.12 Study state waveform of inductor and load current

VII. CONCLUSION

We shall offer a two-loop digital control technique for a two-input integrated converter. Two-decoupled digital controllers one for load voltage regulation and the other for LVS current control—will be used to accomplish this. To create workable input and output, control, and power distribution between the source voltage, the RGA theory will be utilized. This chapter examined the interaction effects of control loops, and the optimal pairing of control variables (d_1 is used to control ig_1, whereas d_2 is used to regulate V_0) was found as a consequence of the study. The effective transfer function approach was used to construct the decentralized controllers for the MIC. PID controllers were created using this transfer function model as the foundation for the technique, which required converting the plant transfer function into a second-order plus time delay model. The resulting decentralized controller produced acceptable dynamic performance in addition to the anticipated power management, it is concluded in light of this transformation and the model formulation. Simulation studies were used to illustrate the converter's dynamic performance in the face of external disturbances. By factoring, robustness was determined.

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