



AN ENERGY EFFICIENT FIR FILTER USING COMPRESSOR TREE TECHNIQUE HIGH SPEED DSP APPLICATIONS

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Abstract— Approximate computing is one of the best data processing methods suitable for complex applications, such as coding and image processing, computer vision, machine learning, data mining, etc. Approximate calculations reduce accuracy, which is good because the cost of improving circuit characteristics depends on the application. Perfection is a threshold that governs the trade. In this process, rounding methods are introduced as a good way to manage this trade. In this case, the multiplier circuit, as the main computing building block in most processors, has been proposed to evaluate the efficiency of the rounding methods. The effect of rounding methods is studied by comparing the properties of multiplier circuits.

I.INTRODUCTION

Coefficients are one of the most important components in computing and are used in various digital signal processors. A variety of computer system applications such as computer graphics, computer science, and image processing are increasingly demanding high-speed processors. The speed multiplier determines how fast the processor can work, and designers are increasingly focusing on speed and low power consumption. A multiplicative architecture consists of a product-creating part, a product-minimizing part, and a final additive part. The profit margin is a large part of the total multiplier, power, and spread. Therefore, to accumulate a part of the product, the compressor uses this part and the multiplexer. The XOR-XNOR circuit is also a form of construction because it helps to reduce phase gain and

also helps to reduce the critical path, which is very important to maintain circuit performance. This is achieved by using a 3-2, 4-2, 5-2 compressor configuration. 3-2 Steppers are also called full lift units. Since these machines are also used in larger systems, better design can play a major role in system performance. The internal structure of the compressor is a series of XOR-XNOR gates such as counting circuits, multipliers, compressors, and parity checkers. In this work, a new XOR-XNOR module is introduced and a 4-2 compressor is implemented using this module. The use of the proposed circuit in the partial product accumulator reduces the number of transistors as well as the power consumption. Addition and multiplication are commonly used operations in computer science; The additional parameters have been thoroughly analyzed for approximate statistics by Liang et al. These additions are compared, and several new metrics are proposed for the evaluation of near additions and potential additions, with an overview of their integrated benefits for the design evaluation of non-standard computing applications. For each circuit input, the error distance (ED) is defined as the calculated distance between the error output and the correct output. Considering the average effect of multiple inputs and the correction of multi-bit addition, mean error distance (MED) and normal error distance (NED) are considered. NED is slightly different from implementation metrics, so it is useful in assessing the reliability of a design. The trade-off between accuracy and

power is reevaluated quantitatively. However, little attention has been paid to the design of the estimates. Multiplication can be thought of as the repeated addition of partial products; however, approximate coefficients cannot be used when designing approximate coefficients because of uncertainties in accuracy, equipment complexity, and other performance metrics. Several coefficient estimates have been proposed. Most of these designs use the truncated coefficient method; they set the lowest column of partial products as a constant. Incorrect combination coefficients are used in neural network applications by eliminating some of the least significant bits of the partial product (thus eliminating some of the extras in the array). A truncated coefficient and correction constants are considered.

II.LITERATURE SURVEY

In this section, some previous work in approximate coefficients is briefly reviewed. Among them, approximate multiplication and approximation based on the broken array multiplier (BAM) technology are considered. By applying the BAM comparison method to the modified traditional Booth coefficient, a signed Booth coefficient is considered. decreased to 41.8%. Kulkarni et al. An approximate multiplier consisting of several 2×2 building blocks is considered, thus saving energy from 31.8% to 45.4% compared to the direct multiplier. The 32-bit signed multiplication calculator is designed for practical applications in pipeline engineering. In them, an error-multiplier is included that calculates the approximate result by dividing the coefficient into a correct part and a close part, where the accuracy for different bit widths is reported. In the case of a 12-bit multiplier, it is said to be greater than 50%. The use of approximate multipliers in image processing applications has been discussed in the literature, and can reduce power consumption, length, and transistor count compared to direct multiplier designs. Configurable Accuracy Multiplier Architecture (ACMA) is recommended for fault-tolerant systems. To increase productivity, the ACMA uses a technique called predictive modeling, which is based on pre-computer logic. Compared to the direct coefficient, the proposed approximate coefficient reduces the latency by approximately 50% by reducing the critical path. Furthermore, Bhardwaj et al. A tree Wallace multiplier (AWTM) is considered. This also calls for carrier prediction to minimize the critical path. In this study, AWTM was used for time-domain image application, achieving a 40% and 30% reduction in power and space, respectively, compared to using the Wallace Tree Multiplier (WTM) right, no image quality. disease formation. Multiplication and division are unsigned multiplications based on the specified logarithm operand approximation. In the proposed multiplication, the number of adjacent journals determines the productivity of the work. Therefore, the coefficient is reduced to some displacement and addition operations. A method is proposed to improve the accuracy of multiplications 18. It is based on integrated operand decomposition. This approach greatly increases the average error at the cost of approximately twice the device size of the estimated coefficient. A dynamic segmentation method (DSM) is proposed, which performs the multiplication operation in m-bit segments starting from the significant bit of the input operand. A dynamic range multiplier (DRUM)

has been proposed that selects m -bit segments starting from the previous bit of the input operand and sets the least significant bit of the truncated value to 1. In this structure, the truncated value is multiplied and shifted to the left to produce the final output. A 4×4 WTM calculation using the wrong 4:2 counter is specified. In addition, an error correction unit is considered to correct the output. To create larger coefficients, these 4×4 inexact Wallace coefficients can be used in an array configuration. Most of the approximate coefficients previously considered are based on modifying the structure or reducing the complexity of some direct coefficients. In this paper, we propose to do the approximation by simplifying the function. The difference between our work and previous work is that although the principles of both works are the same for unsigned numbers, the average error of our proposed method is smaller. In addition, we recommend using some approximation method when doing multiplication with signed numbers

III. EXISTING METHOD

MULTIPLICATION ALGORITHM OF ROBA MULTIPLIER

The main idea behind the proposed approximate multiplier is to make use of the ease of operation when the numbers are two to the power n (2^n). To elaborate on the operation of the approximate multiplier, first, let us denote the rounded numbers of the input of A and B by A_r and B_r , respectively. The multiplication of A by B may be rewritten as

$$A \times B = (A_r - A) \times (B_r - B) + A_r \times B_r + B_r \times A - A_r \times B_r.$$

The main observation is that the reactions $A_r \rightarrow B_r$, $A_r \rightarrow B$, and $B_r \rightarrow A$ can only be done by displacement. However the instrumental implementation of $(A_r \rightarrow A) \rightarrow (B_r \rightarrow B)$ is very difficult. This term has little weight in the final result, depending on the difference between the exact number and the rounded number. Therefore, it is recommended that this section be omitted to aid in the multiplication process. Therefore, to carry out the multiplication process, the following expression is used: In this method, the approximate values of A and B should be determined in the form of 2^n . If A (or B) has a value equal to $3 \times 2^{p-2}$ (where p is a positive integer greater than 1), it has two adjacent values of the form 2^n and their absolute differences equal to 2^p and $2^p - 1$.

Although the two values have the same effect on the accuracy of the coefficient considered, choosing the larger value (except for the case of $p = 2$) results in a lower tool implementation for determining the rounding value almost. It is based on the fact that numbers of the form $3 \times 2^{p-2}$ are said to be insensitive to rounding up and down, so it is easy to do, and if it is used for rounding up, there are fewer logical statements. The only exception is three, and two is considered the closest value among the coefficient estimates.

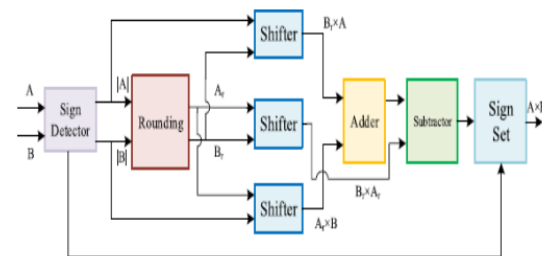


Figure 1: Block Diagram For The Hardware Implementation Of The Roba

It should be noted that, in contrast to previous studies where the estimated results were lower than the correct results, the final results calculated with the RoBA coefficient may be higher or lower than the correct results, depending on the amount of A_r and B_r compared to products. product. and B . Note that if one operand (for example, A) is less than its rounded value, and the other operand (for example, B) is greater than its rounded value, the result will be closer to the result right. Because, in this case the product $(A_r - A) \times (B_r - B)$ will be negative. Since the difference between the two is the result of this result, the approximate result is greater than the exact result. Similarly, if A and B are greater than (or less than) A_r and B_r , the approximate result will be less than the exact result. Finally, it should be noted that the proposed RoBA coefficient effect applies to positive inputs, because the rounded value of negative inputs does not reach the form 2^n in the two's complement sign. Therefore, it is better before starting the multiplication operation, determine the absolute value of the two inputs and the sign of the output product of the multiplication according to the sign of the input, and then perform the operation to on an unsigned number. It should be noted that the pre-estimated profit is less than the Performance and direct profit. On the other hand, the final profit calculated with the RoBA coefficient can be more or less than the direct profit, depending on amounts of A_r and B_r

compared to. the right result. size A and B respectively. Note that if one operand (for example, A) is less than its rounded value, and the other operand (for example, B) is greater than its rounded value, the result will be closer to the exact result. Because, in this case the product $(Ar - A) - (Br - B)$ will be negative.

IV.PROPOSED METOD:

FIR Filter using ROBA Multiplier

Finite Impulse Response (FIR) filters are widely used in digital signal processing (DSP) applications due to their stability and linear phase characteristics. End-to-end feedback filters are critical components in signal processing and communications. Spatial and speed optimization are key requirements for small feedback filters. Finite feedback filters include multiplication, addition, and shift operations. Since the multiplier is the slowest part of the system, it affects the performance of the FIR filter. In today's environment, low power consumption and small space are the most important parameters for building DSP and high performance systems. Currently, many Finite Impulse Response (FIR) filter designs have been developed that focus on small areas, high speed, or lower power consumption. As the area increases, so does the hardware cost of these FIR filters. This leads to the design of low-bandwidth FIR filters with the advantage of high-speed operation. Implementing an FIR filter has three basic construction steps. That is multiplication, addition and signal delay. The coefficient is the most important part of the FIR filter design. Since the multiplier is the slowest part of the system, it affects the performance of the FIR filter. Here, the traditional coefficient is replaced by the modified ROBA coefficient.

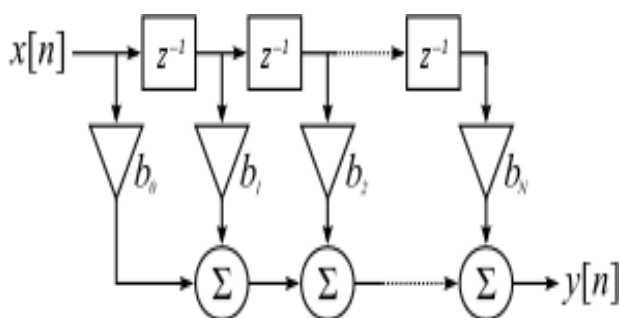


Figure 2. Conventional FIR filter

As the multiplier is the slowest element in the system, it will affect the performance of the FIR filter. So, a ROBA multiplier is suggested since it reduces area and it is faster than other conventional multipliers. The proposed low area-cost FIR filter using a ROBA multiplier is shown in Figure below.

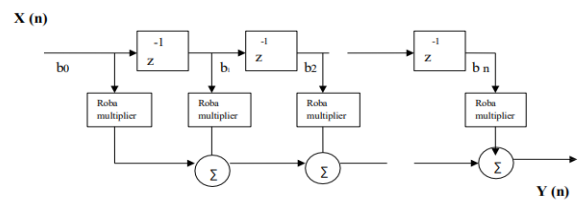


Figure 3: FIR filter using ROBA multiplier

V.RESULTS

1) Existing results

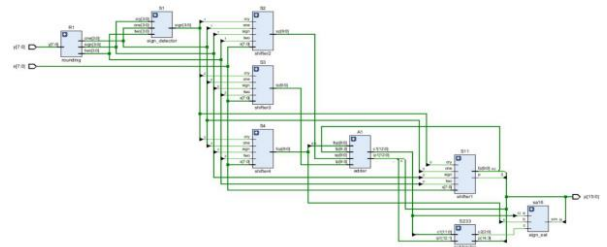


Figure 4: RTL schematic



Figure 5: Area and Power Consumption

Timing Report

Slack: inf

Source: x[4] (input port)

Destination: p[13] (output port)

Path Group: (none)

Path Type: Max at Slow Process Corner

Data Path Delay: 11.930ns (Logic 4.520ns (37.886%) route 7.410ns (62.114%))

Logic Levels: 9 (IBUF=1 LUT3=2 LUT4=1 LUT5=2 LUT6=2 OBUF=1)

| Location | Delay type | Incr (ns) | Path(ns) | Netlist Resource(s) |
|----------|------------|-----------|----------|---------------------|
| | | | | |

Figure 6: Delay

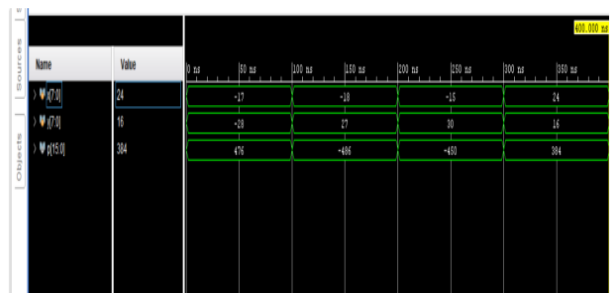


Figure 7: Simulation results

2) Proposed results

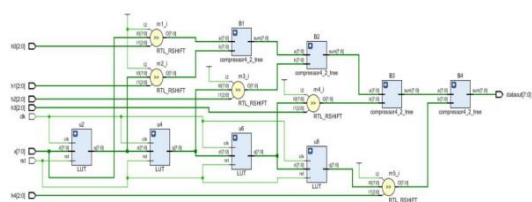


Figure 8: RTL schematic

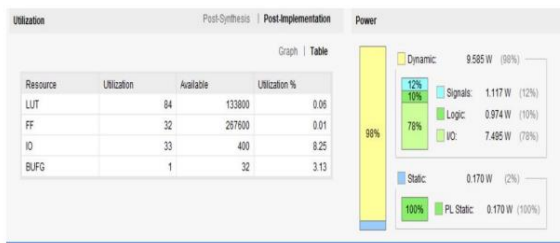


Figure 9: Area and Power Consumption

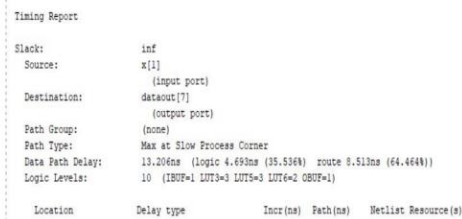


Figure 10: Delay



Figure 11: Simulation results

VI.CONCLUSION

In this paper, we consider a speed and power-efficiency coefficient, called the RoBA coefficient. The coefficient considered is very accurate and based on rounding the input in the form of $2n$. In this way, the part of the multiplication is eliminated, thus increasing the speed and effort on the basis of smaller errors. The proposed method can be used for both signed and unsigned coefficients. Three practical applications of approximate coefficients are discussed, including one for unsigned functions and two for signed functions. The efficiency of the proposed coefficient is assessed by comparing it to several different direct and approximate coefficients using different design parameters. The results show that in most (all), the architecture RoBA coefficients are higher than the corresponding (correct) coefficients. This work was extended to implement a sweep filter using the roba coefficient. This is a great advantage in reducing space.

FUTURE SCOPE

This multipliers plays a very important role in our day to day life. In future the multipliers are going to play a major role. The speed of the multipliers are increased by using carry save adders, carry look ahead adder, and so on. Rounding patterns will be optimized based on required accuracy and different compression techniques. The area and delay can be reduced in future by using advanced technology.

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