DESIGN OF POWER EFFICIENT REVERSIBLE MULTIPLIER

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ABSTRACT

Reversible computing is a new area of research with applications in quantum technology, nanotechnology, and low-power design. It turns out that reverse logic reduces power consumption. This is in stark contrast to traditional multiplicative logic such as addition and multiplication. Some aspects of the multifaceted architecture development process. A multiplier design using different logic gates is considered here. The power consumption of the multiplier design is compared with the conventional multiplier.

I.INTRODUCTION

Low power consumption is a major problem in current VLSI circuits. As the size of the transistor has decreased, IC designers have faced two major problems. The motivation to study reversible adiabatic circuits initially came from the increasing need for low power flow computing. Switchable circuits also play an important role in supercomputers [6] and emerging nanotechnology. To properly ensure integrated circuit performance and durability; Testing and failure analysis are important during the later stages of design and manufacturing. An important consideration for fault location in future parallel logic systems is on-site self-healing and replacement of faulty components. We will show that this process is easier when the circuit is changed. The fault location can be used for manual or automated diagnostic and repair work. In an automated process, a circuit is created with redundant components, when a fault is detected, the circuit is reconfigured by replacing the faulty component with the correct redundant component. This chapter is devoted to the basic information and explanations necessary to navigate smoothly in the world of reverse logic. First, some basic concepts of reverse logic are introduced. Basic and quantitative definitions of reverse logic are explained. Next, three reversible gates are described: Feynman, Toffoli, and Fredkin. Below is an interesting heuristic for reverse logic synthesis. Just like everyday life, everything has a price. The cost of inversion is that it produces "garbage" that is unacceptable in quantum computing and must be eliminated by interpretation. In recent years, switching logic has attracted much attention due to its ability to reduce power consumption, which is a key requirement for low-power VLSI designs. It has many applications in low-power CMOS and optical information processing, DNA computing, quantum computing, and nanotechnology. The statistics of non-convertible devices consume energy due to loss of information. According to Randall's research, each immutable bit has a lot of potential. The minimum work is $KTln2$ Joules, and $K=1.3806505*10-23m2kg-2K-1$ (Joule/Kelvin-1) is Boltzmann's constant and T is the temperature when the work is done. At room temperature, the heat generated by

the loss of a small amount of information is very small, but when the number of bits is large (such as in a high-speed computer), the heat can be very large and lose, affect work and work. . , Bennett showed that KTln2 energy does not disappear from the system as long as the system allows the input to produce the detected output. Reverse logic supports the system's control mechanisms in both forward and reverse directions. This means that the conversion software can produce an input from an output, and then return to a point in the calculation. A circuit is said to be invertible if the circuit can reproduce the input vector from the output vector, and there is a one-to-one correspondence between the input function and the output, i.e. not only the output can be determined independently of the input. , but if the calculation information is not lost, the input can also be recovered from the output, which can reduce or eliminate the power supply.

II.LITERATURE REVIEW

(1) Majeed Hagparast et al. [1] They proposed a new 4x4-bit multiplier circuit. Switching coefficients are faster and the equipment is less complex than other similar coefficients for multiple gates, waste output and continuous input. They use the HNG gate proposed by Haghparast and Navi. The reversible HNG gate can only be used as a reversible switch. The proposed inverting multiplier circuit multiplies two 4-bit binary numbers using HNG gates.

(2) Biswas, AK et al. [2] proposed a better and more efficient inverting logic implementation of point-to-point (BCD) addition and carry-forward BCD addition. The revised design was found to be superior to the current design in terms of number of doors, number of exhaust outlets, durability, and cost. To demonstrate the robustness of the proposed design, the lower limits of the door are also provided with the waste versions of the BCD attachment that can be changed. This circuit can be used to design an inverting speed multiplier unit.

(3) James RK et al. [3] proposed fast point-to-point adder (QAD) suitable for multi-bit BCD adder, using inverting logic. This design uses

reversible Fredkin gates. The implementation strategy is to reduce the level of the area by increasing the speed, which is the most important for high speed areas. This can also be done quickly.

(4) Thapliyal H.M., Arabia H.R. [4] This paper proposes a reversible logic architecture (RPLA) using Fredkin and Feynman switching gates. The proposed RPLA has n inputs and m outputs, which can be used as m functions of n variables. To demonstrate the RPLA design, a 3-input RPLA was designed.

(5) H.M.H. Babu and A.R. Chowdhury [5] proposed a comprehensive method to implement a two-point additive circuit. First, an additional switchable circuit is considered, showing improvements over both circuits.

(6) Himanshu Thapliyal and M. B. Srinivas [6] proposed a multiplicative NXN using TSG gates based on two principles. First, the partial results are made parallel using a reverse d gate, and second, the addition can be reduced to log2N steps by designing an inverting parallel adder using a TSG gate.

(7) Shuli Gau et al [7] An efficient system design technique and approach to implement the multiplication of large integers and quadratic functions using embedded small coefficients. A general architecture for multiplication and quadrature is considered, and a set of equations is derived to aid implementation.

(8) H. Thapliyal and M.B. Srinivas [8] proposed a reversible half adder and reused the new 3x3 reversible TKS to design a fully reversible adder, where two versions were used. as a 2:1 multiplexer device.

III.EXISTING METHOD

MAC Architecture

In this section, we present the two-level (i.e., two-cycle) MAC architecture. The first part handles the PPG process, the PPR process (based on the PPM that combines the PPG results and the accumulated results), the addition of (2N-k-1)

bits (a part of last addition), and addition of α-bits. (used to handle the PPR process) overflow). The second stage adds (k+α) bits to produce the summed result. The main features of the proposed architecture are as follows. In order to reduce the length of the transport, we introduce some additions to the PPR process. To handle overflow during PPR, an α-bit addition is used to calculate the total number of carries. Using gate technology, only the second stage can be performed in the last cycle (of the entire set of multiplier-accumulator operations) to save energy. The proposed two-layer pipe MAC section is shown in Figure 2. For unsigned MAC units, in the PPG process, gates can be used directly to generate PPM. For signed MAC units, since the influence of the signal bit must be taken into account, several PPG algorithms are proposed to generate signed PPMs. In the proposed architecture, the Baugh-Wooley algorithm is used in the PPG process to generate the signed PPM.
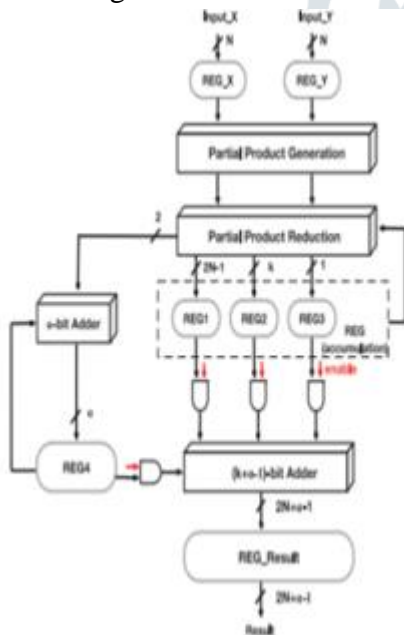

Figure 1:MAC Architecture

We have implemented a tool (a C++ program) to automatically generate the proposed N-bit MAC in Verilog RTL description. The users can specify the value of N and the value of k for automatic generation, where k denotes the number of higher significance bits whose additions (accumulation) are not performed in the final addition. Note that the value of k is equal to the bit width of register REG2.

IV.PROPOSED METHOD:

Implementation of reversible fault tolerant 4×4 Multiplier

The design of the multiplier is based on parallel operation is done using two steps. Part I: Partial Product Generation

Part II: Reversible Fault Tolerant Parallel Adder

As mentioned before, the purpose of this work is the design of reversible fault tolerant multiplier circuit with the aim of optimizing its hardware complexity to make it more economical in terms of number of garbage outputs and constant inputs without losing its efficiency.

The multiplier is implemented using fault tolerant reversible gates. The operation of a 4×4 reversible multiplier is shown in Figure. It consists of 16 Partial product bits of the four bit inputs X and Y to perform 4×4 multiplications. Figure show example of 4×4 bit multiplication.

Figure 2: Multiplication of 4×4 bit

V.RESULTS:

Figure 3: Power and Utilization of the design

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Timing Report

Slack:           inf
  Source:        a[1]
                   (input port)
  Destination:   c[13]
                   (output port)
  Path Group:    (none)
  Path Type:     Max at Slow Process Corner
  Data Path Delay: 9.454ns  (logic 3.932ns (41.593%)  route 5.522ns (58.407%))
  Logic Levels:  13  (CARRY4=4 IBUF=1 LUT3=1 LUT4=2 LUT6=4 OBUF=1)

  Location       Delay type        Incr(ns)  Path(ns)   Netlist Resource(s)
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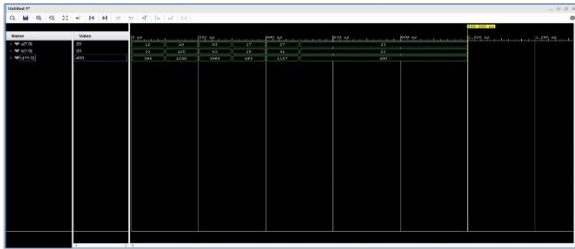
Figure 4: Data path delay

Figure 5: Timing Diagram

VI.CONCLUSION

Computer hardware has grown in power at an amazing pace ever since. The most important computational resources is energy which is deeply linked to the reversibility of the computation. The primary objective of this project was to gain insight into the Reversible Computation and its use for making devices energy efficient for long life. Multiplier is a basic arithmetic cell in computer arithmetic units and it is supposed to be the most power consuming unit when higher order multiplication is to be performed. In this work, looking at advantages of reversibility, we synthesized a parity preserving reversible multiplier circuit with the help of existing fault tolerant Fredkin, F2G and IG gate.

FUTURE SCOPE

Our discussion focuses on inverting logic—the idea that the input and output of an inverting logic gate can be removed independently of each other. Therefore, researchers face many challenges before they can translate reverse logic into a viable competitive technology, such as: (i) An efficient assembly method is required to make complex switching units; (ii) Optimization algorithms are required to reduce inconsistencies and artifacts; (iii) Test and verification tools for reverse logic design. Coupled with the growth in speed and complexity of computer systems, there are trends that these technologies must rely on to achieve the smallest electronic computer. If it is possible to implement an error-free regression design and build a classical regression software, then it is worth comparing to produce error-free results. Therefore, the main challenge is to handle the complex circuits in classical computers and to design more efficient reverse circuits. Although the future of reverse-logic circuits looks promising, this is only one approach to power-free distribution systems. If it is possible to implement an error-free regression design and build a classical regression software, then it is worth comparing to produce error-free results. Because addition/subtraction is the basic building block of any digital circuit; can be used to design error-free complex units such as ALUs. Therefore, the main challenge is to handle the complex circuits in classical computers and to design more efficient reverse circuits.

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