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Performance Comparison of H-Bridge, H5, and H6 Inverter Topologies for Transformerless Grid-Connected Photovoltaic Systems: A Comprehensive Review

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Abstract : This paper presents a comprehensive review of H-Bridge, H5, and H6 inverter topologies for transformerless grid-connected photovoltaic (PV) systems. Transformerless inverters have gained significant attention due to their higher efficiency, reduced size, lower cost, and improved power density compared to transformer-based counterparts. However, the absence of galvanic isolation introduces challenges related to common-mode voltage (CMV) fluctuations and leakage currents, which pose safety hazards and can affect system performance. This review systematically analyzes and compares the H4 (conventional full-bridge), H5, and H6 topologies in terms of efficiency, leakage current suppression, total harmonic distortion (THD), component count, and control complexity. The paper also discusses various modulation strategies, safety standards compliance (VDE 0126-1-1, IEEE 1547), and the impact of wide-bandgap semiconductor devices on inverter performance. Research gaps and future directions, including AI-based optimization and wide-bandgap integration, are identified to guide future research efforts in this domain.

IndexTerms **- Transformerless inverter, H5 topology, H6 topology, common-mode voltage, leakage current, photovoltaic systems, grid-connected inverter.**

I. INTRODUCTION

The global push toward renewable energy has led to a significant increase in photovoltaic (PV) installations, with cumulative installed capacity exceeding 1 terawatt (TW) in 2022 [1]. Single-phase grid-connected PV systems, particularly in residential applications, require efficient and reliable power conversion from DC (generated by PV panels) to AC (fed into the utility grid). Inverters serve as the critical interface in this power conversion process [2], [3]. Traditionally, grid-connected PV inverters employed line-frequency transformers to provide galvanic isolation between the PV array and the grid [4]. While transformers ensure safety by eliminating direct electrical connection, they introduce significant drawbacks including increased weight, larger volume, higher cost, and reduced overall system efficiency due to transformer losses [5], [6]. These limitations have driven the development of transformerless inverter topologies.

Transformerless inverters eliminate the isolation transformer, which brings several advantages. They typically achieve higher efficiency because transformer-related losses are removed, often improving efficiency by about 1–2% [7]. They are also smaller and lighter since they no longer require bulky magnetic components [8]. In addition, they can cost less due to reduced materials and simpler manufacturing [9]. Finally, they generally offer improved power density because the overall system can be designed more compactly [10].

However, removing the transformer introduces a critical challenge: leakage current. In transformerless systems, parasitic capacitances exist between PV panels and the grounded mounting structure [11], [12]. Fluctuations in common-mode voltage (CMV) cause current to flow through these capacitances, creating safety hazards, electromagnetic interference (EMI), and potential system disconnection under safety standards [13], [14].

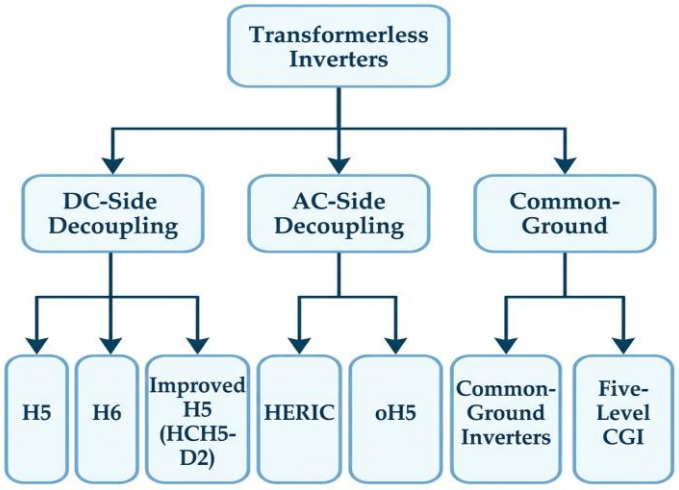


Figure 1: Classification of transformerless inverter topologies based on decoupling method

To address this challenge, various H-bridge derived topologies have been developed, including the H5 (commercialized by SMA Solar Technology AG) and H6 inverter families [15], [16]. These topologies employ additional switches and modified modulation strategies to maintain constant CMV, thereby minimizing leakage current while preserving high efficiency [17].

This paper provides a comprehensive review of H-Bridge (H4), H5, and H6 inverter topologies by discussing the theoretical foundations of common-mode voltage and leakage current, followed by a detailed analysis of the different topologies and their operating principles. It also includes a quantitative comparison of performance, examines modulation strategies and their impact on system behavior, addresses relevant safety standards and compliance requirements, and outlines potential directions for future research.

II. THEORETICAL BACKGROUND

2.1 Common-Mode Voltage and Leakage Current

In transformerless PV systems, the absence of galvanic isolation creates a conductive path through which common-mode currents can flow [18]. The common-mode voltage (CMV) is defined as the average of the voltages from the inverter output terminals to a reference point (typically the negative DC bus):

$$V_{cm} = (V_{AN} + V_{BN}) / 2$$

where V_{AN} and V_{BN} are the voltages from output terminals A and B to the negative DC bus (N) [19].

The leakage current flows through the parasitic capacitance (C_{pv}) between the PV array and ground, driven by CMV fluctuations [20]: $I_{leak} = C_{pv} \times d(V_{cm})/dt$. This relationship reveals the fundamental principle for leakage current suppression: maintaining constant CMV eliminates the driving force for leakage current [21].

2.2 Parasitic Capacitance in PV Systems

The parasitic capacitance between PV panels and ground varies significantly with installation and environmental conditions [22], [23], and this variation directly affects leakage current behavior in transformerless PV systems.

Table 1: Factors Influencing Parasitic Capacitance Between PV Arrays and Ground

Factor	Impact on Cpv
Panel technology	Thin-film: 50-150 nF/kW; Crystalline: 10-50 nF/kW
Mounting structure	Grounded frames increase capacitance
Weather conditions	Rain/humidity can increase Cpv by 2-5×
System size	Scales linearly with installed capacity

Panel technology is an important factor, with thin-film modules generally exhibiting higher parasitic capacitance values than crystalline silicon modules due to their structural characteristics. The mounting structure also influences Cpv, as grounded or metallic frames tend to increase capacitive coupling to earth. Environmental conditions such as rain or high humidity can substantially raise parasitic capacitance, sometimes by several times, while overall system size leads to a roughly linear increase in total capacitance with installed capacity. These effects highlight why accurate modeling of Cpv is important, as demonstrated by Xiao et al. [24], who developed detailed parasitic capacitance models that account for rainwater effects and their impact on leakage current analysis.

2.3 Safety Standards and Requirements

Table 2: Leakage Current Limits and Protection Requirements in International Standards for Transformerless Inverters

Leakage Current	Action Required	Response Time
> 30 mA	Monitoring	Immediate
> 100 mA	Protection	≤ 0.3 s
> 300 mA (peak)	Grid Disconnection	≤ 40 ms

Several international standards regulate leakage current limits for transformerless inverters [25], with specific requirements on allowable current levels and system response. The German standard VDE 0126-1-1 defines multiple leakage current thresholds and corresponding actions: leakage currents exceeding 30 mA must be continuously monitored with an immediate response, currents above 100 mA require protective action within 40 ms, and peak leakage currents greater than 300 mA mandate grid disconnection within 0.3 seconds. In addition, IEEE 1547-2018 specifies that DC current injection into the grid must be less than 0.5% of the rated inverter output [26], while also setting requirements for voltage and frequency ride-through performance as well as reactive power capability to ensure stable and compliant grid interaction [27].

III. Topology Analysis

3.1 H4 (Conventional Full-Bridge) Inverter

The H4 inverter consists of four switching devices (S1-S4) arranged in a full-bridge configuration [28]. While simple and cost-effective, the conventional H4 topology with standard modulation produces varying CMV, resulting in high leakage currents.

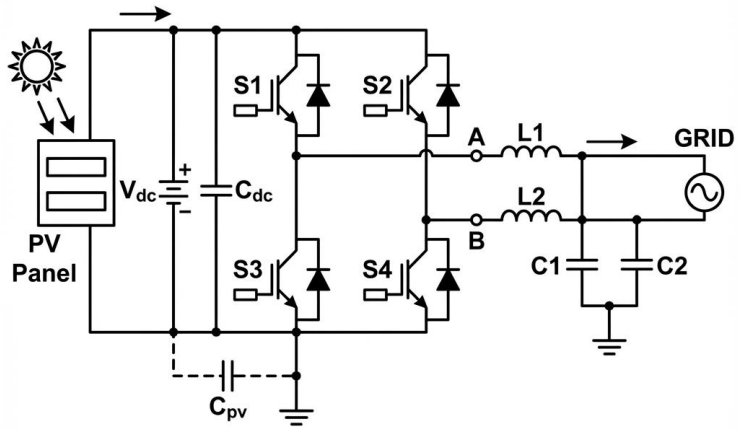


Figure 2: Circuit schematic of conventional H4 (full-bridge) inverter topology

Table 3: Operating Modes, Switch States, Output Voltage, and Common-Mode Voltage for an H-Bridge Inverter

Mode	Active Switches	Output Voltage	CMV
Positive	S1, S4	+Vdc	Vdc/2
Negative	S2, S3	-Vdc	Vdc/2
Zero+	S1, S3	0	0
Zero-	S2, S4	0	Vdc

In the positive mode, switches S1 and S4 are active, producing an output voltage of +Vdc and a common-mode voltage (CMV) of Vdc/2. In the negative mode, switches S2 and S3 are active, producing an output voltage of -Vdc while CMV remains Vdc/2. During zero states, the inverter can produce zero output voltage in two different ways: in the Zero+ mode, switches S1 and S3 are active, the output voltage is 0, and CMV is 0; in the Zero- mode, switches S2 and S4 are active, the output voltage is 0, and CMV becomes Vdc. The key observation from these operating modes is that although both zero states yield the same output voltage (0), they impose very different CMV levels (0 versus Vdc). This difference matters because CMV transitions between 0 and Vdc during zero states create high dV/dt, which drives substantial leakage current, typically greater than 800 mA [29]. Practically, this means the choice and sequencing of zero states in the modulation scheme can strongly influence leakage-current stress even when the output-voltage waveform looks similar.

Modulation strategy directly affects both harmonic performance and CMV behavior. With bipolar PWM, the inverter output switches between two levels (+Vdc and -Vdc) and CMV stays constant at Vdc/2, which helps suppress leakage-current excitation, but it typically comes with higher total harmonic distortion (THD) [30]. With unipolar PWM, the output becomes three-level (+Vdc, 0, -Vdc), which generally reduces THD, but CMV becomes variable because the modulation uses the zero states that shift CMV between 0 and Vdc [31]. This trade-off is central in transformerless designs: unipolar modulation can improve output quality, but it can also increase leakage current unless additional measures are used to control CMV variation.

3.2 H5 Inverter Topology

The H5 inverter topology, developed and commercialized by SMA Solar Technology AG, extends the conventional H-bridge by adding a fifth switch (S5) between the positive DC terminal and the H-bridge [32]. This additional switch enables DC-side decoupling during freewheeling modes, which is a key mechanism for reducing common-mode voltage variation and leakage current. Figure 3 illustrates the circuit schematic of the H5 inverter topology, highlighting the placement and function of the fifth switch (S5) for DC-side decoupling.

In terms of circuit configuration, the inverter consists of four H-bridge switches (S1–S4) that operate at the switching frequency, typically in the range of 10–50 kHz, and an additional switch S5 that operates at the grid frequency of 50 or 60 Hz. The primary role of S5 is to disconnect the PV array from the grid during zero or freewheeling states, thereby preventing rapid CMV transitions [33].

Figure 3: Circuit schematic of H5 inverter topology with fifth switch (S5) for DC-side decoupling

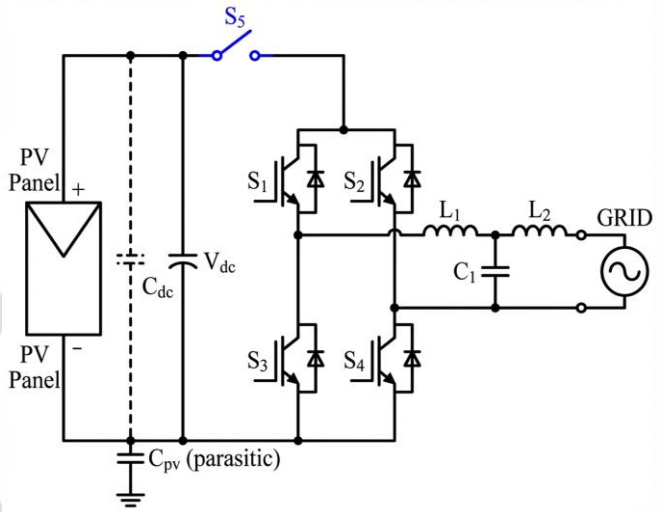


Table 4: Operating Modes, Current Paths, and Common-Mode Voltage in the H5 Inverter Topology.

Mode	Active Switches	Current Path	CMV
Positive Active	S1, S4, S5	3 switches	Vdc/2
Negative Active	S2, S3, S5	3 switches	Vdc/2
Freewheeling+	S1, S3	AC bypass	Vdc/2
Freewheeling-	S2, S4	AC bypass	Vdc/2

During positive active operation, switches S1, S4, and S5 conduct, establishing a current path through three switches and resulting in a common-mode voltage of Vdc/2. In negative active operation, switches S2, S3, and S5 are active, again involving three conducting switches and maintaining CMV at Vdc/2. In the freewheeling modes, S5 is turned off and the current circulates through the AC-side switches only. In the Freewheeling+ mode, switches S1 and S3 conduct, while in the Freewheeling− mode, switches S2 and S4 conduct. In both freewheeling states, the current bypasses the DC source and the CMV is clamped at Vdc/2. An important observation from this table is that, unlike the H4 topology, the H5 inverter avoids CMV transitions between 0 and Vdc during zero states, which significantly reduces dV/dt and associated leakage currents.

The H5 topology offers several advantages. It achieves a substantial reduction in leakage current, typically around 50 mA compared to approximately 800 mA in conventional H4 inverters [34]. Its structure is simpler than many other advanced transformerless topologies, and it has reached a high level of commercial maturity with proven long-term reliability in field applications. However, the topology also has notable limitations. Conduction losses are higher because three switches conduct simultaneously during active modes [35], and the fifth switch S5 is subject to significant thermal stress due to its continuous operation at grid frequency. Additionally, the H5 topology cannot efficiently supply reactive power, which limits its flexibility under modern grid-code requirements [36]. The asymmetric structure may also introduce CMV-related issues when parasitic effects are taken into account.

To address some of these limitations, several improved H5 variants have been proposed. The HCH5-D2 topology uses hysteresis control with two clamping diodes to improve CMV behavior [37]. The OH5 topology introduces mid-point clamping to enhance CMV stability [38], while the 2D-H5 variant employs a capacitor divider to maintain a stable CMV during freewheeling modes.

3.3 H6 Inverter Topology

The H6 inverter topology extends the H5 design by adding a sixth switch, typically placed between the negative DC terminal and the H-bridge, which provides greater switching flexibility and improved performance [39]. Figure 4 shows the circuit schematic of the H6 inverter topology, where the additional switches S5 and S6 enable enhanced decoupling of the PV array from the grid. A key feature of the H6 design is that the sixth switch creates a direct current path during one of the active modes, allowing the number of conducting switches to be reduced from three, as in the H5 topology, to two in certain operating states. This reduction in the conduction path leads to significantly lower conduction losses and improved efficiency [40].

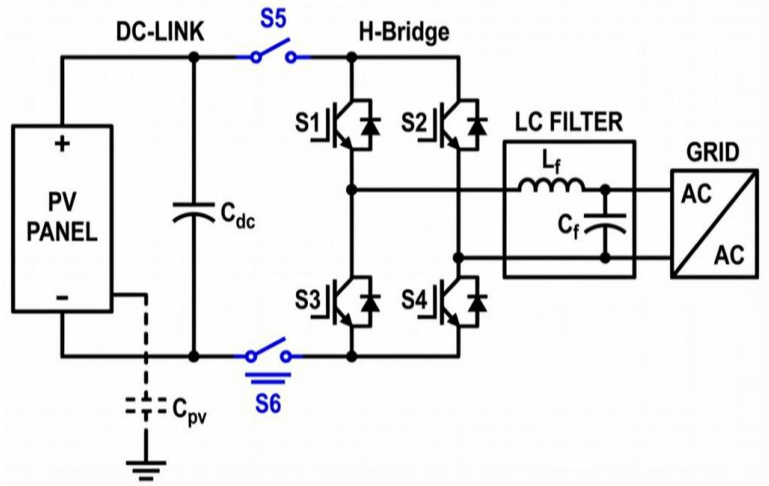


Figure 4: Circuit schematic of H6 inverter topology with switches S5 and S6 for enhanced decoupling

Table 5: Performance Comparison of H4, H5, and H6 Transformerless Inverter Topologies.

Parameter	H4	H5	H6
Leakage Current	803.10 mA	46.87 mA	42.47 mA
CMV Stability	Variable	Semi-constant	Constant
Typical Efficiency	~94%	~95-96%	~97-98%
Switch Count	4	5	6
Control Complexity	Low	Medium	Medium-High

The table compares the H4, H5, and H6 topologies in terms of leakage current, CMV behavior, efficiency, and implementation complexity. The H4 inverter exhibits high leakage current and variable CMV, whereas both H5 and H6 significantly reduce leakage current by improving CMV control. Among the three, the H6 topology achieves the lowest leakage current and maintains nearly constant CMV, which explains its superior efficiency, typically in the range of 97–98%. While the H6 topology requires an additional switch and more complex control than H4, its control complexity remains comparable to H5, making it an attractive trade-off between performance and implementation effort. Figure 5 further illustrates these differences by comparing the common-mode voltage waveforms of the three topologies.

Several H6 variants have been proposed to further enhance performance. The H6-I topology represents the basic sixth-switch extension [41], while H6-II and H6-III introduce modified freewheeling paths and improved clamping mechanisms, respectively. The IH6-BDC variant employs bidirectional diode clamping and has demonstrated a high efficiency of 97.91% at 3.1 kW, highlighting the potential of H6-based designs for high-performance transformerless PV inverters [42].

3.4 HERIC Topology Comparison

The HERIC (Highly Efficient and Reliable Inverter Concept) topology, developed by Sunways AG, offers an alternative approach to transformerless inverter design by employing AC-side decoupling rather than DC-side decoupling [43]. Although it is not the main focus of this review, the HERIC topology is commonly used as a benchmark when comparing the performance of H5 and H6 inverters. The topology uses six switches in total, consisting of a conventional four-switch H-bridge combined with two additional AC-side bypass switches. During freewheeling intervals, the AC-side decoupling isolates the DC source from the grid, which effectively suppresses common-mode voltage variation and results in very low leakage current. The HERIC inverter is also known for its excellent thermal stress distribution among the switches, contributing to high reliability and long-term operation. Peak efficiency values as high as 97.96% have been reported in the literature, further reinforcing its role as a high-performance reference topology for transformerless PV inverter comparisons [44]

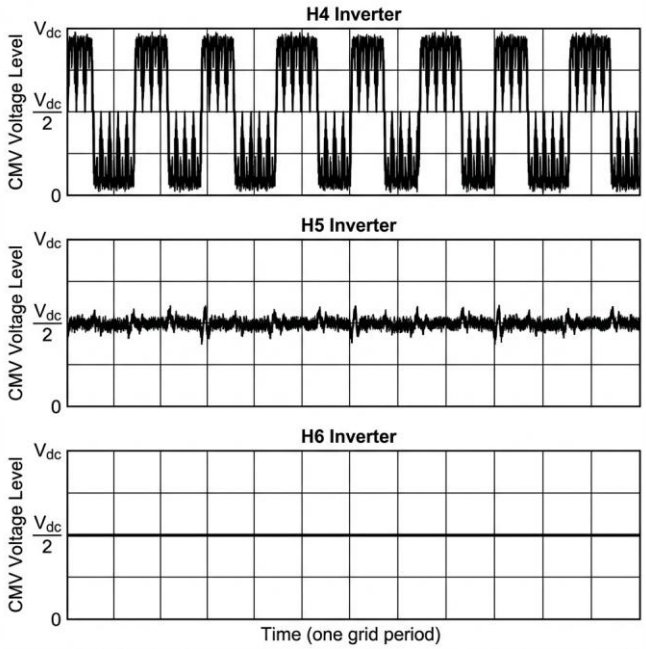


Figure 5: Common-mode voltage waveforms for H4, H5, and H6 inverter topologies

IV. Modulation Strategies

4.1 Bipolar vs. Unipolar PWM

The choice of modulation strategy significantly impacts both THD and common-mode voltage behavior [45].

Table 6: Comparison of Bipolar and Unipolar PWM Effects on THD, CMV, and Implementation.

Parameter	Bipolar PWM	Unipolar PWM
THD (no filter)	98.7%	53.8%
THD (with filter)	5-8%	2-4%
CMV Behavior	More stable	Variable
Switching Losses	Higher	Lower
Implementation	Simple	Moderate

The table shows that bipolar PWM typically produces much higher THD without filtering (98.7%) than unipolar PWM (53.8%), and even with a filter it usually remains in the 5–8% range compared with 2–4% for unipolar PWM. In exchange, bipolar PWM tends to yield more stable CMV behavior, whereas unipolar PWM results in variable CMV due to the use of zero states. The table also highlights common practical trade-offs: bipolar PWM generally incurs higher switching losses but is simpler to implement, while unipolar PWM tends to reduce switching losses at the cost of moderate additional implementation complexity. Research by multiple groups has validated these trends through both simulation and experimental results [46], [47].

4.2 Modified Modulation for H5/H6

H5 and H6 topologies benefit from hybrid modulation approaches that combine two key advantages [48]: (1) unipolar DMV characteristics, which help achieve low total harmonic distortion (THD), and (2) constant common-mode voltage (CMV) characteristics, which help reduce leakage current. For a novel H6 modulation approach, reported results show a no-filter THD of 37.5%, compared with 98.7% for bipolar modulation and 53.8% for unipolar modulation [49]. This approach also maintained constant CMV throughout all operating modes, which is significant because CMV variations are a primary driver of leakage-current-related issues.

4.3 Advanced Control Strategies

Recent research has explored advanced control methods including model predictive control (MPC) for CMV suppression [50], phase-locked-loop (PLL)-based grid synchronization under weak grid conditions [51], and reactive power compensation to satisfy grid code compliance requirements [52].

The hybrid modulation for H5/H6 aims to jointly achieve low THD (via unipolar DMV-like behavior) and low leakage current (via constant CMV) [48]. For the H6 case, the key quantitative comparison is THD without a filter: 37.5% for the novel method versus 98.7% (bipolar) and 53.8% (unipolar) [49], alongside the qualitative outcome of constant CMV across operating modes. In control, the emphasis is on mitigating CMV (MPC) [50], maintaining synchronization robustness in weak grids (PLL-based methods) [51], and meeting grid-code reactive power requirements [52]. Overall, the modulation results directly quantify waveform quality

improvements (THD), while the control strategies target system-level compliance and stability concerns that may not show up in THD alone.

V. Wide-Bandgap Semiconductor Integration

5.1 Technology Overview

Wide-bandgap (WBG) semiconductors, particularly Silicon Carbide (SiC) and Gallium Nitride (GaN), offer significant advantages over traditional silicon devices in inverter applications [53]. Compared with silicon IGBTs, SiC MOSFETs and GaN HEMTs have much wider bandgaps (Si: 1.1 eV, SiC: 3.3 eV, GaN: 3.4 eV), which generally supports higher-temperature operation and faster switching. In practical terms, Si IGBTs tend to have medium switching speed and higher on-resistance, SiC MOSFETs achieve high switching speed with lower on-resistance and are commonly favored for high-power use, while GaN HEMTs typically enable very high switching speed and very low on-resistance and are often best suited for low-to-mid power ranges.

Table 7: Material comparison for inverter switching devices

Parameter	Si IGBT	SiC MOSFET	GaN HEMT
Bandgap (eV)	1.1	3.3	3.4
Max Temperature	Medium	High	Very High
On-Resistance	150°C	200°C	200°C
Switching Speed	Higher	Lower	Lowest
Best Application	Any power	High-power	Low-mid power

This table highlights the main trade-offs designers consider: moving from Si IGBT to SiC or GaN improves switching speed and reduces on-resistance, which can cut switching and conduction losses. The “best application” row is a useful rule of thumb rather than a hard boundary—GaN can appear in higher-power designs and SiC can appear in lower-power ones depending on voltage class, packaging, cost, and thermal constraints. Also, the listed maximum temperatures (150°C for Si IGBT and 200°C for SiC/GaN) reflect typical device capability, but real-world operation is often limited by module/package materials and junction-to-ambient thermal design.

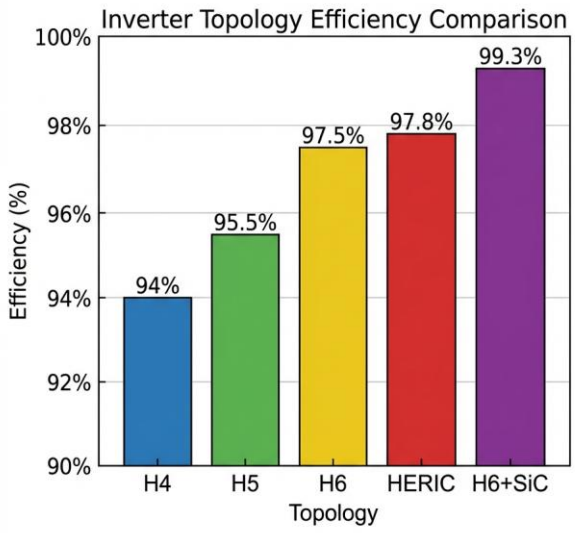
5.2 Efficiency Improvements

Reported peak efficiencies show clear gains when replacing a silicon IGBT baseline (~97%) with WBG devices: SiC MOSFETs reach about 99.3% (an improvement of +2.3%), and GaN HEMTs about 99.18% (an improvement of +2.18%). A noted SiC case at 100 kHz reports about +3% system improvement, described as significant. Research by Barater et al. [54] demonstrated that replacing Si IGBTs with SiC MOSFETs can reduce system losses by half.

Table 8: Efficiency improvements for different configurations

Configuration	Peak Efficiency	Improvement
Si IGBT (baseline)	~97%	-
SiC MOSFET	99.3%	+2.3%
GaN HEMT	99.18%	+2.18%
SiC @ 100 kHz	3% system	Significant

Figure 6: Efficiency comparison of different inverter topologies



5.3 Benefits for H5/H6 Topologies

For H5/H6 inverter topologies, WBG devices enable higher switching frequencies (50–200 kHz), which can reduce the size of passive components [55]. They also reduce conduction losses, improving overall efficiency [56], and offer better thermal performance that can simplify cooling design [57]. Together, these factors increase power density, supporting more compact installations.

VI. Comprehensive Performance Comparison

6.1 Summary

Table 9: Comparative performance of transformerless inverter topologies

Topology	Switches	Efficiency	Leakage Current	THD	Control	Cost
H4 (Bipolar)	4	~94%	High (~800 mA)	Higher	Simple	Lowest
H4 (Unipolar)	4	~95%	Very High	Lower	Simple	Lowest
H5	5	95-96%	Medium (~50 mA)	Low	Medium	Medium
H6	6	~94%	Low (~42 mA)	Low	Med-High	Medium
HERIC	6	97-98%	Very Low	Low	Medium	Higher
H6 + SiC	6	~99%	Low	Very Low	Med-High	Highest

The above table compares commonly used transformerless inverter topologies in terms of efficiency, leakage current, total harmonic distortion (THD), control complexity, and cost. H4 topologies use the fewest switches and therefore have the lowest cost and simplest control, but they suffer from high or very high leakage current, which can limit their use in applications with strict safety standards. H5 and H6 topologies introduce additional switches to better control common-mode voltage, significantly reducing leakage current while improving efficiency. HERIC achieves very low leakage current and high efficiency, but at the expense of higher cost and increased circuit complexity. The H6 topology combined with SiC devices delivers the highest efficiency and lowest THD among the listed options, but it also represents the highest cost due to device price and more demanding control and thermal design requirements.

6.2 Guideline for Selection

For cost-sensitive applications, H5 offers a strong balance between efficiency, leakage current reduction, and moderate cost. When maximum efficiency is the primary objective, H6 combined with SiC or GaN devices is the most suitable choice. Applications with strict leakage current requirements benefit most from H6 or HERIC topologies. For very simple implementations where leakage current limits are relaxed or can be managed, H4 with bipolar modulation remains an option.

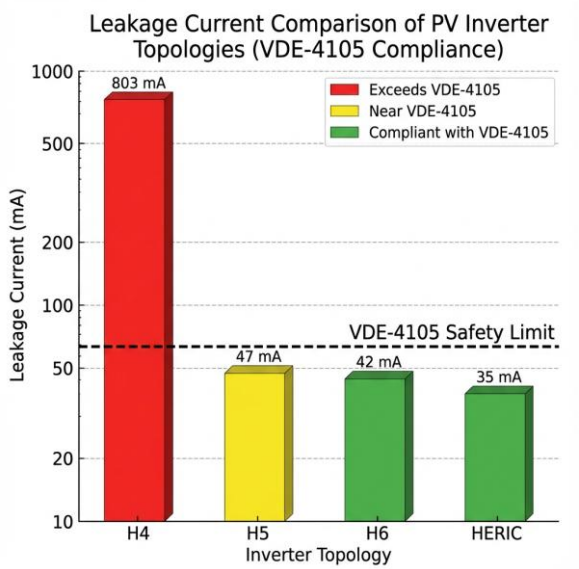


Figure 7: Leakage current comparison of PV inverter topologies according to VDE-4105 compliance.

VII. Research Gaps and Future Directions

Several research gaps remain in the current literature. First, there is a lack of standardized benchmarking, as studies often use different testing conditions, parasitic capacitance assumptions, and grid or load scenarios, making direct comparison difficult [58]. Second, although wide-bandgap devices show strong promise, there is limited experimental data specifically addressing H5 and H6

topologies using SiC or GaN devices, especially with respect to detailed thermal behavior under real operating conditions [59]. Third, most existing work emphasizes steady-state performance, while dynamic behavior—such as transient response during grid faults or the impact of partial shading on common-mode voltage—remains insufficiently studied [60]. Finally, comprehensive cost–performance analyses that include manufacturing complexity and long-term reliability are still largely missing.

VIII. Conclusion

This paper reviewed H4, H5, and H6 transformerless inverter topologies for grid-connected PV systems and found that H4 is simplest and lowest cost but tends to produce high leakage current (about 800 mA) unless heavily modified; H5 offers a proven, practical compromise by cutting leakage to about 50 mA, though three devices conducting increases conduction loss and typically caps efficiency around 95–96%; and H6 generally delivers better overall performance, with leakage around 42 mA and 97–98% efficiency, helped by added switching flexibility to optimize current paths. Wide-bandgap devices (SiC, GaN) can further raise efficiency to 99%+ and support higher switching frequencies for more compact designs. Compliance with safety standards (VDE 0126-1-1, IEEE 1547) remains essential, and H6/HERIC topologies are often better positioned to meet stringent leakage limits (below 30 mA). Future work should prioritize WBG integration, AI-driven optimization, and standardized benchmarking for fair topology comparisons.

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