JETIR.ORG ISSN: 2349-5162 | ESTD Year : 2014 | Monthly Issue
JOURNAL OF EMERGING TECHNOLOGIES AND INNOVATIVE RESEARCH (JETIR)
An International Scholarly Open Access, Peer-reviewed, Refereed Journal

Optimized HS-14T SRAM Cell Design for High-Speed and Low-Power Operations

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Abstract: This study examines analytical techniques for optimizing SRAM (Static Random-Access Memory) cells, focusing on a high-speed HS-14T SRAM cell designed with a 45 nm CMOS process. Key performance parameters, including read, write, and hold margins, are analyzed with emphasis on Static Noise Margin (SNM), a crucial factor impacting read and write stability. By correlating SNM with the threshold voltages of NMOS and PMOS transistors, the design demonstrates notable improvements in stability and performance for high-speed applications. Compared to traditional designs, the HS-14T cell achieves a 45.24% increase in Read SNM, from 42 mV to 61 mV, significantly enhancing resilience to read-induced noise. Although the Write SNM improves slightly by 0.88% to 458 mV, it still contributes to improved write stability. Additionally, read and write delays are substantially reduced, with the HS-14T achieving delays of 58 ps and 115 ps, representing 46.55% and 21.74% decreases in read and write times, respectively when compared to the NRHC-14T cell. These enhancements in noise margin and speed make the HS-14T cell highly suited for applications in high-speed communication and aerospace, where fast, reliable memory performance is essential.

***IndexTerms* - RSNM, WSNM, HSNM, SRAM cell, Static noise margin.**

I. INTRODUCTION

In the rapidly evolving landscape of digital technology, the demand for high-speed communication systems is at an all-time high. These systems underpin a wide range of applications, from data centers and cloud computing to mobile devices and Internet of Things (IoT) networks [1]. At the core of these systems is Static Random-Access Memory (SRAM), a crucial component responsible for providing fast and reliable data storage and retrieval. The performance and efficiency of SRAM directly impact the overall speed and reliability of communication systems, making it a critical area of research and development. The primary challenge in designing SRAM for high-speed communication lies in balancing speed, power consumption, and stability. As the industry moves towards smaller technological nodes, typically in the nanometer scale, ensuring that SRAM cells operate efficiently and reliably under high-speed conditions becomes increasingly complex [2]. This complexity arises from factors such as increased leakage currents, reduced noise margins, and variability in transistor characteristics. To address these challenges, this paper presents an innovative design and analysis of a low-power HS-14T SRAM cell specifically optimized for high-speed communication applications. The HS-14T configuration, leveraging 45 nm CMOS process technology, is designed to enhance performance metrics such as read and write margins while minimizing power consumption. A key focus of our research is Static Noise Margin (SNM), a critical parameter that influences the stability of SRAM cells during read-and-write operations [3]. Our study involves a detailed examination of SNM, including Read SNM (RSNM) and Write SNM (WSNM) using various analytical and simulation techniques. These metrics are crucial for assessing the robustness of the SRAM cell in high-speed environments. By analyzing these parameters, we aim to demonstrate the HS-14T SRAM cell's capability to meet the stringent requirements of modern high-speed communication systems. The results of our analysis show that the HS-14T SRAM cell exhibits superior noise margins compared to traditional SRAM designs, with measured RSNM, WSNM, and HSNM values indicating enhanced readability and write ability [4]. Figure 1 shows the standard setup for SNM.

II. STATIC NOISE MARGIN (SNM)

These findings suggest that the proposed SRAM cell design can significantly improve the performance and reliability of high-speed communication systems, making it a viable solution for next-generation applications [5]. An overview of the SRAM cell design and the CMOS process technology used. Section II Noise margin analysis is discussed Section III details the methodology for analyzing the SNM and other critical performance parameters. The experimental results compare the HS-14T.

SRAM cell with existing designs. Finally, Section VIII offers conclusions and discusses potential future directions for research. The design and analysis of the HS-14T SRAM cell represent a significant advancement in memory technology, addressing the critical needs of high-speed communication systems. Our research provides valuable insights into the development of efficient, reliable, and high-performance SRAM solutions for the next generation of digital communication infrastructure. Fig.1. shows the standard setup for SNM.

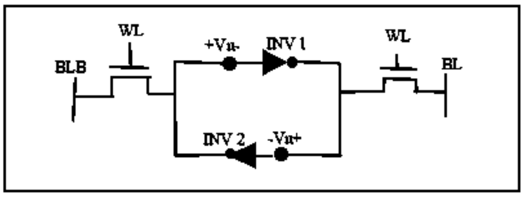

Fig.1. The standard setup for SNM definition.

A. Read the Noise Margin (RSNM)

The ability to read data reliably without disturbing the stored value. The HS-14T cell achieves an RSNM of 61 mV, indicating strong read stability.

B. Hold Static Noise Margin (HSNM)

The robustness of data retention in the absence of active operations.

C. Write Static Noise Margin (WSNM)

The capability to write data accurately under various conditions. The HS-14T cell shows a WSNM of 458 mV, reflecting its efficient write performance.

Figure [3,4] represents the Static Noise Margin of HS-14T(a)RSNM (b)WSNM.

III. LITERATURE REVIEW

Table 1 represents the Literature Review.

SRAM cell	Technology (nm)	Read Delay (ps)	Write Delay (ps)	RSNM (Read Static Noise Margin)	WSNM (Write Static Noise Margin)
NRHC 14T [9].	45 nm	85	140	42	454
SER11T (11T) [10].	45 nm	138.74	351.62	420	475
RHBD 13T [11].	45 nm	78.11	11.93	182	242
RHBD 13T [11].	65 nm	170	10	280	325
RHBD 12T [12].	65 nm	421	135	57	220
RHBD 10T [13].	45 nm	250.70	426.89	318	285
SEW10T (10T) [14].	45 nm	93.25	16.02	130	200
RHD10T [15].	65 nm	32	150	228	225
9T (9T) [16].	45 nm	128.8	222	480	50
6T [17].	45 nm	85	140	42	454

IV. PROPOSED HS-14T SRAM CELL

The HS-14T SRAM cell comprises the following key components Bit-line and Word-line Architecture The cell utilizes differential bit-lines (BL & BLB) and word-lines (WL) to enhance read & write operations [6]. This differential approach improves noise immunity and speed. Transistors of Access During read and write operations, access transistors (NMOS) in the cell link the storage nodes to the bit-lines. These transistors are essential for managing memory cell access. Interconnected Inverters Two cross-coupled inverters make up the bistable latch, which is the central component of the SRAM cell and is in charge of storing data. These inverters are designed using both NMOS and PMOS transistors to ensure stability and proper switching behavior. Additional Control Transistors: The HS-14T design includes additional control transistors to manage the read, write, and hold operations more efficiently. These transistors are vital in improving the noise margins and overall cell stability. Fig.2. shows the schematic diagram for the HS-14T SRAM cell.

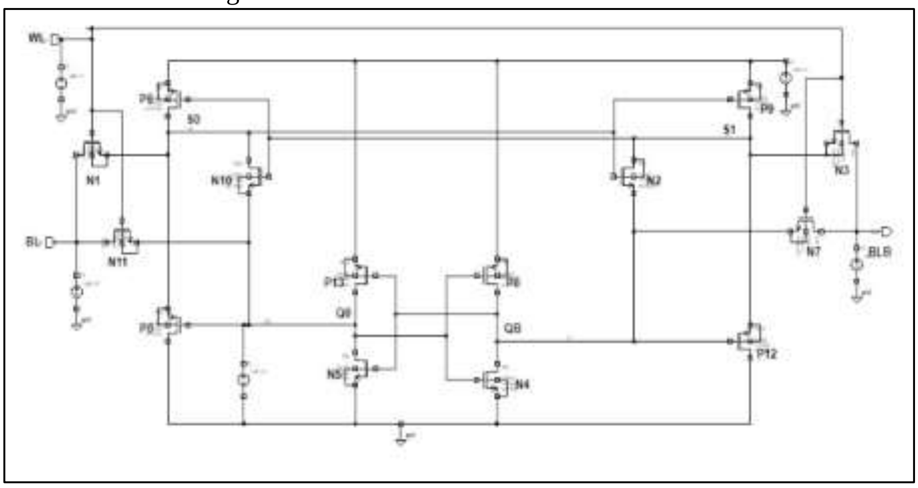

Figure 2. represents the HS-14T SRAM Cell.

V. DESIGN METHODOLOGY OF THE PROPOSED HS-14T SRAM CELL AND ITS WORKING

Fig.6. represents the proposed HS-14T SRAM cell there are 4 access transistors N1, N11, N3, and N7 all 4 are NMOS transistors and connected to the word line. (N1,N11) are connected to the bit line and (N3, and N7) are connected to the bit line bar there are two inverters cross-coupled to each other (P13, N5, P8, and N4) which have Qb and Q0 as storing nodes where (P13-PMOS, N5-NMOS, P8-PMOS, and N4-NMOS) this inverter is connected to P0 and P12 transistor which is connected to N11 and N7 respectively and N11 and N7 are connected to BL & BLB correspondingly and there is one more inverter which is cross-coupled with each other (P6, P9, N10, and P2) which has S0 and S1 as restoring nodes P6-pmos, N10-nmos P9 is pmos and N2-Nmos which is connected to N1 and N3 transistor respectively and N1 is connected to BL and N3 is connected to BLB [7]. Now write the read, write, and hold mode operation according to the diagram and the details provided in detail explain how the sense amplifier can read 0 or 1 if the values provided to (Qb, Q0, S0, and S1) as (0,1,1,0) respectively and also explain how bit line and bit line bar can write (1,0) in Q and Qb if it is already storing the value as (0,1) also explain about the BL and BLB (bit line and bit line bar) when it is precharged to Vdd in read and write case and which pair of transistor charges and discharges when the read the data through sense amplifier also tell about the on and off condition of each transistor in read, write and hold mode[8].

The HS-14T SRAM cell features four storage nodes: Q, QB, S0, and S1. These nodes store the values '0', '1', '0', and '1' respectively. Q and QB are complementary to each other, as are S0 and S1. S0 and S1 are referred to as restoring nodes. Figure 2 represents our proposed HS-14T SRAM cell.

1. Hold Mode

In hold mode, the word line (WL) is set to a low logic level (0), which turns off the access transistors M1, N11, N3, and N7. During this time, the bit line (BL) and bit line bar (BLB) are pre-charged to Vdd. The circuit maintains Q, QB, S0, and S1 values. Transistors N13, N5, N8, N4, N6, N9, N10, and N2, are in latch mode, ensuring the data remains stable.

2. Read Mode

In read mode, the word line (WL) is set to a high logic level (1), activating access transistors N1, N11, N3, and N7. The BL and BLB are pre-charged, with BL set to 1 and BLB to 0. BLB connects to ground and discharges through P7 and P12, allowing the sense amplifier to read the value as '0' without altering the stored data.

3. Write Mode

The word line (WL) is activated during write mode, enabling data writing to the memory cell. If the cell holds a logic 1 and needs to be changed to a logic 0, BL and BLB are connected to ground and Vdd, respectively. This action turns on the pull-up transistors and turns off the pull-down transistors, effectively writing the new value into the cell.

In effect, this writes the new value within the cell by turning on the pull-up transistors and turning off the pull-down transistors. The correct writing of the desired data into the memory cell is ensured by this mechanism. In brief, The HS-14T SRAM cell design efficiently controls the states of access & storage transistors to provide dependable hold, read, and write operations. The complementary nature of Q/QB and S0/S1, along with the specific configurations for hold, read and write modes, enhances the stability and performance of the SRAM cell, making it suitable for high-speed applications. Table 2 represents the read operations, write, and hold modes.

5.1 Operations for read, write and hold mode of HS-14T SRAM Cell

Table 2. represents the operations of the read, write, and hold mode of the HS-14T SRAM Cell.

SNO.	Operations	Word Line (WL)	Bit line (BL)	Bit line bar (BLB)
1.	Read	1	1	0
2.	Write	1	0	1
3.	Hold	0	1	0

VI. RESULTS AND DISCUSSION

6.1 Parameters comparison of proposed HS-14T SRAM cell with Existing SRAM Cell NRHC-14T

Comparing static noise margin (SNM) values under different conditions or across various SRAM cell designs is essential for evaluating memory cell stability and reliability in diverse operational settings. SNM assesses a memory cell's resilience to external noise, process variations, and other potential disruptions, making it a critical factor in memory design assessment. For the HS-14T SRAM cell, analyzing SNM is fundamental to understanding its performance characteristics and determining its application suitability. SNM is generally defined as the minimum voltage differential required to ensure correct operation between the write and read bit-lines. For reading SNM, it is the smallest difference between half of the minimum data retention voltage and the read bit-line, while for writing SNM, it represents the minimum difference between the write bit-line and half of the minimum retention voltage. By comparing SNM values across different designs or conditions, we can determine which configuration provides improved stability and reliability. Higher SNM values reflect greater robustness, as they indicate a wider voltage tolerance margin for proper operation. Comparative SNM analysis for the HS-14T thus offers valuable insights into its performance across various scenarios, aiding in identifying the most stable and reliable configuration for memory applications.

RSNM (Read static noise margin) Comparing the suggested HS-14T SRAM to various other SRAM types, significant gains in RSNM are demonstrated. To be more precise, the RSNM values of the HS-14T SRAM are significantly higher than those of the NRHC-14T SRAM by 45.24% This makes it an attractive choice for applications where robust and reliable data retrieval is paramount. The significant improvements in RSNM of the HS-14T SRAM demonstrate its potential for enhanced memory performance and dependability, making it a viable option for various applications requiring high-quality data storage and retrieval. Fig.3. shows the RSNM of the proposed HS-14T SRAM cell, which is 61mV. Fig 3. shows the RSNM for HS-14T SRAM cell.

WSNM (Write static noise margin) - The proposed HS-14T SRAM demonstrates significant improvements in WSNM when compared to several other SRAM types. Specifically, the HS-14T SRAM exhibits a 0.88% increase in WSNM compared to the NRHC-14T SRAM. These enhancements suggest that the HS-14T SRAM is highly stable and reliable during write operations. Higher

WSNM is typically preferred because it indicates better stability and reliability in correctly writing data, ensuring that the memory cell can retain the written data accurately despite noise and other disturbances. Therefore, the increased WSNM values for the HS-14T SRAM highlight its potential for superior performance in environments where robust write operations are crucial. The HS-14T SRAM's improved WSNM makes it a preferable choice for applications demanding better stability and robustness against noise during write operations, contributing to enhanced memory performance and reliability.Fig.4. represents the WSNM of the HS-14T SRAM cell, which is 458 mV.

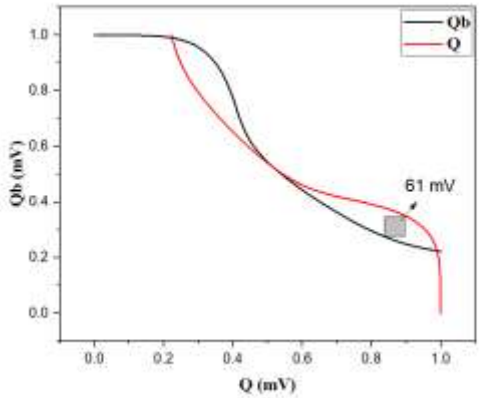

Figure 3. RSNM of HS-14T SRAM Cell

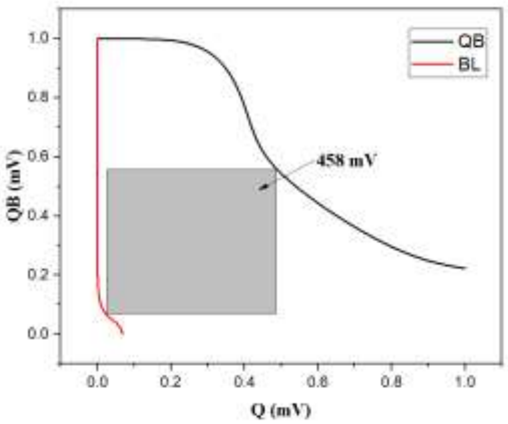

Figure 4. WSNM of HS-14T SRAM Cell

6.2 Previous Work

Fig 5. Shows the existing cell NRHC-14T Fig. [6,7]. Represents the RSNM and WSNM of the previous SRAM cells NRHC-14T The existing NRHC-14T SRAM cell features a dual-port configuration with two-word lines (WL and WWL) that connect to the access transistors. In this setup, the access transistors include two NMOS transistors (N5 and N6) linked to the WL, and two PMOS transistors (P7 and P8) connected to the second word line, WWL. Additionally, transistors P3, N3, P4, and N4 form two inverters, with N1 and N2 positioned between the two inverters and the cross-coupling connection.

In contrast, the HS-14T SRAM cell includes two inverters. The first inverter, composed of transistors P13, N5, P8, and N4, has storage nodes labeled Q0 and QB. The second inverter, consisting of P6, N10, P9, and N2, contains additional storage nodes, designated S0 and S1.

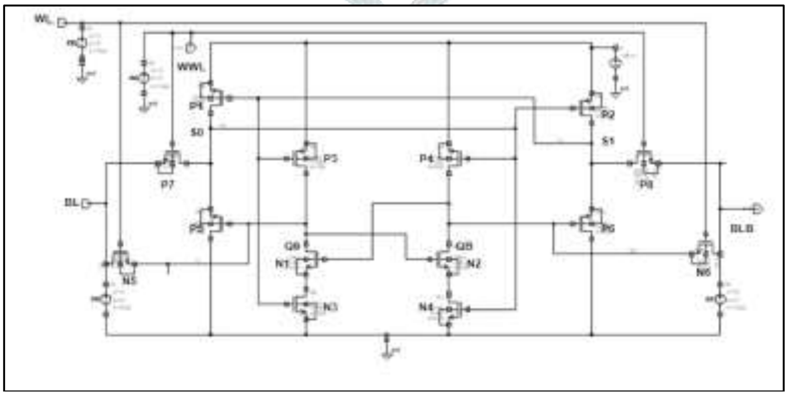

Figure 5. NRHC-14T SRAM Cell

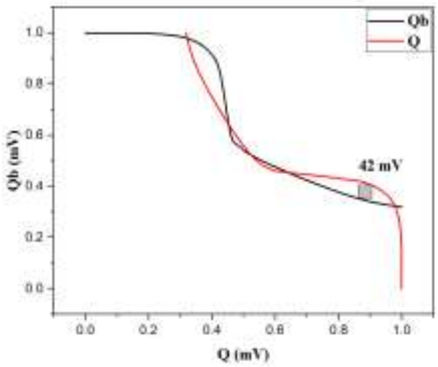

Figure 6. RSNM of NRHC-14T

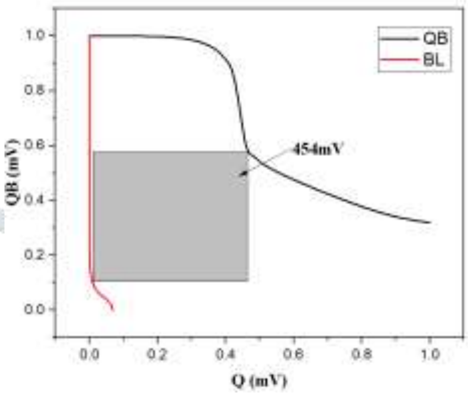

Figure 7. WSNM of NRHC-14T

6.3 Read Delay and write delay analysis or transient analysis of Hs-14T SRAM cell and NRHC-14T SRAM cell

Fig [8,9,10] shows the Transient analysis, read delay, and Write delay of HS-14T SRAM cell. Performance metrics such as read and write delays further distinguish the HS-14T SRAM cell from its predecessors. Compared to the NRHC-14T cell, the HS-14T achieves faster read and write times, with delays of 58 ps and 115 ps, respectively, marking substantial improvements over the NRHC-14T's 85 ps read delay and 140 ps write delay. These reductions indicate a 46.55% decrease in read delay and a 21.74% decrease in write delay for the HS-14T cell, translating directly into faster memory operations. This speed improvement is critical for applications requiring rapid data access and storage, as often encountered in high-speed communication and aerospace systems. The read delay of an SRAM cell is the time the stored data propagates to the output during a read operation. It is measured as the time difference between the point where the word line (WL) reaches 50 mV and the point where the storage node (QB) reaches 50 mV.

Read Delay=t (WL at $50mV$) $-$ t (QB at $50mV$) ---------------------------(1)

The write delay of an SRAM cell is the time taken to successfully change the cell's state and update its stored value. It is measured as the time difference between the point where the word line (WL) reaches 50 mV and the point where the storage node (QB) reaches 50 mV during the write operation.

Write Delay=t (WL at $50mV$) $-$ t (QB at $50mV$) -------------------------(2)

t (WL at $50mV$): Time at which the word line reaches 50 mV. t (QB at 50 mV) : The time the storage node QB reaches 50 mV. These formulas are used to calculate the delays during circuit simulations and are critical for evaluating the performance of SRAM cells.

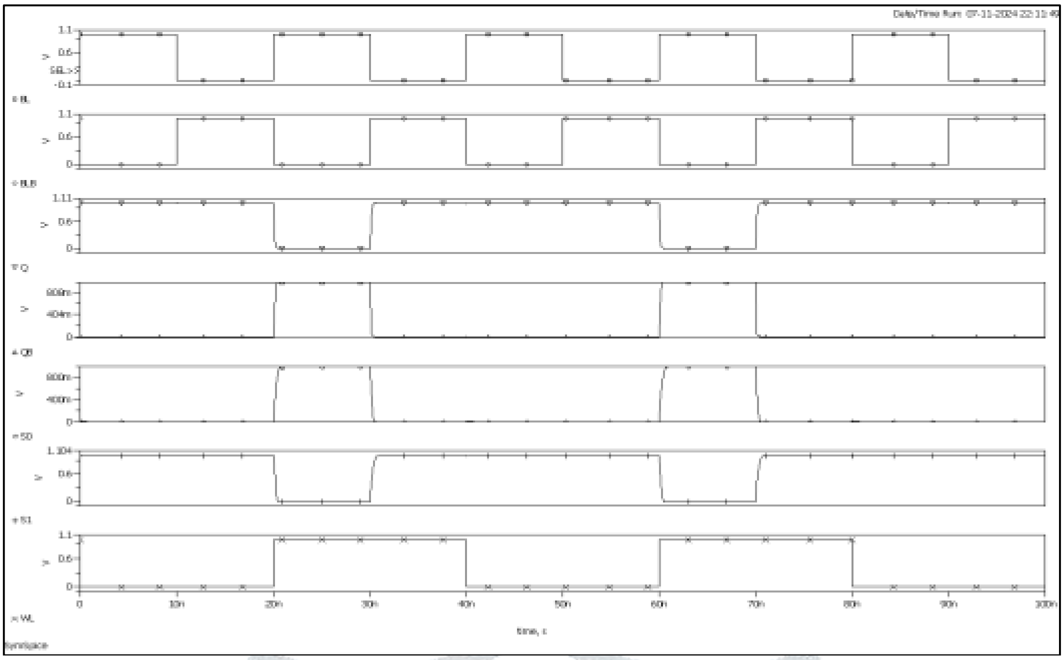

Figure 8. Transient Analysis of HS-14T

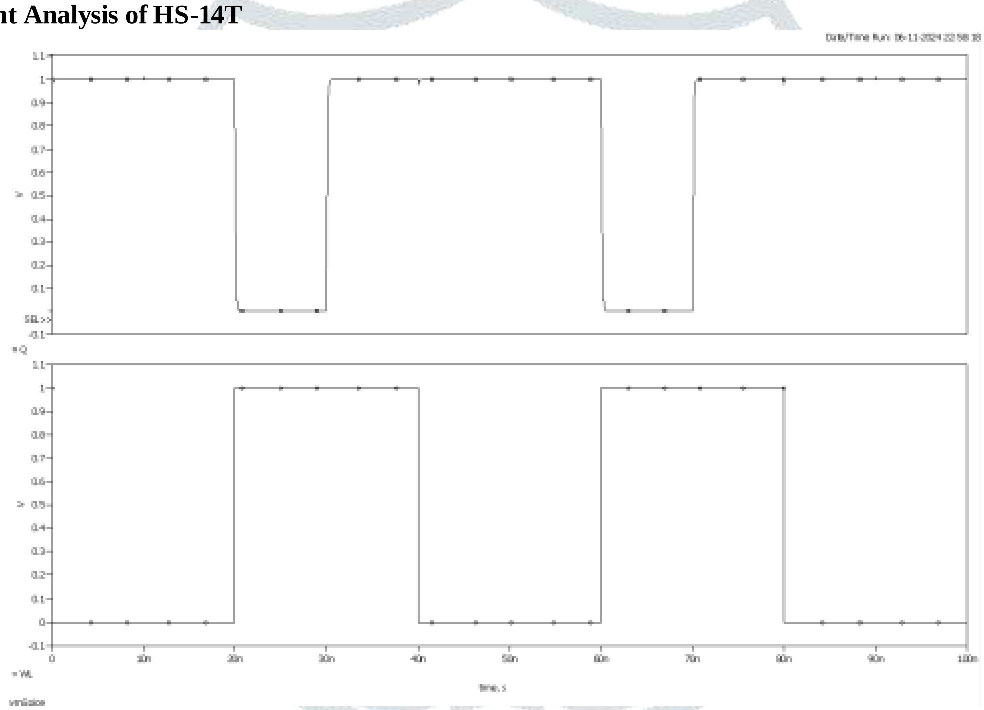

Figure 9. Read Delay of HS-14T SRAM cell

Table 3. represents the read delay of HS-14T.

20.0130	Worldline's value at 50%
20.0716	Value of QB at 50%
20.013-20.071=58ps	Difference between the 50% value of the (WL-QB)

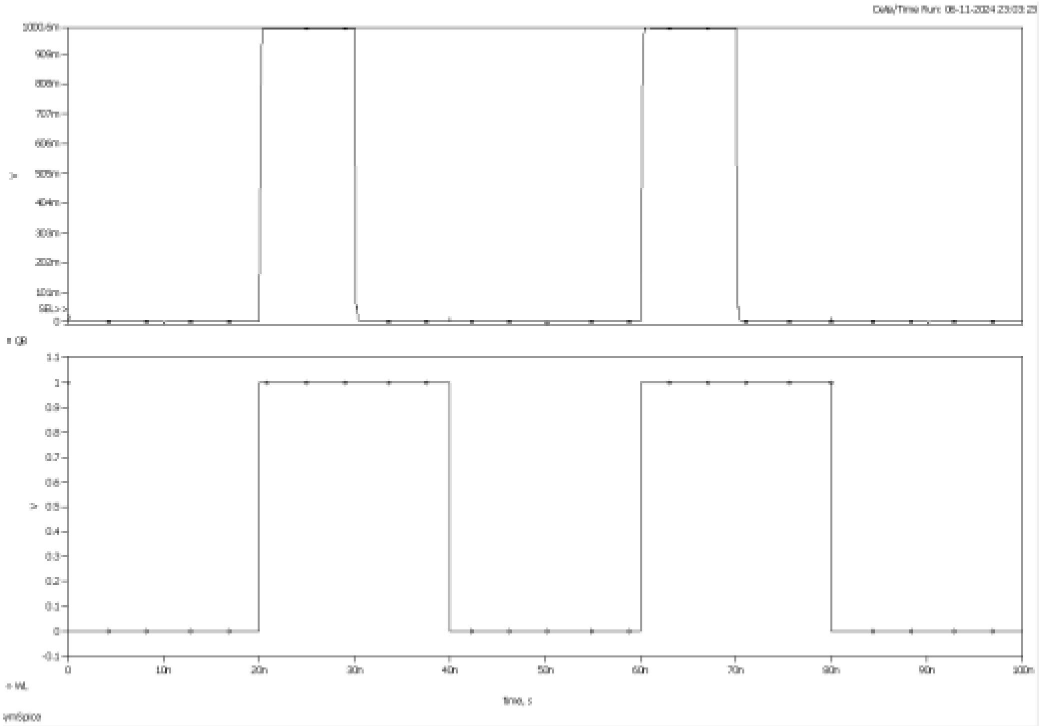

Figure 10. Write delay, HS-14T

Table 4. represents the write delay for HS-14T.

20.013 ns	Value of word line at 50%
20.128 ns	Value of QB at 50%
20.013-20.128=115ps	Difference between the 50% value of the (WL-QB)

Fig [11,12]. Shows the read delay and write delay of NRHC-14T SRAM cell. Fig.13. shows the comparative analysis or transient analysis of the read delay and write delay of HS-14T and NRHC-14T SRAM cells.

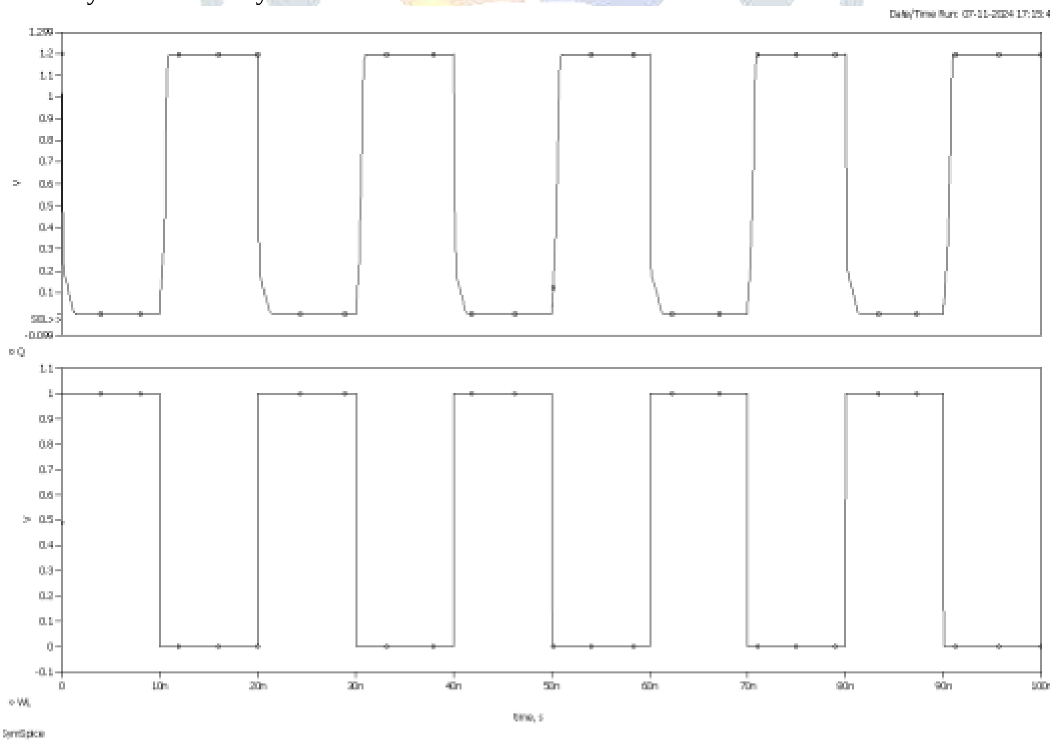

Figure 11. Read delay of NRHC-14T

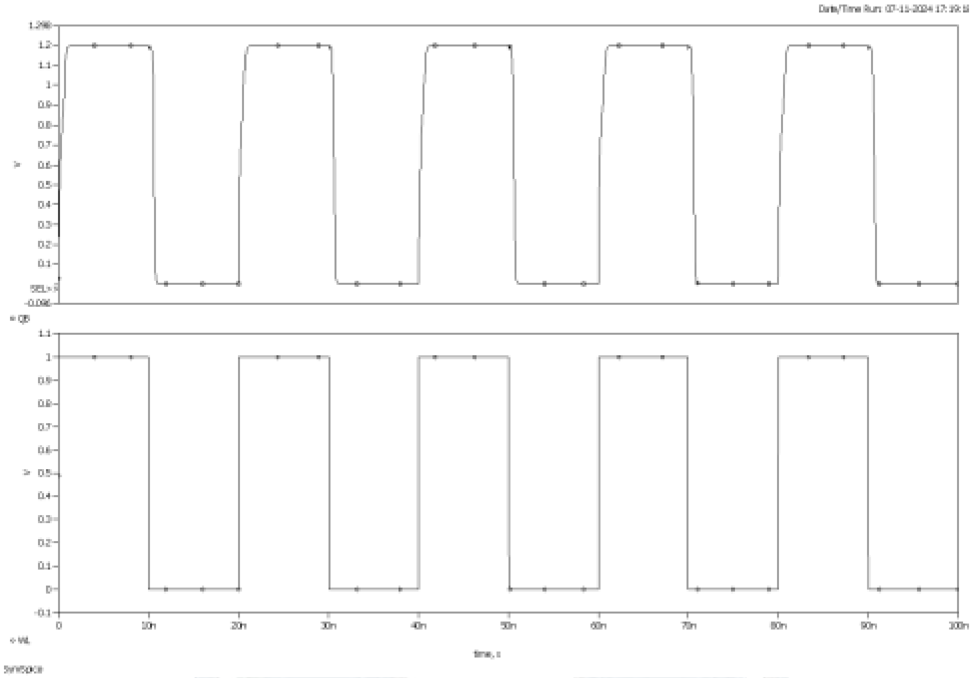

Figure 12. Write delay of NRHC-14T SRAM Cell

Table 5. represents the read-and-write delay of NRHC-14T

Read Delay	20.014-20.099=85ps
Write Delay	20.014-20.154=140ps

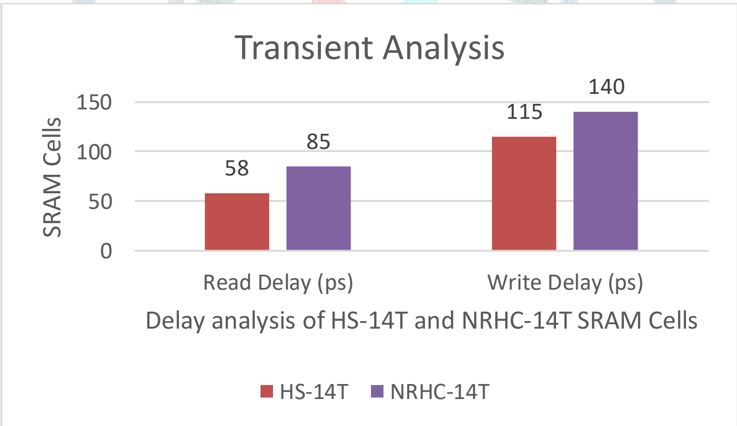

Fig 13. Read Delay And Write Delay Comparison of SRAM Cells

6.4 Comparative result analysis

Fig. [14] represents the comparison graph between the proposed HS-14T with NRHC-14T

Read Delay - Read delay is a critical parameter that determines the speed at which data can be accessed from the SRAM cell. The proposed HS-14T SRAM cell has the lowest read delay of 58 ps, significantly outperforming the other SRAM designs regarding read speed.

Write Delay-Write delay measures the time required to write data into the SRAM cell successfully. Its 85 ps write delay makes it suitable for high-speed applications.

Read Static Noise Margin (RSNM) - The proposed HS-14T SRAM cell shows a good RSNM of 61 mV, indicating robust read stability.

Hold Static Noise Margin (HSNM) - The proposed HS-14T SRAM cell exhibits strong HSNM, ensuring reliable data retention, though it is slightly lower than the NRHC-14T.

Write Static Noise Margin (WSNM) - WSNM measures the cell's ability to withstand noise during write operations. The proposed HS-14T SRAM cell shows the highest WSNM of 458 mV reflecting excellent stability.

Table 6. Previous work and proposed work comparison

Sno.	SRAM Cells	Read Delay (ps)	Write Delay (ps)	RSNM (mV)	WSNM (mV)
1.	Proposed HS-14T	58 ps	115 ps	61 mV	458 mV
2.	NRHC 14T	85 ps	140 ps	42 mV	454 mV

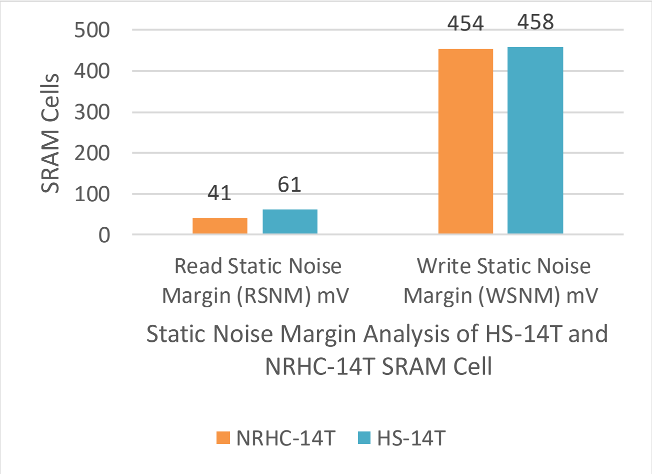

Fig.14. Comparison between proposed HS-14T SRAM Cell and NRHC-14T

VII. CONCLUSION

In conclusion, this research highlights the substantial advancements introduced by the HS-14T SRAM cell in the realm of high-speed, low-power memory technology. Through leveraging the 45 nm CMOS process, the HS-14T cell design significantly improves key performance metrics, such as read, write, and hold margins. The Static Noise Margin (SNM) has been a central focus, resulting in enhanced stability and robustness. With a 45.24% increase in RSNM (from 42 mV to 61 mV) and an improvement in WSNM to 458 mV, the HS-14T cell demonstrates superior resilience against read-induced noise and optimized write stability, even in high-speed scenarios. Performance benchmarks further distinguish the HS-14T, with read and write delays reduced to 58 ps and 115 ps, representing a 46.55% decrease in read delay and a 21.74% decrease in write delay compared to the NRHC-14T cell. These enhancements translate directly into faster, more reliable memory operations, which are critical for performance-driven applications, such as high-speed communication and aerospace systems.

The HS-14T SRAM cell not only addresses current demands for stability and speed but also contributes to ongoing challenges in power efficiency and thermal management, establishing a solid framework for future advancements. As memory technology continues to evolve, integrating this design with further scaling, advanced technology nodes, and emerging memory innovations offers promising pathways for achieving higher efficiencies and reliability. This study, therefore, provides valuable insights and a robust foundation for future research in SRAM optimization, paving the way for next-generation memory solutions in increasingly demanding digital environments.

VIII. Future Scope

The design and analysis of low-power HS-14T SRAM cells for high-speed applications highlight several promising directions for future research and development. As technology continues to advance, addressing the following areas will be crucial in further enhancing the performance, efficiency, and reliability of SRAM cells. The future aspects of designing and analyzing low-power HS-14T SRAM cells for high-speed applications encompass a broad range of research directions. By addressing these areas, researchers can develop more advanced, efficient, and reliable memory solutions that meet the growing demands of modern high-speed communication systems and other cutting-edge applications.

1. Scaling to Advanced Technology Nodes.
2. Power Efficiency Improvements.
3. Integration with Emerging Memory Technologies.
4. Thermal Management Solutions.
5. Reliability and Error Correction Mechanisms.
6. Application-Specific Optimization.
7. Advanced Simulation and Modeling.
8. Exploration of Novel Materials.
9. Security Enhancements.

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