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DESIGN AND DEVELOPMENT OF HIGHWAY ADDRESSABLE REMOTE TRANSDUCER (HART) CONVERTER

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Abstract : The HART (highway addressable remote transducer) protocol is extensively employed in industrial applications due to its ability to transmit both digital and analog data over a single communication bus. It is used for monitoring of different types of input such as pressure, flow, level. It gives simultaneous 2 channels for communication one is analog process value in the form of 4mA to 20mA and another is digital FSK modulated signal which contain all sensor process value, configuration details and diagnostic data. FSK modulated signal uses very low Frequency of 1200 Hz and 2400 Hz with small AC amplitude so it cannot interference with DC current signal. While designing of HART converter required hardware components such as a microcontroller, communication IC, power supply, Isolation transformer unit etc. With dedicated peripheral interfaces for HART communication. HART protocol is implemented in microcontroller which can able to transmit and receive HART Frame, after receiving HART Frame this converted in to readable values by applying in IEEE 754 float format conversion. The converter implements handling of point to point and multi-drop configurations. As HART is master slave architecture which support 2 Master on same bus with maximum 15 slave, to synchronise this we need to implement different timers such as response timer, turnaround delay timer, response time limit timer, and token-passing timer for smooth and healthy communication of HART between slave and both master. [1]

Index Terms **- HART protocol, Microcontroller, Serial Communication, FSK Modulation, Analog output.**

1. INTRODUCTION

The HART converter is essential for industrial automation for monitoring of parameters which enabling communication between legacy HART devices and newer control systems. It provides cost-effective upgrades, enhances data access and diagnostic capabilities, improves interoperability, and supports real-time monitoring. It also plays a vital role in bridging the gap between traditional industrial systems and emerging industry 4.0 technologies, ensuring flexibility and scalability in industrial automation environments. The large number of process automation equipment use's a milliampere (mA) analog signal for remote communication because 4-20 mA is reliable, low cost, and standard communication but it can transmit only single process value. In industry other parameter also required from sensor/transmitter or controller for monitoring, diagnosis or controlling which is not possible on single 4-20 ma output. To overcome this HART communication protocol (highway addressable remote transducer) is used. [1][3]

The HART protocol was developed in the mid-1980s by Rosemount inc. HART is a in the OSI model a layer 7, application. Layers 3–6 are not used. When sent over mA it uses a bell 202 for layer 1. As the digital FSK signal is phase continuous, there is no interference with the 4-20ma signal. The digital signal contains information from the device including Process value, device status, diagnostics, and additional measured or calculated values, etc. The two communication channels provide a complete field communications solution that is easy to design, simple to use, low cost and extremely reliable.[4] HART support two operation mode for connection of slave devices one is point to point and another is multi-drop. In point-to-point mode both the 4–20 mA current and the digital signal are available on HART bus while in multidrop mode only digital data can be access on HART bus analog loop current is fixed at 4 mA and it is possible to have more than one instrument on a signal loop.[2]

2. Objective

The purpose of this is to design and development of HART converter using microcontroller which can enable seamless communication between field devices such as flowmeter, pressure transmitter, temperature controller etc. In industrial control systems. HART provide efficient and reliable data exchange in process automation applications. This design and implementation aims to provide a comprehensive roadmap to develop a robust HART device ensuring that the system can read process value and diagnostics data from any HART device. Microcontroller with HART modem can used to facilitate bidirectional digital communication over analog 4-20ma current loops.[6] this implementation explores various design methodologies also offering different implementation strategies and testing approaches for system design. HART protocol stack includes error handling, multi drop mode with physical layer, data link layer, and application layer integration. In converter we had implement different timers such

as response timer, turnaround delay timer, response time limit timer, and token-passing timer for smooth and healthy communication of HART between slave and both master.

3. Design

I. Interfacing Of HART Modem IC With Microcontroller

This design contains various hardware components HART modem IC, RS232 communication ports, signal isolation, power supply and an external crystal oscillator. As HART has modulated FSK signal we need to do modulation and demodulation to send and receive digital data, all this can be done using HART modem IC figure 3 shows internal structure of HART modem IC. IC DS8500 is capable for modulation and demodulation of incoming FSK signal but DS8500 does not implement any portion of the HART communication protocol, it only handles the modulation and demodulation of the encoded information. HART protocol we need to implement in microcontroller. For implementation and design we have used Nuvoton M480 microcontroller. [5]

The Nuvoton M480 series microcontroller is embedded with arm® cortex® -M4F core with hardware cryptography which supports DSP (Digital Signal Processer) instruction and an integrated floating-point unit. The M480 series supports Flash size up to 2560 kb and SRAM size up to 160 kb. The operating Frequency is up to 192 MHz with 175/130 µa/ MHz dynamic power consumption and the standby current can be lower to 1 µa. Nuvoton M480 series support built-in Nested vectored interrupt controller (NVIC). The NVIC and the processor core interface are closely coupled to enable low latency interrupt processing and efficient processing of late arriving interrupts. Hardware IEEE 754 compliant floating-point unit (FPU), dsp extension with hardware divider and single-cycle 32-bit hardware multiplier,24-bit system tick timer, serial and USB boot loader, on-chip flash programming with in-chip programming (ICP), in system programming (ISP) and in-application programming (IAP) capabilities, cyclic redundancy calculation (CRC) require for HART CRC calculation, it Support CRC-8, CRC-16 and CRC-32 polynomials. Auto Flow control (RTS and CTS) which is required for HART modem IC, Supports RS-485 9-bit mode and direction control, incoming data, received data FIFO reached the threshold and RS-485 address match and wake-up function in idle mode. Supports hardware or software that enables to programming of RTS pin to control RS-485 transmission direction, supports wake-up function, 8-bit receiver FIFO time-out detection function, supports break error, frame error, parity error and receive/transmit FIFO overflow detection function, PDMA operation [8].

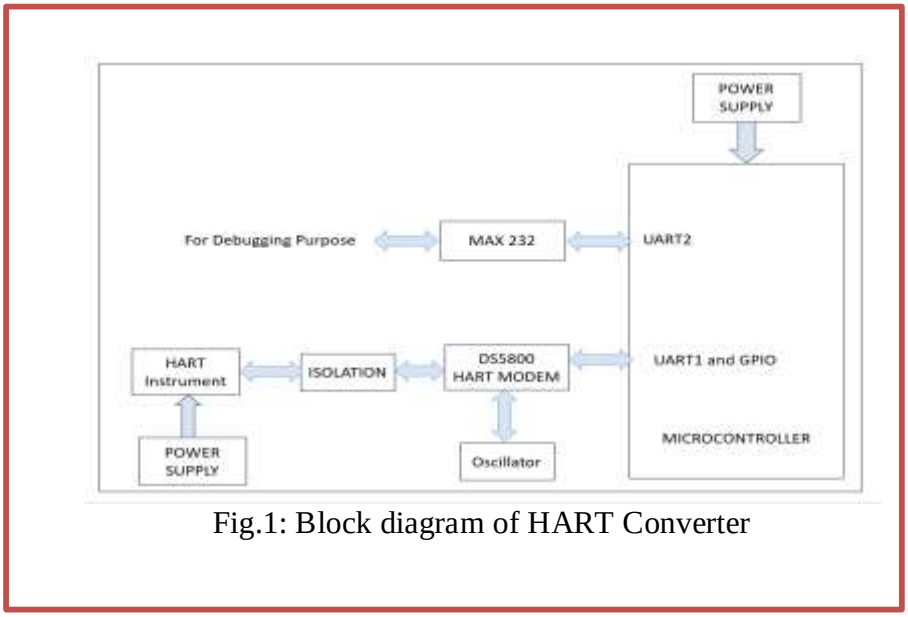

Fig.1: Block diagram of HART Converter

Figure 1 provide details for hardware design for HART converter. The HART instruments may be either single or multiple, powered by the same or different power supplies. Dc 12V/24V power supply is used as input supply further which converted in to 5V and 3.3V. All HART modem IC, microcontroller work on 3.3V while RS232 IC work on 5V power supply. The microcontroller is configured for UART1 (universal asynchronous receiver-transmitter) communication with a HART modem which enable physical layer communication at a baud rate of 1200 with even parity. Additional general-purpose input/output (GPIO) pins are used to interface and send modulation and demodulation commands during signal transmission and reception. Microcontroller UART2 is interfaced with MAX232 IC which is used for debugging and checking communication log on HyperTerminal. To avoid electrical noise and ground loop interference isolation is required in HART bus it allows for multiple devices to operate on the same HART network without mutual interference.[5][8]

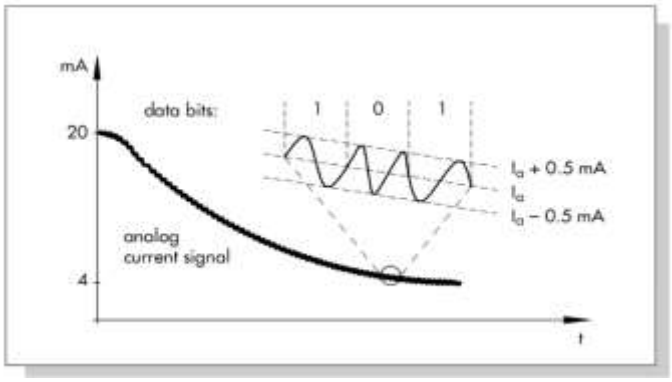

Fig. 2: HART signal superimposed on analog current signal.

Figure 2 illustrates how HART signals are superimposed onto an existing 4-20 ma current signal using frequency-shift keying (FSK) modulation. The bell 202 standard employs FSK to transmit digital data over a voice-grade telephone line. In this standard, two distinct frequencies are used to represent binary 0 and binary 1. Typically, a lower frequency (1200 Hz) corresponds to binary 0, while a higher frequency (2200 Hz) corresponds to binary 1. This modulation technique preserves the integrity of the traditional 4-20 mA analog signal while enabling the simultaneous transmission of digital communication signals over the same wiring. As a result, it allows for bidirectional communication with smart instruments without interfering with the analog 4-20 mA signal.[4]

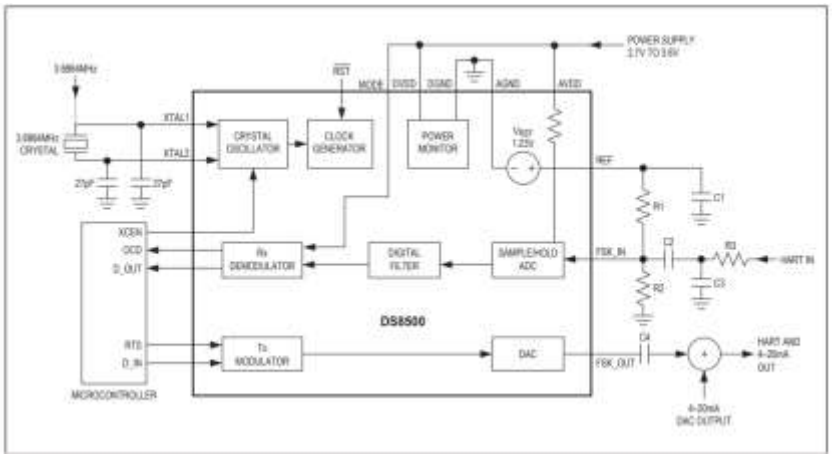

Fig. 3: Typical Microcontroller Interfacing Circuit for DS8500 HART Modem [5].

Figure 3 shows internal structure and Microcontroller interfacing of HART modem IC. OCD and RTS are modulation and demodulation control pins and D_IN and D_OUT are data transmit and receive pins.

Fig. 4: Hardware Design for HART Converter

Figure 4 shows actual designed Hardware for HART Converter with all its component.

II. Implementation of HART protocol

Each HART device has 38-bit address that consist of manufacturer id, device type, device unique identifier. There are two types of frames in the HART protocol short frames and long frames. Short frames are used to retrieve basic device information and connection status while long frames are employed to fetch detailed data from devices. Both frame types must be implemented to get data from HART devices. HART support primary and secondary master on single bus while implementation we need to define device as primary or secondary master. HART supports point to point and multidrop connection, in point-to-point connection analog (4 to 20 mA) and digital data can be accessed with HART id as 0 while in multidrop mode analog value get fixed to 4 mA and digital data can be accessible. In multidrop maximum 15 devices can be connect in a single HART bus.[1]

HART provides numerous commands categorized as universal, common practice, and device-specific commands. Universal commands apply to all devices, common practice commands are used by most devices, and device-specific commands are tailored to particular device families or manufacturers. To obtain minimal data from a HART device commands 0, 1, 2, and 3 are used and this is need to be implemented. Command 0 is used to read basic device information, command 1 reads the primary variable, command 2 retrieves the current output and percentage of range, and command 3 fetches four predefined dynamic variables with current output. The predefined dynamic variables include the process value and percentage of range, executing commands 1 and 2 may not be necessary. Some HART devices support burst communication mode which give fast data update. In burst mode master instruct slave device to continuously broadcast a standard HART reply message, master will receive continues data until it instructs the slae device to stop bursting. Furthermore, it is crucial to implement logic for switching between master and slave functions, an error handling mechanism to prevent false data and precise timers for smooth HART communication such as the response timer, turnaround delay timer, response time limit timer, and token-passing timer.[1]

Table 1&2 shows HART transmit and receive frame structure which consists of a preamble, start delimiter, address byte, command byte, data bytes, and a checksum.

HART transmit frame format

PR	SD	AD	CD	BC	Status	Data	CRC

Table 1. HART transmit frame structure.

PR – Preamble (5 to 20 byte hex FF) used for data synchronisation
SD – Start character
AD – Address (source and destination 1 to 5 bytes)
CD – Command
BC - Byte count of status and data filed.
Status – Command, communication, and device status 2 byte from slave to host only.
Data – 0 to 255 bytes of data
CRC – CRC 8 checksum

HART response frame format

PR	SD	AD	CD	RC	Data	CRC

Table 2. HART response frame structure

PR – Preamble (5 to 20 byte hex FF) used for data synchronisation
SD – Start character
AD – Address (source and destination 1 to 5 bytes)
CD – Command code
RC - Response code.
Data – 0 to 255 bytes of data
CRC – CRC 8 checksum

Above HART frames are implemented in Nuvoton M480 Microcontroller. Microcontroller Support Embedded C Coding which is done by Keil software.

4. Result and conclusion

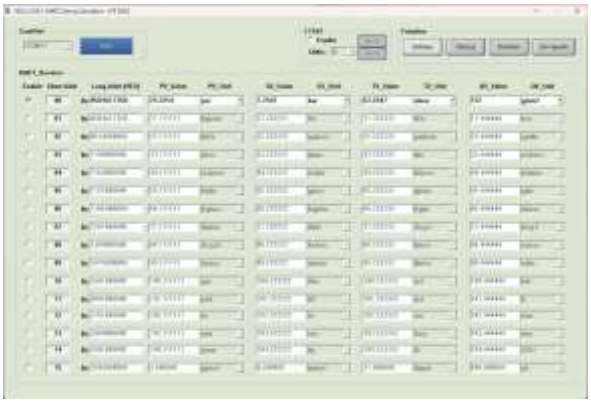

Fig. 5: HDS (HART Device Simulator) Software

Figure 5 shows HDS (HART device simulator) which is used for testing of hardware and implementation of HART converter. Simulator has facility to simulate single (point to point) with HART device id 0 and multiple (multipoint) with HART id from 0 to 15 HART device option. It supports more than twenty HART commands (like: cmd0/1/2/3 ...). Simulator provide HART device id, process value and unit code change option. The four main values and units of PV/SV/QV/TV of HART command 3 can be set for every HART simulation device. ICP das i-7567 (USB to HART) converter is used which is connected to HDS software and HART converter.

Figure 6 shows serial log of HART converter. To read data from HART first need to send cmd0 (read unique identifier) command. Command 0 is typically the first step in discovering devices on the HART network which gives fundamental information about a HART device. Master sends request to all connected device from id 0 to id 15 corresponding slave device give response which contain device type, manufacturer id, universal command revision, software version, hardware version, device unique identifier. After getting CMD0 response CMD1/ CMD2/ CMD3 required to send which provide sensor data. HART CMD3 read all dynamic variables with % of current output. Command 3 response data field contains mA reading, PV (primary variable) units code and value, SV (secondary variable) units code and value, TV (tertiary variable) units code and value, QV (quaternary variable) units code and value are values and mA filed. Further this data converted in to IEEE 754 float format to get actual reading.[9]

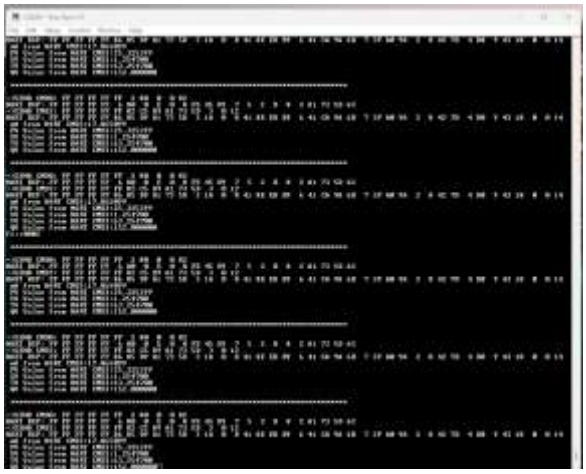

Fig. 6: Hardware UART Logs for HART Command and DATA

Figure 5 and figure 6 shows HART simulator values gets read and match with actual reading by HART converter by implementing HART protocol.

5. Future directions

In industrial applications serial communication does not directly support to maximum industrial controller so we can do implementation of some industrial standard protocol over the serial communication such as MODBOS ASCII/MODBUS RTU. We can Integrate RTOS which allows implementation of tasks with different priorities, ensuring that critical tasks, such as data processing and communication, are executed on time by assigning priorities. The RTOS also provides buffer management, where HART data can be stored and forwarded to Serial port which eliminating timeout delays at the host side. Also implementation of artificial intelligence (AI) within the HART converter can enhance predictive maintenance capabilities by analysing operational data to predict potential failures before they occur. Additionally, advanced error detection and correction algorithms can be integrated to improve the reliability and accuracy of data transmission between devices.

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