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HARDWARE IMPLEMENTATION OF DELAY EFFICIENT CDMA BASED ROUTING FOR NoC APPLICATIONS

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***Abstract*— The network on chip is an emerging approach for the implementation of the on chip communication architecture. It has emerged as underlying infrastructure for communication between intellectual property cores. It is the solution for communication architecture of future system. In order to improve the design complexity and area efficiency the structure of CDMA –NoC with the standard basis code is implemented. In the gate level MUX is used in the transmitter and receiver module. In the transmitter module data from different senders are encoded with an orthogonal code of a standard basis code and these coded data are mixed by the MUX operation. Then these data's are transmitted through NoC. In the receiver module these coded data's can be retrieved by the MUX operation between the data and the orthogonal code. After a simple accumulation the original data can be reconstructed.**

***Index Terms*— CDMA, MUX, NoC, Encoding/Decoding, Standard basis code.** *(key words)*

I. INTRODUCTION

Network on chip or network on a chip (NoC or NOC) is a communication subsystem on an integrated circuit (commonly called a "chip"), typically between intellectual property (IP) cores in a system on a chip (SoC). NoCs can span synchronous and asynchronous clock domains or use unclocked asynchronous logic. NoC technology applies networking theory and methods to on-chip communication and brings notable improvements over conventional bus and crossbar interconnections. NoC improves the scalability of SoCs, and the power efficiency of complex SoCs compared to other designs [1]. The Network on chip is an emerging approach for the implementation of on chip communication architecture. The system on chip designs incorporating large no. of processing cores and modular structure of Network on chip makes a fitting replacement for system on chip [6]. Network on chip is intended to solve the shortcomings of these, by implementing a communication network of switches, micro routers and resources, System on chips are not containing IP cores only and traditional methods for communication such as bus are not suitable solution for future System on chips. The Network-on-Chip has emerged as underlying infrastructure for communication between Intellectual Property cores [4], [5]. Network on chip is solution for communication architecture of future System on chips that are composed of switches and IP cores where communicate among each other through switches. Between IP cores data move in the form of packet.

Code division multiple access (CDMA) is a channel access method used by various radio communication technologies [2]. CDMA is an example of multiple accesses, where several transmitters can send information simultaneously over a single communication channel. This allows several users to share a band of frequencies (see bandwidth). To permit this without undue interference between the users, CDMA employs spread-spectrum technology and a special coding scheme (where each transmitter is assigned a code).

II. EXISTING SYSTEM

The CDMA technique has recently attracted research attentions in the NoC community. To show the advantages of CDMA NoC, Kim used Walsh codes [3] to distinguish different senders and develop a hierarchical star mesh topology to handle a large number of communication processors. To further improve the CDMA NoC performance, a globally asynchronous locally synchronous (GALS) CDMA NoC is modeled and simulated [6].

A. Structure of CDMA NoC

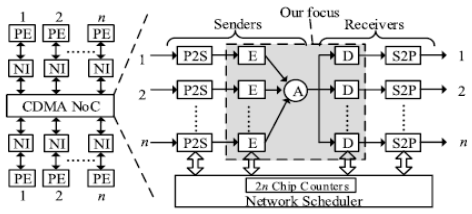

Fig. 1. Structure of CDMA

Figure1 shows the basic structure of applying CDMA technique to NoC with a star topology [8]. The PE executes tasks of the application and network interface (NI) divides data flows from PE into packets and reconstruct data flows by using packets from NoC. In the sender, packet flits from NI are transformed to a sequential bit stream via a parallel-to-serial (P2S) module.

B. CDMA Encoder

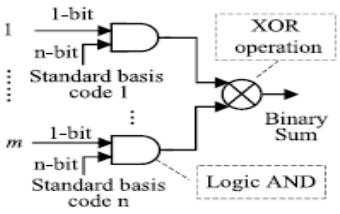

Fig. 2. Schematic Diagram of Encoder

Figure 2 shows the Schematic diagram of encoder. An original data bit from a sender is fed into an AND gate in a chip-by-chip manner, and it will be spread to n-chip encoded data with an orthogonal code of a standard basis [7]. Then, the encoded data from different senders are mixed together through an XOR operation, and a binary sum signal is generated. Therefore, the output signal is always a sequence of binary signal transferred to destination using one single wire.

C.CDMA Decoder

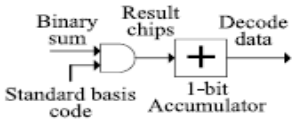

Fig. 3. Schematic Diagram of Decoder

Figure 3 shows the schematic diagram for decoder. It consists of standard basis code, binary sum and 1-bit accumulator. It explains the Standard Basis decoding method. When the binary sum signal arrives at receivers, an AND operation is taken between the binary sum and the corresponding orthogonal code in chip by chip manner. Then, the result chips are sent to an accumulator. After m-chips are accumulated (m is the length of the orthogonal code), the output value of the accumulator will be the corresponding original data. There is always only one chip equal to 1 and all other chips are equal to 0 for an orthogonal code in standard basis. Hence, the maximal accumulated value in the SB accumulator is 1 and it can be stored in a 1-bit register.

III. PROPOSED SYSTEM MODEL

In the existing system standard basis code have been proposed with the AND and XOR operation in the encoder part and in the decoder part AND operation and one accumulation is used. To reduce the design complexity, in the proposed method MUX is implemented in the gate level modification. The structure of CDMA is same for the existing and the proposed system, the design of gate level only changed. In the encoder part the AND gate and XOR gate is replaced by the MUX. In the decoder part the AND gate is replaced by the MUX.

A. Proposed Structure of CDMA NoC

The structure of proposed CDMA structure and the existing structure is the same one. The encoder part is replaced with the MUX and decoder part is replaced with the MUX. Star topology has implemented in this CDMA structure.

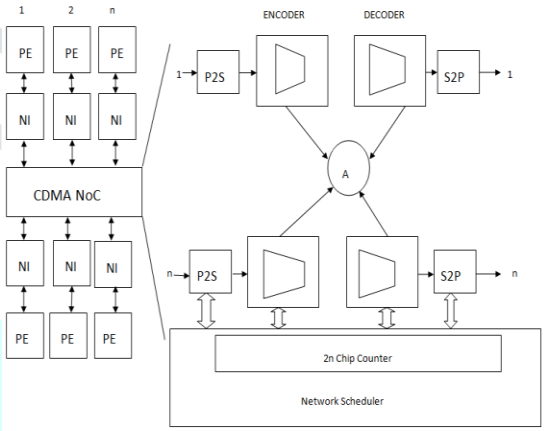

Fig. 4. Proposed Structure of CDMA NoC

Figure 4 shows the proposed structure of CDMA NoC. It consists of processing elements, network interface, parallel to serial converter, and serial to parallel converter, encoder as sender and decoder as receiver. The Processing Element will assign a task to the Network Interface. The Network Interface flits the packets. These packets are send to P2S Module. The P2S module sends the packets to encoder. The encoder will encode the data using standard basis code.

The data from different senders are combined by the addition module. The data's are considered as binary sum. The combined binary sum data's are send to decoder. Then the decoder will decode the data using the standard basis code. After a simple accumulation the original can be retrieved. The data send to S2P module to convert the data parallel packets. Then these packets are Network Interface. The network scheduler receives the request and assigns a proper spreading code to the sender and the receiver. For multiple sender arbitration scheme is applied. Chip counter is used to calculate the orthogonal chips for encoding/decoding operation.

i. Processing Elements

A Processing Element (PE) design is provided for improving performance and reducing the number of memory ports by eliminating the dedication of ports to specific functional units and by providing data paths to other forward results from functional unit outputs directly to other functional unit inputs. In the rapid growth of computational complexity processing elements are integrated in to single chip. The processing element executes a task of applications to the

network interface. The N number of processing elements can be used.

ii. Network Interface

A Network Interface (NI) is the point of interconnection between a computer and a private or public network. It is generally a network interface card (NIC), but does not have to have a physical form. Instead the network interface can be implemented in software.

In computing, a Network Interface is a system's (software and/or hardware) interface between two pieces of equipment or protocol layers in a computer network. A network interface will usually have some form of network address. This may consist of a node Id and a port number or may be a unique node Id in its own right. Network interfaces provide standardized functions such as passing messages, connecting and disconnecting, etc.

Network Interface is useful for a multi-homed system, which is a system with multiple NICs. Using Network Interface, you can specify which NIC to use for a particular network activity [8]. To send the data, the system determines which interface is used. However, if you have a preference or otherwise need to specify which NIC to use, you can query the system for the appropriate interfaces and find an address on the interface you want to use. When you create the socket and bind it to that address, the system uses the associated interface. Network Interface to identify the local interface on which a multicast group is to be joined.

In the CDMA NoC architecture Network Interface will divide the data flows from processing elements (PE) in to packets and reconstruct the data flows by using packets from NoC [11]. The packets are flits from NI and then it transformed to a sequential bit stream to the sender via a P2S module.

Reconstructed sequential bit streams are transferred to the S2P module. Then these files are transferred to NI [9]. The Network Interface transformed to multiple bit streams is to make tradeoff between the power, area, cost and latency of the packet transfer.

iii. Parallel to Serial (P2S) Module

A conversion process in which the stream of data elements received all at once is converted and sent as a stream of data at one bit at a time. Conversion of a stream of multiple data elements, received simultaneously, into a stream of data elements transmitted in time sequence.

The data packets from the sender are flits from NI to the P2S module. The P2S module will convert the stream of parallel bit to the serial bit and these sequential bits are sending to the encoder.

iv. Serial to Parallel (S2P) Module

Conversion of a stream of data elements received in time sequence, i.e. one at a time, into a data stream consisting of multiple data elements transmitted simultaneously. In the receiver block, decoding module reconstruct the data chips. These sequential bit streams are transformed to packet flits by serial to parallel (S2P) module.

v. Addition Module

In the encoding module data from different senders are encoded. The data packets of different encoding modules are added together by the addition module [13].

vi. Network scheduler

A Network Scheduler, also called packet scheduler, is an arbiter program on a node in packet switching communication network. It manages the sequence of network packets in the transmit and receive queues of the network interface controller, which is a circular data buffer. There are several network schedulers available for the different operating system kernels, which implement many of the existing network scheduling algorithms.

The network scheduler logic decides, in a way similar to statistical multiplexers, which network packet to forward next from the buffer. The buffer works as a queuing system, storing the network packets temporarily until they are transmitted. The buffer space may be divided into different queues, with each of them holding the packets of one flow according to configured packet classification rules; for example, packets can be divided into flows by their source and destination IP addresses. Network scheduling algorithms and their associated settings determine how the network scheduler manages the buffer. Also, network schedules are enabling accomplishment of the active queue management and traffic shaping. In the CDMA NoC structure, network scheduler receives the transmitting requests from sender and assigns a proper spreading code to the senders and requested receivers [14].The all-zero code word is assigned to nodes having no data to transmit/receive. When the multiple senders requesting the same receiver, the scheduler will apply an arbitration scheme.

vii. Chip Counter

In digital logic and computing, a counter is a device which stores (and sometimes displays) the number of times a particular event or process has occurred, often in relationship to a clock signal. The most common type is a sequential digital logic circuit with an input line called the "clock" and multiple output lines. The values on the output lines represent a number in the binary or BCD number [15] system. Each pulse applied to the clock input increments or decrements the number in the counter.

In the structure of CDMA NoC, the chip counter calculates how many orthogonal chips are used in one encoding/decoding operation. Each node needs two chip counters, one for the sender and other for the receiver.

B. Proposed CDMA Encoder

An encoder is a device, circuit, transducer, software program, algorithm or person that converts information from one format or code to another, for the purposes of standardization, speed or compressions. A device used to change a signal (such as a bit stream) or data into a code. A simple encoder assigns a binary code to an active input line. Priority encoders establish the priority of competing inputs (such as interrupt requests) by outputting a binary code representing the highest-priority active input. For producing n no. of output when there is 2^n no. of inputs.

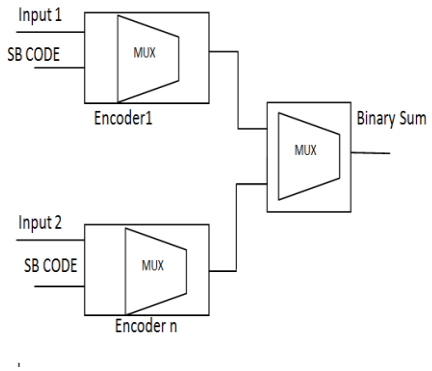

Fig. 5. Proposed Block - Encoder

Figure 5 shows the proposed block diagram of encoder. The encoder block consists of MUX for the encoding operation. The source data from each sender are separately encoded with the orthogonal code of a standard basis code by using MUX operation. An original data bit from sender is fed in to MUX in a chip by chip manner, and it will be spread to n-chip encoded data with the orthogonal code of standard basis. Here the standard basis code consists of N number of bits; these bits are called as chips [9]. The encoded data from different senders are mixed together through a MUX operation, and a binary sum signal is generated. The output signal is always a sequence of binary signal transferred to destination using one single wire.

C. Proposed CDMA Decoder

A decoder is a circuit that changes a code into a set of signals. It is called a decoder because it does the reverse of encoding. A device or program that translates encoded data into its original format (e.g., it decodes the data).

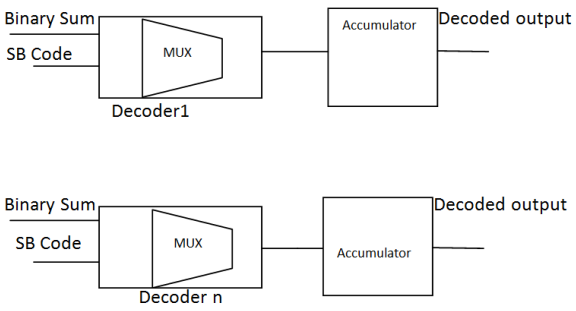

Fig. 6. Proposed Block Diagram – Decoder

Figure 6 shows the proposed block diagram of decoder. The SB decoding scheme is done in the decoder block. When the binary sum signal arrives at receivers, an MUX operation is taken between the binary sum and the corresponding orthogonal code in chip-by chip manner. Then, the result chips are sent to an accumulator [10]. After m-chips are accumulated (m is the length of the orthogonal code), the output value of the accumulator will be the corresponding original data. Note that there is always only one chip equal to 1 and all other chips are equal to 0 for an orthogonal code in standard basis [12]. Hence, the maximal accumulated value in the SB accumulator is 1 and it can be stored in a 1-bit register. Therefore, in the SB decoding module, only one MUX and an accumulator with one 1-bit register are used, resulting in less logical resources.

The CDMA NoC structure consists of encoder and decoder. In the encoder and decoder block MUX is designed to improve the efficiency of the area. In this project we propose a new CDMA encoding/decoding method for on chip communication. It is realized by using a simple logic, less power and area. The standard basis code is used as a spreading code. It will decrease the encoding/decoding latency and increase the maximum throughput of NoCs.

IV. SIMULATION RESULT OF CDMA NOC

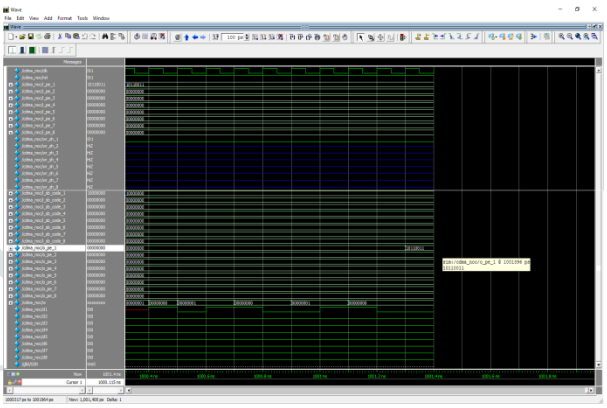

Fig. 7. Simulation Result of CDMA NoC

Figure 7 shows the simulation result of CDMA Noc. This shows the overall result of CDMA after the implementation of encoding and decoding method.

V. NETLIST OF PROPOSED SYSTEM

A Netlist is a description of the connectivity of an electronic circuit. A Netlist consists of list of terminals of the electronic component of the circuit. The fundamental purpose of every Netlist is to convey the connectivity information.

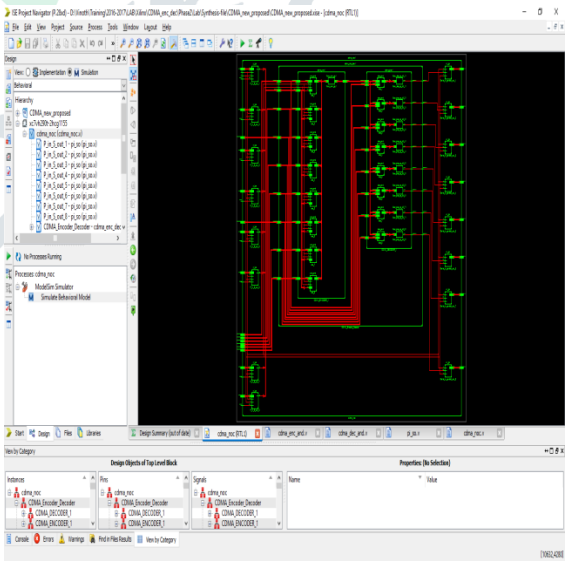

Fig. 8. RTL View of Proposed system

Figure 8 shows the RTL view of proposed system. This Netlist consists of a encoder and decoder block of the CDMA NoC.

IV. CONCLUSION

Table 1 shows the comparison of existing and proposed system. Each one having the comparison of units between the existing system and proposed system. In 4bit adder proposed system has units. In one bit register units are less than existing system. So less registers will give more efficiency to the circuit.

Table 1 Comparison of Existing and Proposed System

S.NO	UNITS	EXISTING SYSTEM	PROPOSED SYSTEM
1	4-BIT ADDER	0	8
2	1-BIT REGISTER	136	8
3	4-BIT REGISTER	0	8
4	8-BIT REGISTER	16	32
5	32-BIT 2- TO-1 MULTIPLEXER	0	72
6	8-BIT 2- TO -1 MULIPLEXER	0	8
7	1-BIT XOR	8	8
8	8-BIT XOR	1	1
9	4-BIT UP COUNTER	8	8
10	FLIP FLOPS	264	264

In this project code division multiple access (CDMA) technique has applied to network on chip. To improve the performance of the on chip communication infrastructure the standard basis code is used for encoding and decoding. To improve the area efficiency and power saving, the encoder block and decoder block is designed with the MUX. By using this design and structure the area efficiency has improved.In future gate level modification can be done to improve the efficiency of the on chip communication network.

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