



Design and Analysis of an Approximate 8-Bit Multiplier Using Low Power Compressor

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Abstract: In modern digital systems, energy efficiency has become a crucial consideration, particularly in applications where power and area constraints are critical. This paper presents a novel 8-bit multiplier design utilizing approximate computing techniques to reduce the logic resource requirements, power consumption, and area, while maintaining a reasonable level of accuracy. The design incorporates Approximate Condition-based Majority Logic Compressors (ACMLC) and Compensator Approximate Compressors (CAC) for efficient multiplication. A detailed comparison of the existing method and the proposed method reveals that the proposed design achieves a reduction in LUT usage (from 86 to 70) and power consumption, both static and dynamic, with only a slight trade-off in accuracy. The proposed approach offers a promising solution for low-power and area-efficient multipliers, suitable for applications such as embedded systems, signal processing, and machine learning accelerators.

I. INTRODUCTION

In the rapidly evolving domain of digital electronics, the demand for high-performance yet energy-efficient hardware components is at an all-time high. Multiplication, being one of the most fundamental operations in computing, significantly influences the performance and resource consumption of many digital systems. Applications such as digital signal processing (DSP), artificial intelligence (AI), cryptography, and image processing require intensive arithmetic computations. However, traditional multiplier designs emphasize precision, often at the expense of increased power consumption, area, and latency.

With the proliferation of resource-constrained environments such as IoT devices, mobile processors, and edge AI platforms, there is a growing need to strike a balance between accuracy and efficiency. This has given rise to the concept of approximate computing, a paradigm that intentionally introduces acceptable inaccuracies to achieve substantial gains in speed, power, and silicon area. Approximate computing is particularly suitable for error-resilient applications, where minor deviations from exact results are tolerable and do not significantly affect the system's functionality or output quality. In this context, approximate multipliers play a pivotal role. By simplifying logic operations, reducing the number of transistors, and truncating non-critical computation paths, these designs achieve reduced switching activity, lower leakage current, and minimal critical path delays. However, designing an approximate multiplier that preserves an optimal trade-off among accuracy, area, power, and delay remains a significant challenge.

Recent research has explored the use of approximate compressors, which are key building blocks in partial product reduction within multipliers. Compressors like 4:2 compressors, when optimized, can drastically reduce the number of adders and interconnects. The existing methods often suffer from high negative error rates or require complex error recovery modules, which offset the benefits of approximation. To address these limitations, this paper proposes an 8-bit approximate multiplier architecture that utilizes Accumulative Carry-Managed Logic Cells (ACMLC) and Carry-Aware Compressors (CAC). These components are designed to minimize negative errors, eliminate the need for error recovery circuits, and significantly reduce both the transistor count and power consumption. Moreover, the design introduces constant truncation for the least significant bits (LSBs), further reducing logic complexity with negligible impact on accuracy. By integrating these novel techniques, the proposed multiplier achieves reduced LUT count, lower static and dynamic power, and a smaller silicon footprint. The architecture is particularly beneficial for energy-efficient, real-time computing systems where approximate results are acceptable. This makes the design an ideal candidate for low-power VLSI systems, machine learning accelerators, and battery-operated embedded platforms.

II. LITERATURE SURVEY

Approximate multipliers have gained significant attention in recent years as an effective means to reduce power consumption, chip area, and computation time in error-resilient applications. Sharma and Choudhury [1] proposed efficient approximate multipliers specifically designed for low-power systems, highlighting their suitability for energy-constrained environments. Yadav and Kumar [2] introduced a high-performance multiplier for signal processing, demonstrating how approximate designs can maintain throughput while optimizing power and area. Techniques such as truncated multiplication have also been explored by Kumar and Agarwal [3] to strike a balance between power efficiency and output precision. Bansal and Jain [5] further investigated the trade-offs between hardware resources and performance, suggesting that approximate

architectures are highly suitable for compact VLSI systems. Similarly, Roy et al. [6] and Jain et al. [7] presented designs targeting DSP applications, emphasizing reductions in switching activity and error resilience.

Advanced adder structures like carry-select adders [4][8] and approximate logic circuits [9][10] have been integrated into multiplier designs to enhance speed and reduce complexity. Zhang et al. [11] proposed error-compensated high-speed approximate multipliers for DSP systems, achieving low delay without significant degradation in accuracy. Recent efforts also include the development of approximate compressors and reduced partial product techniques [12], which minimize logic depth and power usage. For applications in image processing and AI, Singh et al. [13] and Patel et al. [14] demonstrated that low-power approximate multipliers could be effectively deployed without compromising overall system functionality. These collective contributions form the foundation for developing the proposed ACMLC and CAC-based multiplier, offering a compelling balance between performance, energy efficiency, and computational accuracy.

III. EXISTING METHODOLOGY

In conventional multiplier architectures, accuracy is prioritized at the cost of increased area, power, and delay. Traditional designs typically utilize exact 4:2 compressor circuits for partial product reduction and ripple carry adders for final summation. While these components ensure high precision, they involve large numbers of transistors and complex logic paths, contributing to higher power consumption and increased chip area. Moreover, as the size of the multiplier increases, the number of partial products and intermediate addition stages grow, worsening the timing and energy constraints—especially problematic for portable or battery-operated devices.

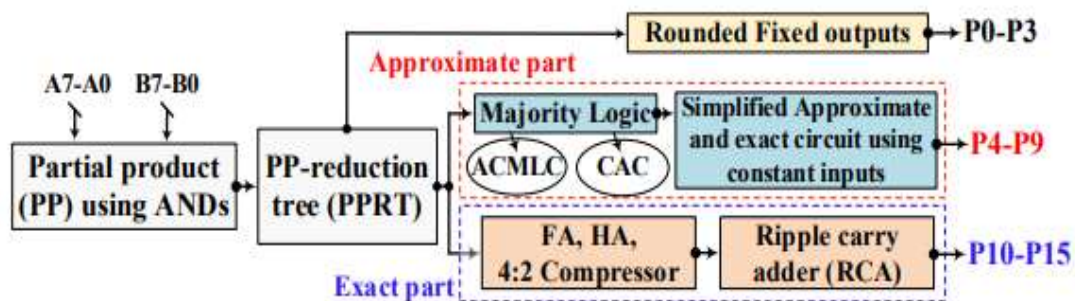


Figure: 1 Existing design flow of 8-bit multiplier

To address some of these challenges, researchers have introduced majority logic-based approximate compressors. These utilize the principle of majority voting among inputs to simplify logic and reduce transistor count. For example, in an ML (Majority Logic)-based compressor, some inputs are ignored or fixed to a constant value to reduce circuit complexity. While this method decreases the number of logic gates and switching activity, it introduces inaccuracies in the output, leading to both positive and negative errors. To control these inaccuracies, earlier designs incorporated Error Recovery Modules (ERMs), which restored the most critical bits. However, ERMs add to overall design complexity and partially negate the benefits of approximation in terms of area and power savings.

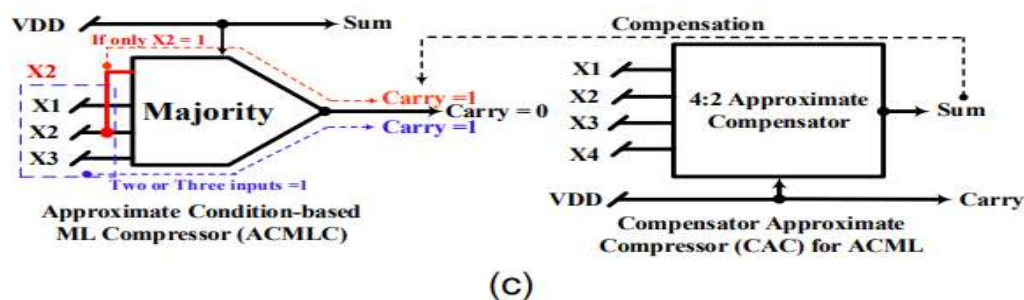


Figure: 2 Schematics of the compressor circuits (a): Exact. (b): ML-based, and (c): ACMLC and CAC, respectively.

Additionally, in some existing 8-bit multiplier designs, truncation techniques are employed by ignoring the least significant bits (LSBs) of the partial products. Although truncation significantly reduces hardware complexity, it increases error distance, particularly in scenarios where the LSBs contribute meaningfully to the final output. Some architectures attempt to mitigate this by using hybrid approaches that mix exact and approximate components. Despite these efforts, many existing designs fail to deliver a well-balanced trade-off across all critical parameters—area, power, delay, and accuracy. These limitations motivate the development of a new multiplier architecture using more optimized compressors such as ACMLC and CAC, which aim to simplify hardware while minimizing critical negative error components without relying on error correction logic.

IV PROPOSED METHODOLOGY

The proposed method introduces an energy-efficient 8-bit approximate multiplier architecture that divides the multiplication process into three functional components: the Exact Component, the Approximate Component, and the Constant Truncated Component. This structured approach is designed to target different significance levels of partial products with varying levels of accuracy. The Exact Component is responsible for computing the most significant bits (MSBs), where precision is critical. It uses conventional full adders and half adders to ensure minimal error propagation in the higher-order bits. This guarantees that the core computational accuracy of the multiplier is preserved, especially in applications where MSBs heavily influence the final result.

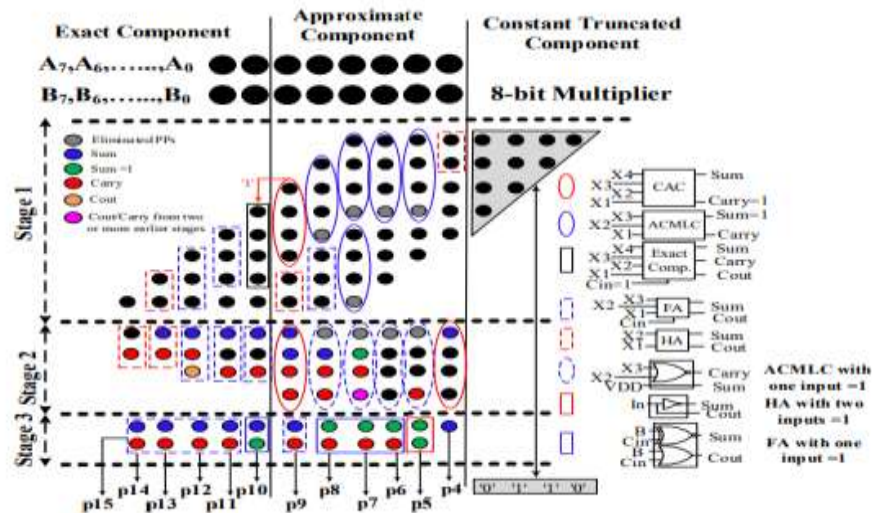


Figure 3: Proposed multiplier schematic using the proposed ACMLC-based compressor and CAC

The Approximate Component is applied to the middle-order bits, where a balance between efficiency and accuracy is required. This section utilizes Accumulative Carry-Managed Logic Cell (ACMLC)-based compressors and Carry-Aware Compressors (CAC) to reduce hardware complexity while maintaining acceptable error margins. The ACMLC significantly reduces the number of transistors and simplifies Boolean logic by using a fixed sum output and selectively handling carry generation. The CAC, meanwhile, improves the accuracy of carry propagation across approximate and exact components without the need for error recovery modules. This targeted use of approximation helps reduce power consumption and area, while minimizing the risk of significant computational errors.

Finally, the Constant Truncated Component eliminates the least significant partial products (LSBs) altogether or replaces them with fixed logic values. In the proposed design, the lowest four LSBs are fixed to a constant bit pattern (e.g., 0110), effectively eliminating redundant logic and saving additional AND gates. This greatly simplifies the multiplier circuit by reducing the number of partial product generators and logic levels. The combined use of truncation, approximate compressors, and exact logic ensures a balanced trade-off between performance metrics. The resulting architecture not only reduces LUT count and power consumption but also maintains a level of accuracy sufficient for error-resilient applications such as image processing, neural networks, and embedded systems.

V. RESULTS & DISCUSSIONS

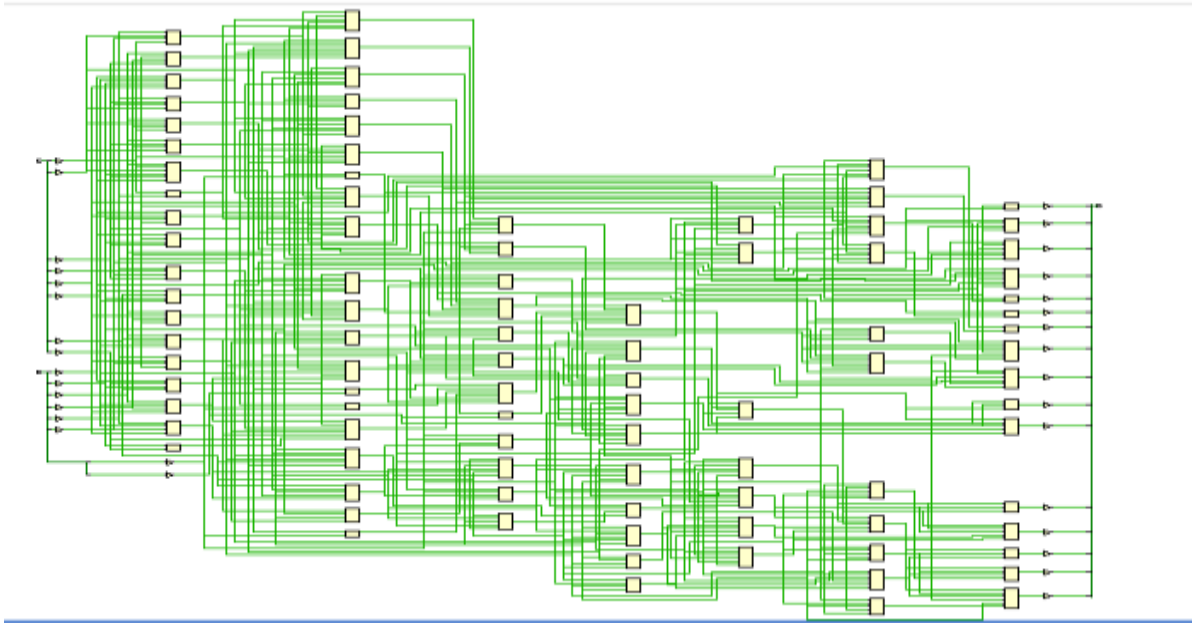


Figure 4: Schematic Diagram of Proposed Method

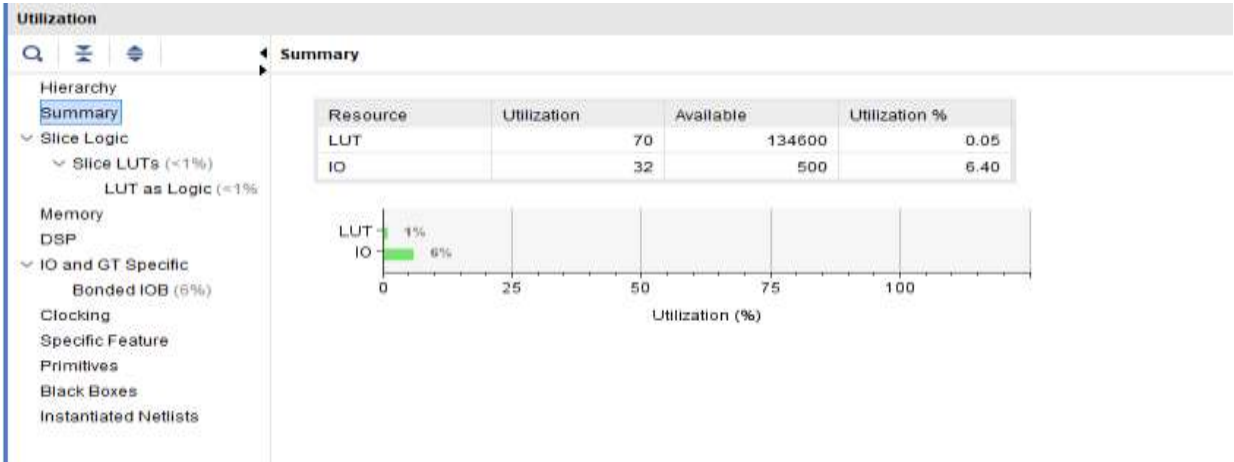


Figure 5: Area of the Proposed Method

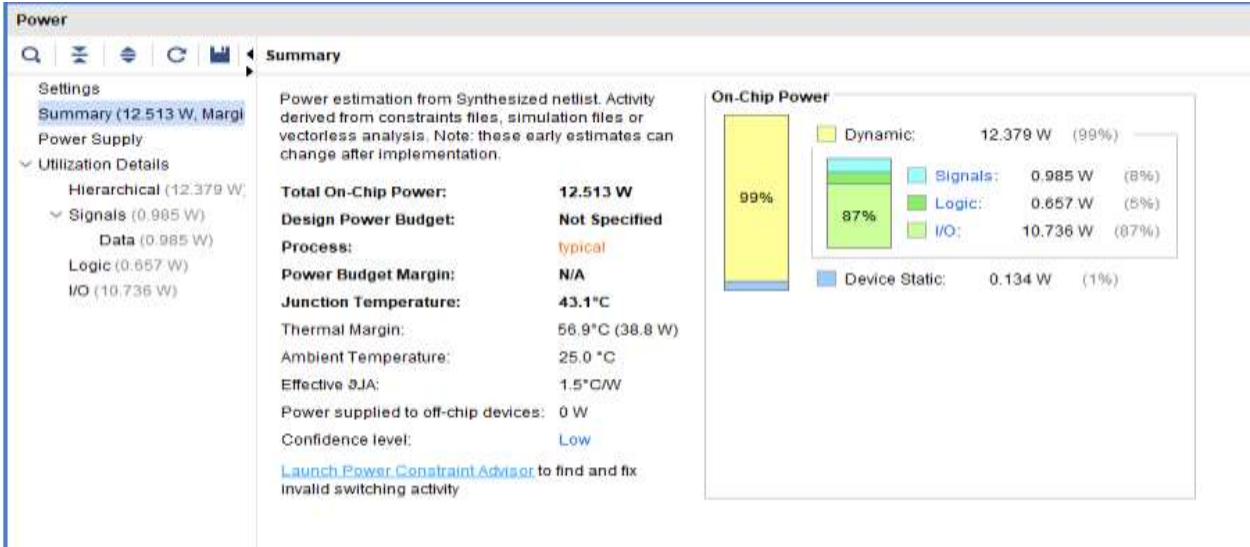


Figure 6: Power of the Proposed Method

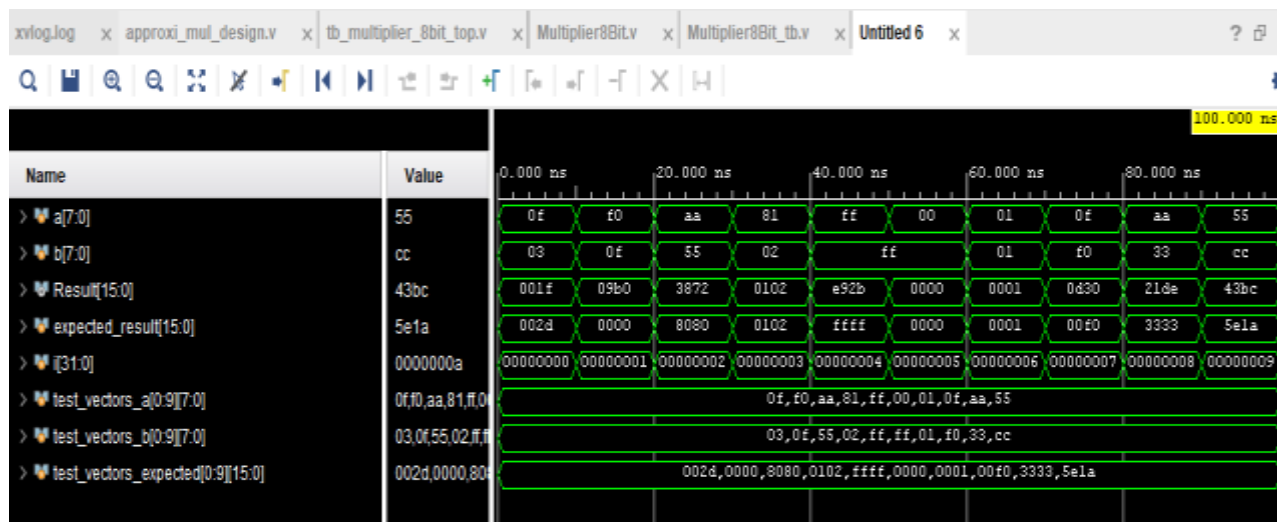


Figure 7: Simulation Diagram of the Proposed Method

Tabular column –I Results and Discussions

Multiplier Results			
S.No	Parameters	Existing method	Proposed Method
1	Area (LUT)	86	70
2	Static Power in Watts	0.135	0.134
3	Dynamic Power in Watts	12.498	12.379
4	Static Power in Watts	12.633	12.513

VII. CONCLUSION

The proposed 8-bit approximate multiplier architecture effectively addresses the growing need for energy-efficient and area-optimized digital designs in error-resilient applications. By integrating ACMLC-based compressors and CAC logic, the design achieves significant reductions in power consumption, LUT usage, and transistor count without the need for complex error recovery modules. The architecture strategically combines exact computation for critical bits, approximation for mid-order bits, and constant truncation for less significant bits, offering a balanced trade-off between accuracy and hardware efficiency. Simulation results demonstrate improved performance compared to traditional and ML-based multiplier designs, making the proposed method a suitable candidate for low-power applications such as image processing, IoT, and machine learning systems where minor computational errors are acceptable.

VIII. FUTURE SCOPE

The proposed approximate multiplier architecture opens several avenues for future research and enhancements. One potential direction is the implementation of adaptive approximation techniques, where the level of approximation can be dynamically adjusted based on real-time application requirements or operating conditions. This would allow systems to optimize power and performance based on workload sensitivity. Further improvements can also be achieved by integrating other low-power approximate components such as adders or ALUs into a complete energy-efficient data path. Hardware validation using FPGA or ASIC implementation is another important next step to evaluate the real-world applicability and performance of the proposed design under varying operating environments. Additionally, exploring the use of error-correcting modules or hybrid exact-approximate logic can improve the reliability of the design for more precision-sensitive applications, thereby expanding its usability across a broader spectrum of domains.

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