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DESIGN AND VALIDATION OF SPI CONTROLLER INTEGRATION FOR OPEN POWER PROCESSOR CORE BASED FABLESS SYSTEM ON CHIP(SOC)

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ABSTRACT: The Serial Peripheral Interface (SPI) is a synchronous communication protocol known for enabling fast, full-duplex data exchange between microcontrollers and peripheral devices. Its high-speed performance makes it ideal for applications that require efficient and rapid data transfer. This paper presents the design and verification of an SPI controller integrated with the A2O Core, a fabless System-on-Chip (SoC) developed within the OpenPOWER processor architecture. The goal is to enhance the A2O Core's capability to interface effectively with external peripherals. The controller is designed using Verilog HDL and verified through simulation and synthesis using the Xilinx Vivado toolset. The integration process involves creating a hardware description, functional verification, developing an AXI-compliant wrapper, and connecting the controller via an AXI interconnect to the A2O Core. This structured design approach enables scalable, high-speed peripheral communication and provides a reusable SPI interface suitable for future OpenPOWER-based processor implementations.

***Index Terms*- A2O, SPI, AXI Interconnect, SoC, Verilog**

I.INTRODUCTION

The swift advancement of embedded systems and open-source hardware has highlighted the demand for robust, adaptable communication protocols to connect microcontrollers and processors with peripheral devices. The Serial Peripheral Interface (SPI), a synchronous serial communication standard, has become a pivotal solution for these applications due to its full-duplex functionality and rapid data transfer capabilities, making it ideal for real-time systems requiring efficient data exchange between a master device and one or more slave peripherals. As depicted in Figure 1, SPI utilizes a straightforward four-wire interface—consisting of Serial Clock (SCLK), Master Out Slave In (MOSI), Master In Slave Out (MISO), and Slave Select (SS)—allowing it to achieve data transfer speeds that often surpass those of asynchronous protocols such as I²C or UART.

This work centers on the integration of an SPI controller with the A2O Core, a 64-bit open-source processor, using a structured AXI-based interface within a custom System-on-Chip (SoC) design.

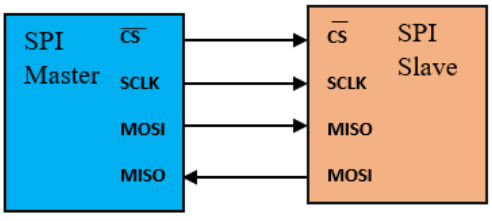

Figure 1: Architecture of SPI Four-Wire Interface

II. SPI-A2O INTEGRATION

The integration is designed to connect the processor core with peripheral devices through an optimized communication channel that promotes synchronization, adaptability, and enhanced performance. The system architecture is organized into distinct layers—from core processing to peripheral connectivity—each precisely defined to separate operational functions while ensuring fluid coordination throughout the system. This approach streamlines development and debugging processes, while also boosting the design's portability and scalability, making it ideal for diverse embedded and System-on-Chip (SoC) applications. The framework comprises three primary components: the A2O Core, the AXI Interconnect, and the SPI Controller, as shown in Figure 2.

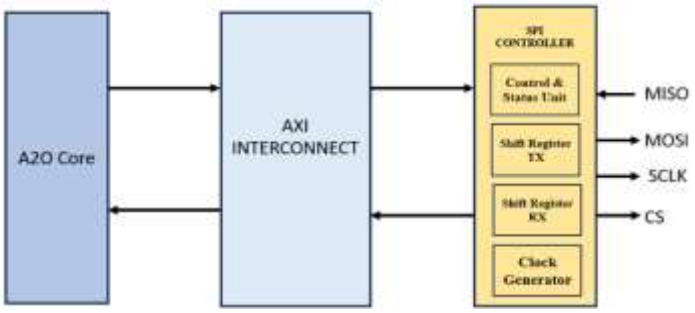

Figure 2: Architecture for Integrating SPI Controller with A2O Core

2.1 A20 Core

The A2O Core is a 64-bit, out-of-order, multi-threaded processor developed for the OpenPOWER SoC platform, engineered to optimize single-thread performance. It builds upon the modular framework of the A2I core and incorporates an Auxiliary Execution Unit (AXU) to enable support for diverse applications. Equipped with 2-way Simultaneous Multi-Threading (SMT) based on the POWER ISA 2.07 and fabricated using 45nm technology, it operates at frequencies exceeding 3 GHz. The core also functions as the master, managing SPI communication and processing data from peripherals.

2.2 AXI Interconnect

Built on the AMBA AXI4 protocol, the AXI Interconnect serves as a critical link between the A2O Core and the SPI Module, supporting AXI4, AXI4-Lite, and AXI3 standards. It manages multiple masters and slaves (up to 16 each) with a 32-bit address and data width. The interconnect facilitates clock domain crossing, ensures compliance with AXI read/write protocols, and supports burst transactions with adjustable bandwidth to enhance communication efficiency. Internally, it incorporates an arbiter to prioritize master requests, a decoder to route addresses to the appropriate slave, and a multiplexer (mux) to direct data flow as shown in Figure 3, optimizing system performance and resource allocation.

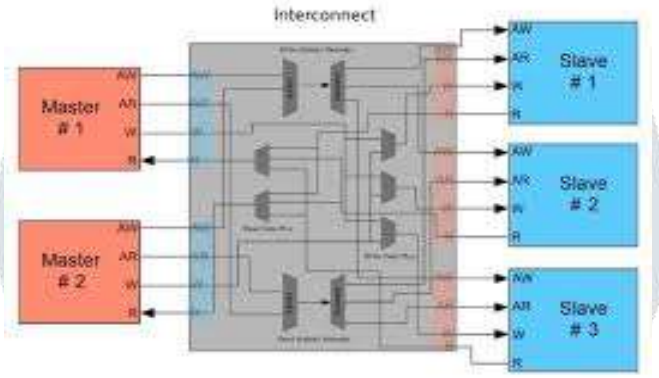

Figure 3: AXI Interconnect Multi-Master/Multi-Slave

2.3 SPI Module

The SPI module is a full-duplex master interface, crafted in Verilog HDL to align with the AXI architecture of the A2O Core. It functions in a single-master, single-slave setup, employing SPI Mode 0 (CPOL = 0, CPHA = 0) with an active-low chip select. The module handles 32-bit data and address widths, transmitting data in MSB-first sequence (from bit 31 to bit 0). Its core components—control unit, clock divider, shift register, and status register—facilitate dependable communication with diverse peripherals.

III. ARCHITECTURE IMPLEMENTATION AND DESIGN FLOW

The architecture is structured around a clear separation of interconnects and functional modules. At its core, the SPI controller is interfaced with an AXI interconnect, which serves as a communication bridge between the A2O processor core and peripheral devices. Data transmission proceeds through the following sequence: A2O Core → AXI Interconnect → SPI Module → Peripheral Device. The return path for data follows the same route in reverse, enabling full-duplex communication and synchronized control.

The design emphasizes modularity and hierarchical organization, allowing the SPI controller and its interfacing components to be easily scaled or reused in other SoC configurations. The architecture supports clean port mapping, consistent signal flow, and efficient clock domain management.

A procedural flow for design and verification includes:

- HDL implementation of the SPI module and AXI Interconnect
- Simulation and behavioral verification.
- Wrapper development for interfacing.
- Full-system integration with the A2O core.
- Functional validation through testbench simulations.

IV. BLOCK DIAGRAM FOR SPI INTEGRATION WITH A20 CORE

The block diagram for SPI Controller Integration with A2O Core in the OpenPOWER Processor via AXI Interconnect" provides a detailed visual representation of the system's hardware design. It highlights the structure of internal connections and the flow of signals between components. At the center of the diagram is the AXI Interconnect, functioning as the primary communication hub, with multiple input and output ports to manage data exchange between the A2O Core and various peripheral interfaces. As shown in Figure 4, the spi_axi_0 module is positioned on the right side of the layout, with the SPI signal lines—Serial Clock (SCLK), Master Out Slave In (MOSI), Master In Slave Out (MISO), and Slave Select (SS)—clearly marked and extending outward to denote connections with external devices. The diagram was generated using Xilinx Vivado's IP Integrator tool and effectively captures the port mappings and interconnection details, offering an optimized view of the system's communication framework to support high-performance data transfer.

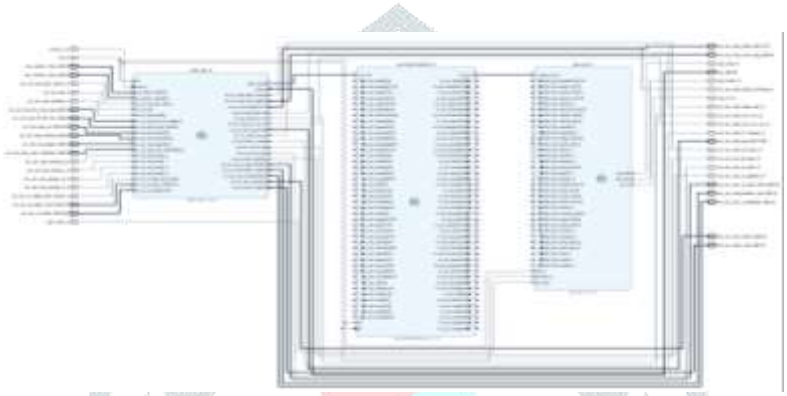

Figure 4: Detailed Block Diagram of the SPI Integration with A20 Core System Architecture, Generated Using Xilinx Vivado

V. SIMULATION RESULTS

The successful completion of AXI transactions highlights the reliability and effectiveness of the AXI Interconnect in managing data communication within the A20 Core environment. During write operations, the AXI control signals AWVALID and AWREADY are asserted at the clock's rising edge, confirming proper design functionality and data transfer initiation. Similarly, during read operations, the signals ARVALID and ARREADY are also asserted at the rising edge, verifying correct transaction execution. These interactions are illustrated in Figures 5(i), 5(ii), and 5(iii), which showcase the signal behavior throughout the communication process.

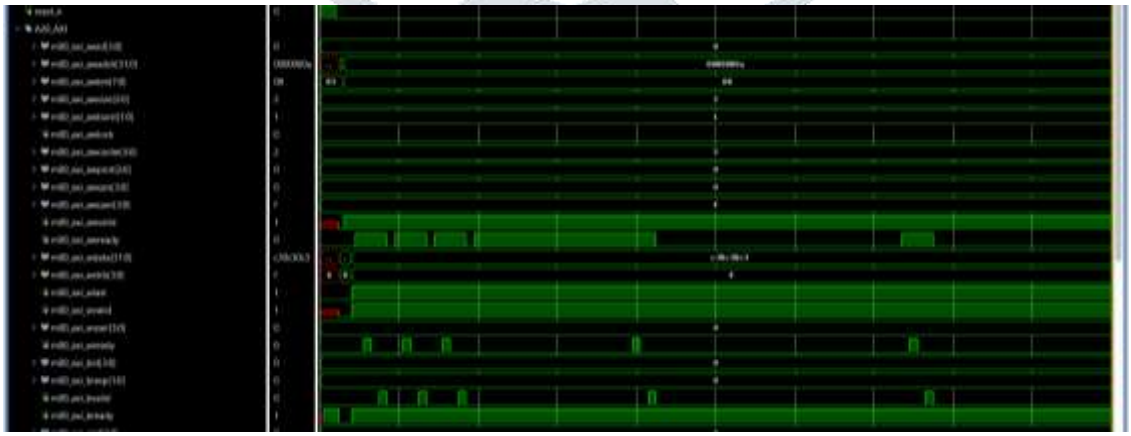

Figure 5 (i)

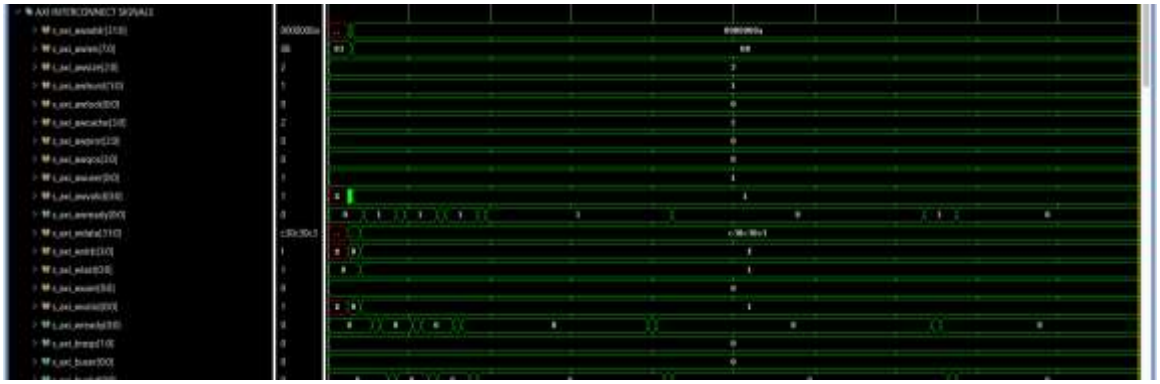

Figure 5 (ii)

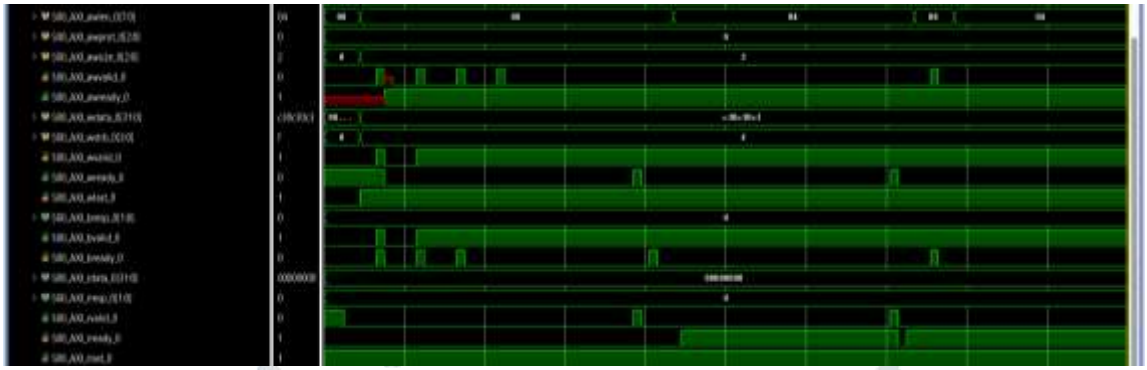

Figure 5 (iii)

Figure 5 (i), (ii), (iii) Read and Write Transactions

VI. CONCLUSION

This paper presented a detailed approach to designing and integrating an SPI controller with the A20 Core, developed within the OpenPOWER processor framework. The implementation was carried out using Verilog HDL and synthesized using the Xilinx Vivado toolset. The resulting architecture enables efficient, high-speed, full-duplex communication between the A20 Core and external devices. Simulation outcomes validate the system's reliability, with the successful assertion of key AXI interface signals—AWVALID, AWREADY, ARVALID, and ARREADY—at the rising edge of the clock, confirming accurate and stable data transactions. The development process involved structured phases such as hardware description design, wrapper development for AXI compliance, and seamless integration, all of which effectively addressed synchronization and interfacing challenges. This work delivers a modular, reusable SPI communication module that significantly enhances the functional scope of the A20 Core in embedded applications. Future developments will aim to improve timing consistency, extend compatibility with additional peripherals, and evaluate the design under real-world operating conditions to further support innovation in OpenPOWER-based SoC platforms.

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