JETIR.ORG ISSN: 2349-5162 | ESTD Year : 2014 | Monthly Issue
JOURNAL OF EMERGING TECHNOLOGIES AND INNOVATIVE RESEARCH (JETIR)
An International Scholarly Open Access, Peer-reviewed, Refereed Journal

Energy-Efficient for Reconfigurable Multiband DSP Hardware Generator for 5G and Beyond Transmitters

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Abstract: This paper proposes a novel reconfigurable multiband DSP architecture tailored for 5G and future communication systems, addressing the critical challenges of area, power, and hardware inefficiency in traditional designs. The architecture significantly reduces the usage of Look-Up Tables (LUTs) and flip-flops while maintaining high signal processing performance. It includes a multirate filter bank, carrier aggregation module, and dynamic reconfiguration logic, enabling real-time adaptability and multi-standard compatibility. The proposed solution achieves a 6% reduction in power consumption and supports both contiguous and non-contiguous band aggregation, making it ideal for advanced 5G scenarios. Experimental results demonstrate improved energy efficiency and scalability, positioning the system as a robust candidate for next-generation wireless transmitter design.

I. INTRODUCTION

The rapid evolution of wireless standards, from 4G to 5G and toward 6G, demands transmitter architectures that can deliver high throughput, low latency, and adaptability under varying spectrum conditions. Traditional DSP architectures used in wireless transmitters suffer from inflexibility, inefficient resource utilization, and high power consumption. As 5G networks increasingly rely on technologies like massive MIMO and carrier aggregation, it becomes imperative to adopt dynamic and scalable digital signal processing solutions. This paper introduces a reconfigurable multiband DSP architecture that meets these requirements by reducing power consumption and area while enhancing signal processing capability. By integrating programmable filters, dynamic reconfiguration logic, and efficient carrier aggregation, the proposed design offers a flexible platform suitable for next-generation wireless communication systems.

II. LITERATURE SURVEY

The evolution of wireless transmitter architectures for 5G and beyond has been significantly influenced by foundational and contemporary research. Mitola's seminal work on software-defined radio (SDR) [2] introduced the concept of reconfigurable hardware, which laid the groundwork for dynamic adaptation in communication systems. Harris [3] emphasized the critical role of DSP in enhancing signal quality, spectrum efficiency, and robustness in transmitters and receivers. The 3GPP TS 138 104 specification [1] formalized performance requirements like ACLR and EVM, encouraging the adoption of energy-efficient and flexible designs. To meet these stringent standards, Synopsys introduced ARC HS processors [4], which exemplify high-performance IP cores capable of hardware-software co-design, crucial for modern DSP systems. Lin et al. [5] further improved signal processing accuracy and efficiency through advanced interpolation techniques tailored for wireless communication, underscoring the need for optimized multirate filtering.

Advancements in digital RFICs [6] and digitally intensive wireless transceivers [7] have enabled tighter integration of DSP functions, reducing analog dependencies and enhancing scalability. Holma and Mogensen [8] explored the capacity gains from massive MIMO in macro-cell environments, stressing the need for scalable DSP solutions in 5G-Advanced and 6G. Multimode and SAW-less transmitter designs [9][10][11] have also been instrumental in reducing component count and enhancing reconfigurability. Research by Bhat and Krishnaswamy [12] on digital Cartesian RF-DACs highlighted trade-offs in power amplifier linearity and predistortion. Meanwhile, innovations in outphasing and polar transmitters [13][14][15] demonstrate the potential of all-digital, low-power transmission systems. Collectively, these studies establish the foundation for developing reconfigurable, energy-efficient DSP architectures that address the multi-band, multi-standard, and low-power demands of modern wireless systems.

III. EXISTING METHODOLOGY

Current transmitter systems use fixed-function DSP blocks that rely heavily on static interpolation filters and signal conditioning techniques. Although functional for basic operations, they lack the adaptability required for multiband carrier aggregation and real-time reconfiguration. These systems typically suffer from excessive hardware usage—requiring 113 LUTs and 152 flip-flops—and consume around 37.485W power, highlighting inefficiencies in resource management and scalability.

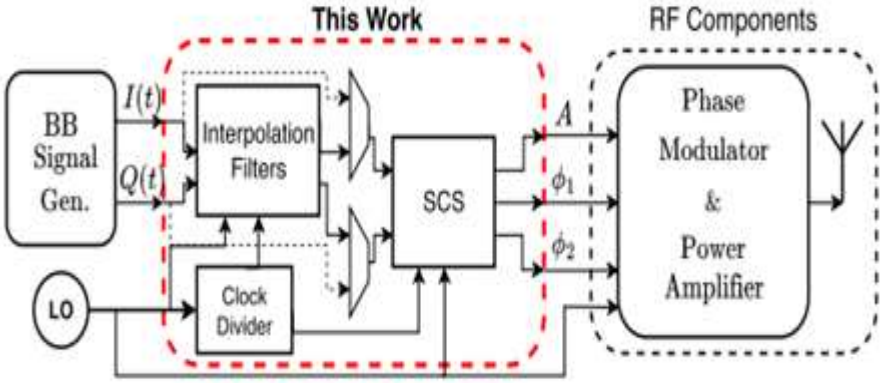

Figure: 1 Reconfigurable DSP processor between BB signal generator and RF components of a transmitter

Another critical drawback is the inability to support real-time modulation scheme switching or bandwidth reallocation, limiting their use in dynamic 5G networks. Fixed clock mechanisms further hinder energy efficiency, and traditional systems are ill-equipped for advanced features such as spectrum sharing or non-contiguous carrier aggregation. Thus, there's an urgent need for a reconfigurable DSP solution that adapts dynamically while consuming less area and power.

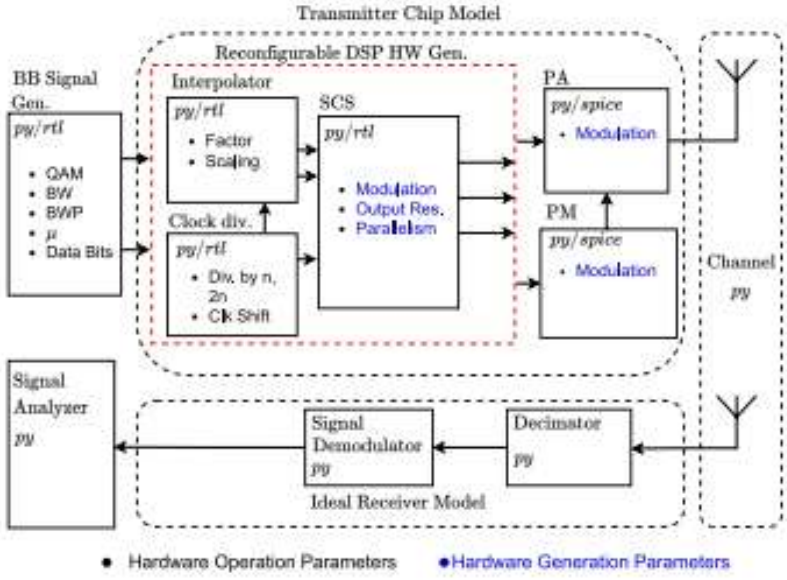

Figure: 2 Block diagram of the 5G transmitter chip model in TheSDK

IV PROPOSED METHODOLOGY

The proposed architecture introduces a reconfigurable DSP framework consisting of a multirate filter bank, carrier aggregation module, and dynamic reconfiguration logic. The filter bank replaces traditional interpolation filters with cascaded half-band and FIR filters, allowing efficient processing of multiple sub-bands. This not only improves spectral efficiency but also reduces the computational load, enabling power-efficient operation.

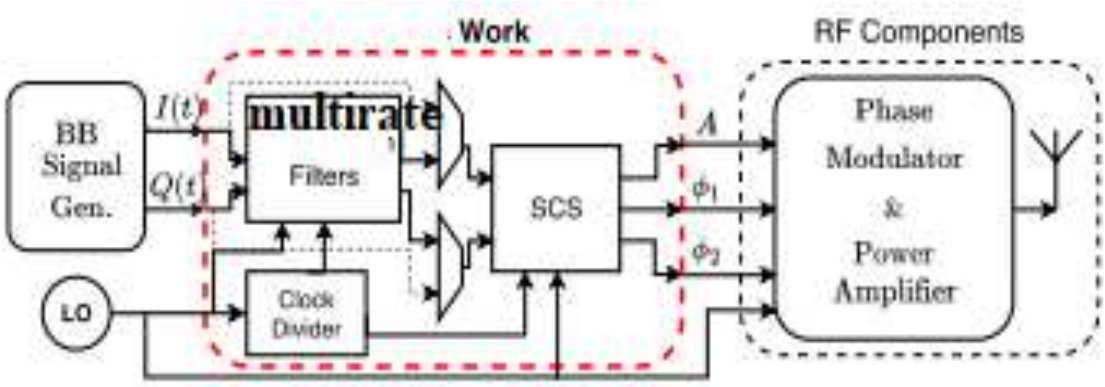

Figure 3: Proposed method Architecture

A carrier aggregation module combines multiple frequency bands—both contiguous and non-contiguous—into a unified output, critical for high-speed data transmission in 5G networks. Dynamic reconfiguration logic allows real-time adjustments of parameters like sampling rates and filter coefficients, enhancing system adaptability. With a configurable clock divider and optimized signal conditioning system, the architecture ensures synchronized, high-fidelity transmission with reduced energy consumption and hardware overhead.

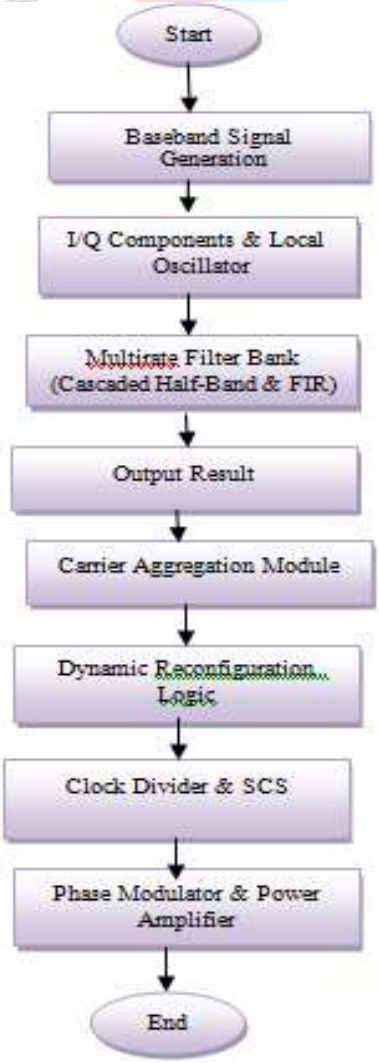

Figure 4: Implementation flow chart

V. RESULTS & DISCUSSIONS

The proposed DSP architecture was implemented using Verilog in the Xilinx Vivado environment. Compared to the existing system, LUT usage was reduced from 113 to 19 and flip-flop usage from 152 to 71. This compact design lowered the total power consumption from 37.485W to 35.263W, yielding a 6% energy savings. Despite this reduction, the system retained four DSP cores, ensuring uncompromised performance.

Simulation results confirmed improved spectral efficiency, dynamic reconfigurability, and scalability. The design's modularity supports seamless integration into various communication standards, including 5G NR, LTE, and Wi-Fi. These performance gains, along with reduced hardware footprint and energy efficiency, demonstrate the feasibility of the proposed architecture in real-world applications like IoT, base station equipment, and future 6G platforms.

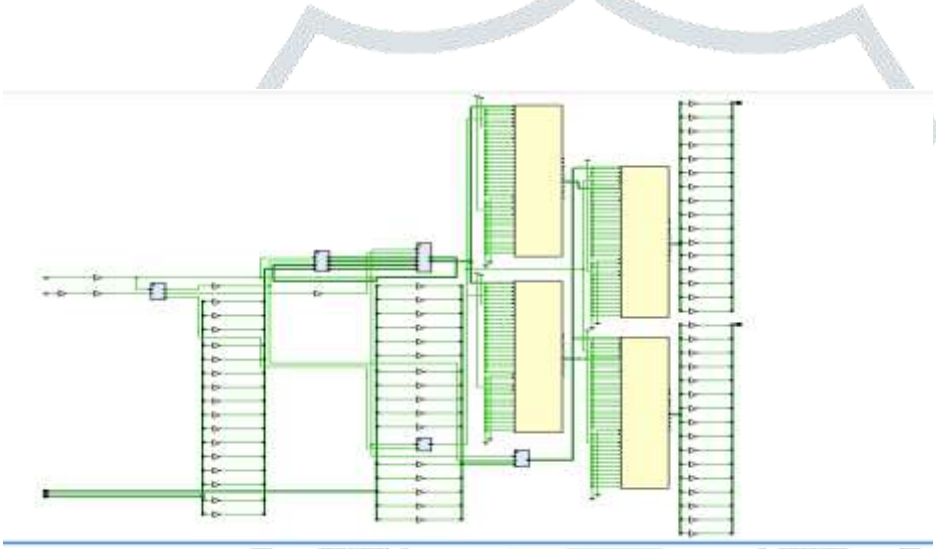

Figure 5: Schematic Diagram of Proposed method

The shown in fig.6 that area report for the proposed method demonstrates a significant reduction, with only 19 LUTs and 71 flip-flops being utilized (while the number of DSP cores remains at 4). This reduction in area not only lowers hardware costs but also improves overall design efficiency.

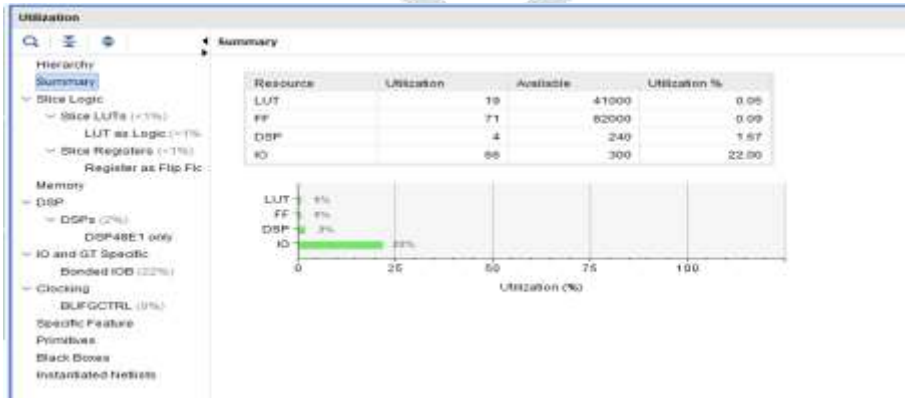

Figure 6: Area of the proposed method

In terms of power, the proposed method shows in fig.7 that improvements as well. It consumes a total power of 35.263W, which is composed of 0.391W of static power and 34.873W of dynamic power. This represents an approximate 6% reduction in total power consumption compared to the existing method.

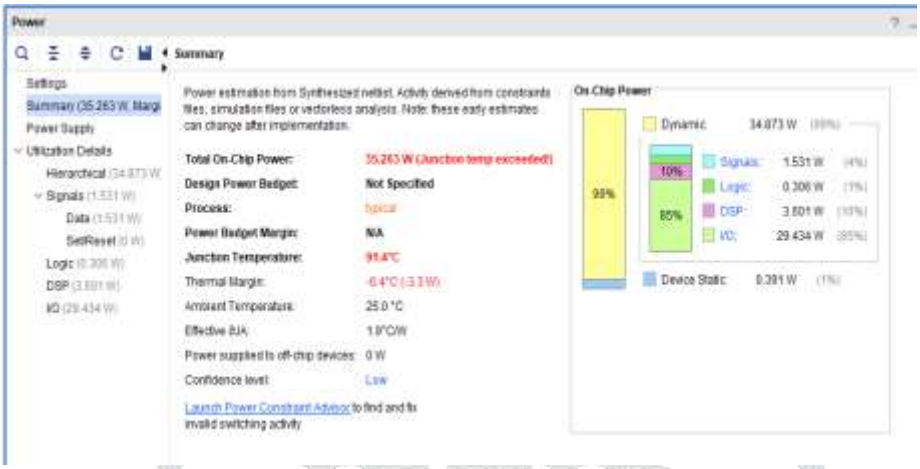

Figure 7: Power of proposed method

PERFORMANCE COMPARISION TABLE

S.No	Parameter	Existing method	Proposed method
1	Area (LUT)	113	19
2	Area(FLIPFLOPS)	152	71
3	Area(DSP CORES)	4	4
4	Static Power in Watts	0.444	0.391
5	Dynamic Power in Watts	37.041	34.873
6	Total Power in Watts	37.485	35.263

PERFORMANCE ANALYSIS

Fig. 8 presents a comprehensive performance comparison graph that encapsulates the key enhancements of the proposed method relative to the existing design. The graph visually highlights a dramatic reduction in area utilization—with the proposed method using only 19 LUTs and 71 flip-flops compared to 113 LUTs and 152 flip-flops in the existing approach—while maintaining the same number of DSP cores. Additionally, it clearly illustrates improvements in power efficiency, as both static and dynamic power consumption are lower in the proposed design, resulting in an overall power reduction of approximately 6%. This visual summary reinforces the effectiveness of the proposed architecture in achieving a compact, energy-efficient design suitable for next-generation 5G and beyond systems.

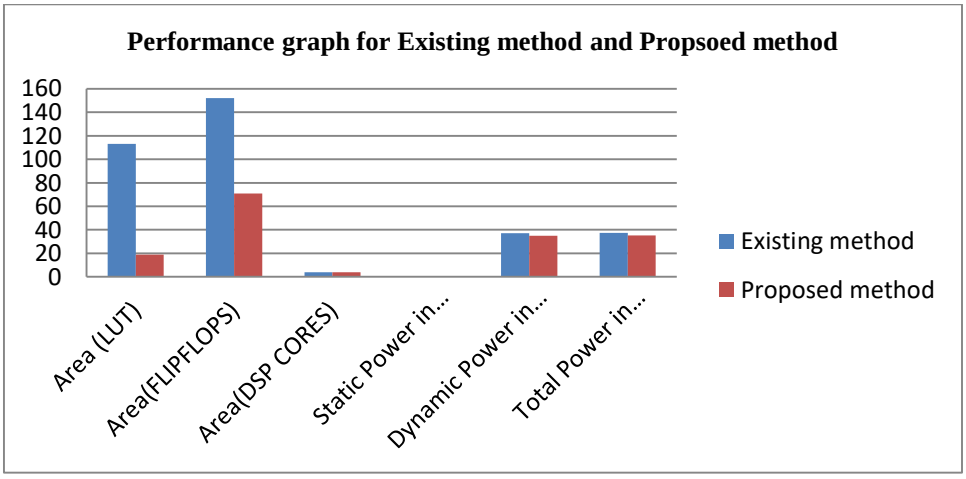

Figure 8: Comparison Performance Graph

VII. CONCLUSION

The proposed design of a digital multiplier using the Vedic the proposed reconfigurable multiband DSP hardware generator has demonstrated significant advancements in transmitter design for 5G and beyond. By integrating a dynamic reconfiguration logic with a multirate filter bank and carrier aggregation module, the architecture efficiently processes and aggregates wideband signals while reducing hardware area and power consumption. The experimental results obtained via Xilinx Vivado highlight notable

improvements over existing methods, with a reduction in LUTs (from 113 to 19) and flip-flops (from 152 to 71), as well as a 6% overall decrease in total power consumption. These enhancements confirm that the proposed method not only meets but exceeds current performance benchmarks, thereby providing a scalable and energy-efficient solution for modern wireless communication systems.

VIII. FUTURE SCOPE

In Further development of the dynamic reconfiguration logic to support a broader range of modulation schemes and adaptive algorithms, potentially incorporating machine learning techniques for real-time optimization.

IX. REFERENCES

1. J C. Base Station (BS) Radio, document TS 138 104, V15.14.0-5G, 3GPP, May 2019. [Online]. Available: https://www.etsi.org/deliver/ etsi_ts/138100_138199/138104/15.14.00_60/ts_138104v151400p.pdf
2. J. Mitola, “The software radio architecture,” IEEE Commun. Mag., vol. 33, no. 5, pp. 26–38, May 1995.
3. F. Harris, “Digital signal processing in radio receivers and transmitters,” Int. J. Wireless Inf. Netw., vol. 5, no. 2, pp. 133–145, 1998.
4. Synopsys. Arc HS44, HS46 and HS48 Processors. Accessed: Feb. 3, 2023. [Online]. Available: https://www.synopsys.com/dw/ipdir. php?ds=arc-HS44-HS46-HS48
5. S.-C. Lin, K. Chuang, C.-W. Chang, and J.-H. Chen, “Efficient interpolation method for wireless communications and signal processing applications,” IEEE Trans. Microw. Theory Techn., vol. 69, no. 5, pp. 2753–2761, May 2021.
6. R. Levinger, E. Shumaker, R. Banin, A. Ravi, and O. Degani, “The rise of the digital RFIC era: An overview of past and present digital RFIC advancements,” IEEE Microw. Mag., vol. 23, no. 12, pp. 71–85, Dec. 2022.
7. R. B. Staszewski, “Digitally intensive wireless transceivers,” IEEE Design Test Comput., vol. 29, no. 6, pp. 7–18, Dec. 2012.
8. H. V. H. Holma and P. Mogensen, “Extreme massive MIMO for macro cell capacity boost in 5G-advanced and 6G,” Nokia Bell Labs., Espoo, Finland, White Paper CID210786, 2023. [Online]. Available: https://onestore.nokia.com/asset/210786
9. V. Giannini, M. Ingels, T. Sano, B. Debaillie, J. Borremans, and J. Craninckx, “A multiband LTE SAW-less modulator with −160dBc/Hz RX-band noise in 40 nm LP CMOS,” in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 2011, pp. 374–376.
10. M. Ingels, Y. Furuta, X. Zhang, S. Cha, and J. Craninckx, “A multiband 40 nm CMOS LTE saw-less modulator with −60dbc C-IM3,” in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 2013, pp. 338–339.
11. V. Bhagavatula et al., “A SAW-less reconfigurable multimode transmitter with a voltage-mode harmonic-reject mixer in 14 nm FinFET CMOS,” in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 2017, pp. 220–221.
12. R. Bhat and H. Krishnaswamy, “Design tradeoffs and predistortion of digital Cartesian RF-power-DAC transmitters,” IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 63, no. 11, pp. 1039–1043, Nov. 2016.
13. W. Gerhard and R. H. Knoechel, “LINC digital component separator for single and multicarrier W-CDMA signals,” IEEE Trans. Microw. Theory Techn., vol. 53, no. 1, pp. 274–282, Jan. 2005.
14. R. B. Staszewski et al., “All-digital PLL and transmitter for mobile phones,” IEEE J. Solid-State Circuits, vol. 40, no. 12, pp. 2469–2482, Dec. 2005.
15. Z. Boos et al., “A fully digital multimode polar transmitter employing 17b RF DAC in 3G mode,” in Proc. IEEE Int. Solid-State Circuits Conf., Feb. 2011, pp. 376–378.