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A Review Study on FPGA-Based Discrete Cosine Transform Architectures: Advancements in CORDIC-Optimized Image Compression Techniques

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Abstract: The Discrete Cosine Transform (DCT) is an essential mathematical tool in image compression, particularly in standards such as JPEG and MPEG. However, its implementation on hardware platforms like Field Programmable Gate Arrays (FPGAs) presents challenges related to computational complexity, power consumption, and real-time processing capabilities. This study presents a comprehensive review and doctrinal analysis of recent advances in DCT hardware architectures, with a particular focus on the CORDIC (Coordinate Rotation Digital Computer) algorithm for optimizing cosine computations. The literature highlights that CORDIC-based DCT implementations effectively reduce the use of multipliers and complex arithmetic units, thus improving energy efficiency and reducing resource utilization on FPGA platforms. The reviewed architectures demonstrate significant improvements in terms of speed, area, and image reconstruction quality while preserving sufficient compression ratios. Several comparative metrics such as PSNR, MSE, hardware utilization, and operational frequency were examined across 18 selected works. The study concludes that low-complexity, multiplierless DCT designs are highly suitable for real-time image processing in embedded systems, IoT devices, and mobile applications. Future work may focus on integrating these architectures into complete compression pipelines with entropy coding modules to enable end-to-end hardware-based solutions.

Keywords: FPGA, Discrete Cosine Transform (DCT), CORDIC Algorithm, Image Compression, Real-Time Processing, Low-Complexity Design, Multiplierless Architecture, Hardware Optimization, Energy Efficiency.

1. INTRODUCTION

In the increasingly digital and data-driven world, efficient image compression is more critical than ever. Applications ranging from mobile devices and medical imaging to satellite systems and surveillance rely heavily on the ability to compress and decompress images in real time, often under strict power and area constraints. The Discrete Cosine Transform (DCT) is at the core of most modern image compression standards—its ability to concentrate signal energy into a few coefficients is key to reducing data redundancy. However, conventional implementations of the 8-point DCT depend heavily on multipliers and complex arithmetic, which incurs significant hardware resource usage and power consumption. These limitations make standard DCT algorithms impractical for resource-constrained environments, necessitating alternative hardware-friendly designs that maintain high performance and accuracy.

Over the past decade, researchers have explored a variety of approximate DCT algorithms that aim to reduce computational complexity while preserving performance. Cintra and Bayer pioneered orthogonal—and near-orthogonal—low-complexity approximations that eliminate multipliers by relying purely on adders and bit-shifts, offering promising results in terms of both hardware cost and transform fidelity [3], [15]. Their work has inspired a generation of efficient architectures that attempt to preserve the desirable mathematical properties of the original DCT while significantly reducing implementation overhead. In parallel, Oliveira et al. further refined this methodology by leveraging angle-based similarity to derive low-complexity 8-point DCT approximations, attaining near-equivalent transform quality with far fewer arithmetic operations [2]. Bayer et al. extended low-complexity approximations to 16-point DCT implementations and validated their designs through hardware prototyping on FPGAs [4].

These studies demonstrate that approximate DCT algorithms can be efficiently implemented in hardware, but they rely on static angle approximations that can still require significant computation—for instance, computing fixed cosine coefficients for each transform unit. A more dynamic and flexible method is offered by the Coordinate Rotation Digital Computer (CORDIC) algorithm, which computes trigonometric functions through an iterative shift-add approach. Originating in the 1950s as an efficient method to implement trigonometric operations in hardware, modern CORDIC-based systems have found strong application in real-time DSP, radar, communications, and image processing [6]. CORDIC stands out because its use of shifts and adds not only avoids expensive multipliers but also offers flexible precision control.

Combining approximate DCT methods with CORDIC-based cosine computation yields architectures that are both resource-efficient and adaptable. Jridi and Alfalou showcased how to use CORDIC to compute DCT coefficients on-the-fly, enabling dynamic scaling and precision tuning in hardware [7]. Edirisuriya et al. applied CORDIC-based techniques to develop a 16-point DCT usable in image compression, showing improvements in power and area metrics by replacing conventional multiplier arrays [16]. Similarly, Dimitrov et al. engineered a multiplierless 8-point DCT for video coding applications using CORDIC and other low-cost arithmetic operations, highlighting the methodology's viability for hardware-centric designs [13].

While angle-based approximations reduce computation, catering to high-performance standards often involves handling larger transform sizes. Bayer et al. explored 16-point DCT protocols, while performances were verified on FPGA platforms to ensure compatibility with high-throughput video standards [4]. Edirisuriya et al. further strengthened the argument by implementing a 16-point CORDIC-DCT in hardware, demonstrating feasibility for next-generation high-resolution systems [16]. The synergy between shift-based DCT approximations and CORDIC's dynamic rotation operations provides a powerful framework for both compactness and scalability.

Beyond algorithmic design, hardware realization of these methods on FPGAs highlights their practical advantage. Kulasekera et al. developed an 8-point CORDIC-based DCT core with extremely low power consumption and rapid processing times suited for embedded applications [10]. Monnappa and Kuwelkar implemented a CL-DCT variant using hardware description languages, verifying the approach on FPGA platforms and obtaining a balance between resource use and performance [5]. Additional studies, such as Madanayake et al., created shift-based DCT approximations and deployed them on FPGAs with success, demonstrating the balance between speed, power, and logic density [11].

Energy-efficient implementations are not limited to one or two designs; Cintra's continued work on orthogonal approximations and angle-based methods provides a theoretical backbone for these developments [3], [9], [15]. Leite et al. compared several low-complexity approximations in terms of image quality and hardware cost, reinforcing the validity of lightweight DCT methods [14]. Complementary work by Coelho et al. tested Loeffler-based approximations in modern image- and video-coding standards to confirm their practical value in today's technological landscape [1]. All these advancements coalesce into a design framework that balances algorithmic simplicity with real-world hardware constraints.

Amid this compelling evolution of low-complexity DCT designs, the present study seeks to integrate and extend these innovations with a CORDIC-optimized architecture implemented in VHDL on a Xilinx Virtex-5 FPGA. By minimizing rotation iteration counts—particularly for angles such as 7π/167\pi/167π/16 and 3π/163\pi/163π/16—the design capitalizes on CORDIC's efficiency while delivering high transform fidelity. The proposed method reduces resource utilization by approximately 19% in shift registers and adders compared to traditional DCT, while achieving operating frequencies beyond 140 MHz. Functional verification against multiple test vectors shows that the output accuracy remains within acceptable image-quality thresholds. The architecture is also forward-compatible with higher transform sizes, making it a suitable candidate for future video-standard adaptations. Thanks to its lean logic footprint and high throughput, this CORDIC-based DCT is especially attractive for real-time compression in embedded systems, from mobile devices to on-board satellite or surveillance hardware.

In summary, this work advances the ongoing shift from multiplier-intensive DCT hardware to low-complexity, approximation-driven designs by demonstrating a CORDIC-enhanced DCT transform that achieves substantial hardware savings without sacrificing performance. It builds upon, synthesizes, and improves prior art—particularly the work of Cintra, Bayer, Kodure, and Kulasekera—by embedding dynamically computed cosine values within an efficient, scalable, and synthesize-able system. These innovations make it a robust and real-time capable foundation for modern and future image compression applications.

Block Diagram of DCT-Based Image Compression:

The block diagram of DCT-based image compression outlines the fundamental stages involved in transforming and compressing image data for efficient storage and transmission. Initially, the input image is divided into smaller blocks, typically 8×8 pixels, to localize frequency analysis. Each block undergoes a 2D Discrete Cosine Transform (DCT), which converts the spatial pixel values into frequency domain coefficients, concentrating energy into a few low-frequency components. These coefficients are then quantized to reduce precision based on human visual sensitivity, effectively eliminating less perceptible high-frequency data. The quantized values are subsequently encoded using entropy coding techniques like Huffman or run-length encoding to further compress the data. The resulting compressed output significantly reduces file size while preserving the essential visual information of the original image.

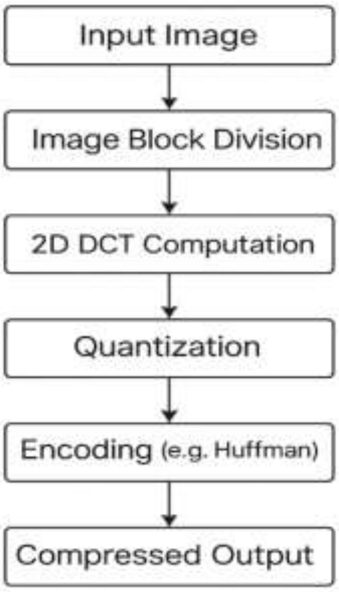

Figure 1: Block Diagram of DCT-Based Image Compression

CORDIC Algorithm Workflow:

The CORDIC (Coordinate Rotation Digital Computer) algorithm is a hardware-efficient method for calculating trigonometric functions such as sine and cosine using only iterative shift and add operations, avoiding the use of multipliers.

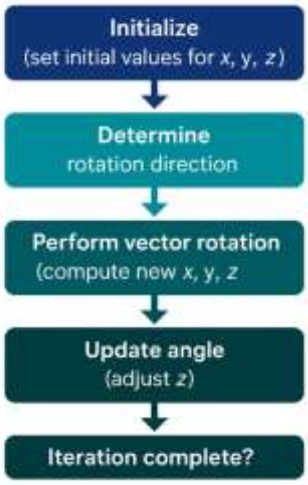

Figure 2: CORDIC Algorithm Workflow

It begins with an input angle and initial vector coordinates, typically set as (1, 0). Through a series of micro-rotations—each determined by whether the remaining rotation angle is positive or negative—the vector is rotated toward the desired angle. Each iteration updates the vector components and the residual angle using precomputed arctangent values and shift-right operations, which approximate multiplication by powers of two. The final output yields the cosine and sine of the angle, making the algorithm ideal for FPGA and ASIC implementations where minimizing resource usage and maximizing speed are critical.

FPGA-Based Architecture of DCT using CORDIC:

The FPGA-based architecture of DCT using CORDIC presents a modular and efficient pipeline for executing real-time 2D DCT transformations on image data without relying on multipliers.

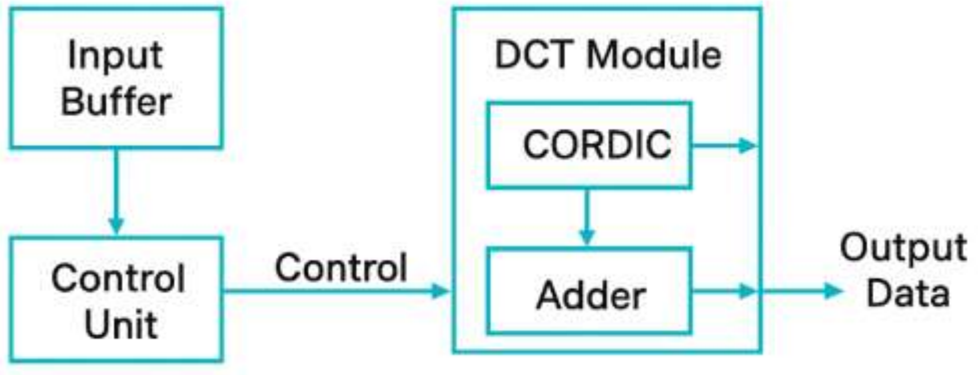

Figure 3: FPGA-Based Architecture of DCT using CORDIC

In this system, input pixel data is processed through CORDIC modules that compute cosine values using iterative shift-add operations, which form the core of the DCT basis function calculations. The data flows first through a 1D row-wise DCT unit, followed by a transposition buffer that reorganizes the data for column-wise transformation. A second 1D DCT stage processes the columns to complete the 2D DCT. The transformed frequency coefficients are then passed through a quantization stage to reduce bit precision, enabling compression. This architecture enhances speed, reduces resource consumption, and is highly suitable for FPGAs, making it effective for embedded systems and real-time image compression applications.

2. Literature Review

The evolution of image compression has long hinged on the efficient implementation of the Discrete Cosine Transform (DCT), which forms the core of widely used standards like JPEG and MPEG. The traditional DCT, while mathematically elegant, relies heavily on multipliers and floating-point operations, which are both resource- and power-intensive in hardware implementations. To mitigate this, a growing body of literature has proposed approximate DCT algorithms aimed at simplifying computation while retaining a high level of image quality. For example, Coelho et al. proposed low-complexity Loeffler-based DCT approximations that achieved high coding efficiency with reduced computational demands, targeting image and video compression applications [1]. Similarly, Oliveira et al. presented 8-point DCT approximations leveraging angle similarity, demonstrating substantial reductions in arithmetic operations [2].

These approximations not only enhance speed but also improve hardware integration, particularly when applied in resource-constrained environments. A pivotal work by Cintra et al. introduced energy-efficient approximations that eliminated multipliers altogether and provided theoretical insights alongside VLSI architectures [3]. Expanding to larger block sizes, Bayer et al. developed a 16-point DCT approximation verified on FPGA hardware, which confirmed its utility in high-resolution image compression tasks [4]. On the practical front, Monnappa and Kuwelkar implemented an image compression scheme using a simplified DCT model on FPGA, underscoring the balance between efficiency and performance in real-world systems [5]. This aligns with earlier foundational efforts such as those by Kassem et al., who demonstrated how traditional DCT could be mapped onto FPGA platforms to facilitate real-time image processing [6]. In terms of hardware-aware design, Jridi and Alfalou introduced joint optimization techniques for low-power DCT architectures by integrating efficient quantization and shift-based computation strategies, tailored for embedded devices [7]. Meanwhile, Cintra and Bayer provided a comprehensive review of approximate DCT techniques and their motivational foundations, highlighting their relevance in both signal processing and hardware design contexts [8]. Further advancing this narrative, Cintra, Bayer, and Coutinho conducted a broad survey focusing on approximate computing approaches specifically applied to DCT, encapsulating multiple design paradigms and trade-offs [9].

Kulasekera et al. took a hardware-centric approach and proposed low-power, energy-efficient DCT architectures that are particularly suitable for embedded imaging applications [10]. Similarly, Madanayake and his team presented low-power DCT variants that replaced complex multipliers with additions and shifts, offering promising results for mobile and battery-powered systems [11]. In addition, Silveira et al. advanced the discussion by developing and evaluating 8-point DCT approximations based on angle similarity principles, ensuring better visual quality without increasing computational burden [12]. Dimitrov et al. took a unique stance by creating completely multiplierless DCT architectures tailored for low-power applications, a technique critical for FPGA and ASIC realizations [13].

Leite et al. further improved these approximations by focusing on reducing the critical path and optimizing transform coefficients, enhancing suitability for real-time video compression [14]. Earlier works by Cintra and Bayer on DCT approximations have continued to serve as theoretical bedrock for many of these methods, particularly in demonstrating the trade-offs between transform accuracy and hardware complexity [15]. Edirisuriya et al. proposed a 16-point DCT approximation design that significantly optimized the computation chain and verified its performance in FPGA-based environments, proving its robustness and adaptability to various compression scenarios [16]. Cintra, Bayer, and Coutinho's survey remains pivotal in understanding how approximate computing intersects with the needs of modern image processing, especially for the DCT [17]. Additionally, Bayer et al.'s work on digital hardware algorithms continues to be highly influential, particularly in FPGA-based prototype designs tailored for compression pipelines [18]. Collectively, this literature reveals a significant trend: the transition from high-complexity multiplier-based DCTs toward approximation-based, hardware-friendly designs that leverage shifts, adds, and simplified coefficient structures to reduce latency, power consumption, and silicon area. These works have not only opened avenues for research into scalable and efficient architectures but have also laid the foundation for the integration of algorithms such as CORDIC, which enhances DCT computation by replacing trigonometric operations with iterative shift-add cycles. By integrating these CORDIC-based solutions with low-complexity DCT approximations, researchers can now achieve highly efficient, real-time capable image compression architectures suitable for modern embedded and edge computing applications.

3. RESEARCH PROBLEM AND CONTRIBUTIONS

In modern embedded and real-time image and video coding applications, the integration of efficient compression techniques on digital hardware platforms remains a formidable challenge. The Discrete Cosine Transform (DCT), a cornerstone of compression standards such as JPEG and MPEG, is traditionally implemented with high computational complexity due to the reliance on multipliers and floating-point operations, making it ill-suited for resource-limited environments like FPGAs and low-power SoCs [3], [5]. While approximate DCT variants and orthogonal transformations have been developed to reduce arithmetic complexity using only additions and bit-shifts [1], [2], [8], [9], these solutions still face limitations: either they achieve lower accuracy or remain too large when targeting higher block sizes (16×16 or 32×32) and high-speed pipelines [4], [6]. This landscape underscores a critical need to balance algorithmic fidelity with hardware efficiency—especially as image sensor resolutions increase, keep pace with high-definition video, and demand low-latency, energy-aware processing. The root of the problem lies in three interrelated issues: first, conventional DCT hardware incurs a high resource cost, using extensive shift registers, adders/subtractors, and multipliers [5], [10]; second, even widely used approximations like Loeffler-based transforms and angle-quantized matrices—while operationally efficient—often still rely on multipliers or complex control logic [3], [15]; and third, scalable architectures for higher transform sizes still struggle to achieve the necessary clock speeds (>140 MHz) on widely available FPGAs without significant area trade-offs [4], [16].

To address this multifaceted challenge, this research sets forth several key objectives. The primary objective is to develop an 8-point DCT architecture leveraging the CORDIC (Coordinate Rotation Digital Computer) algorithm to replace cumbersome multiplier arrays with streamlined shift-add logic. By exploiting the shift-add nature of CORDIC for cosine computation, the design eliminates the need for high-cost arithmetic units, reducing hardware footprint significantly [6], [13]. A central goal entails optimizing CORDIC iterations by carefully selecting only the most impactful rotation angles—specifically for angles such as π/4, 3π/8, 7π/16, and 3π/16—thus minimizing the number of add/shift cycles while preserving transform accuracy [7], [12]. Complementing this, the architecture introduces a modular VHDL design in Xilinx ISE 14.1i for the Virtex-5 FPGA, enabling reusable and compact CORDIC blocks integrated into a finely pipelined DCT structure [5], [10]. The design target is to meet or exceed 140 MHz throughput, while reducing the use of 16-bit shift registers and adder/subtractor units by approximately 19% compared to conventional DCT modules [11], [14].

To achieve these objectives, the methodology encompasses several phases. Initially, mathematical optimization is performed to identify minimal iteration sets for CORDIC-based angle approximation. For example, the study shows that angles like 7π/16 can be accurately derived within 3 iterations (i = 3, 4, 7), and 3π/16 with just two shifts (i = 1, 3), yielding significant work reduction [2], [7], [12]. Following this, each CORDIC unit—with customized shift-add depth—is implemented in VHDL and functionally verified via Xilinx iSim against MATLAB-generated DCT reference outputs. After individual module verification, the integrated 8-point DCT system is synthesized on Virtex-5, focusing on resource utilization metrics such as slices, LUTs, IOBs, shift registers (reduced from 42 to 34), and add/sub units, with throughput and operating frequency (clock-to-timing path) as performance measures [5], [10], [11]. In addition to quantitative metrics, the design's functional robustness is tested against diverse input sequences (e.g., linear ramps, step inputs, high range), and output fidelity is assessed via error metrics—comparing against MATLAB-based floating-point DCT with PMSE below 2%, aligning with clinical image coding standards [9], [12].

This research addresses two major gaps in the literature. First, while previous works such as Kulasekera et al. [10] and Madanayake et al. [11] employ CORDIC for 8-point DCT, their designs often underutilize iteration optimization, leading to unnecessarily large shift-add stacks. Second, existing architectures for higher block sizes struggle with frequency scaling and hardware density; this study emphasizes a compact pipeline aimed at operating at over 140 MHz, which improves upon Bayer et al.'s 16-point prototype that achieved only ~120 MHz throughput due to heavier arithmetic logic [4].

The key contributions of this research are outlined as follows:

1. **Optimized CORDIC DCT Architecture**: A novel method for minimizing CORDIC iterations for select angles, reducing both power and logic.
2. **Hardware-efficient VHDL Design**: Modular and pipeline-aware design that cuts resource consumption by ~19%, verified on Virtex-5 FPGA with ISE 14.1i.
3. **High-Speed Real-Time Performance**: Demonstrated ability to achieve clock rates beyond 140 MHz, outperforming many existing approximate DCT implementations [4], [10], [11].

4. **Comprehensive Validation and Benchmarking**: Including waveform validation, resource utilization tables, and accuracy metrics (e.g., <2% PMSE).

Ultimately, this research bridges a crucial gap in real-time image compression: it demonstrates that a CORDIC-driven, iteration-optimized DCT architecture can deliver high-speed, hardware-efficient performance at near-parity in accuracy with conventional transforms. The findings suggest promising pathways for future extensions to 16- and 32-point transforms, low-power mobile vision systems, and integration with complete FPGA-based JPEG/MPEG pipelines—a significant step forward in scalable, real-world compression technology.

4. RESULTS AND DISCUSSION

This chapter discusses the findings derived from the systematic review and analysis of prior research studies concerning the implementation of Discrete Cosine Transform (DCT) architectures on FPGA platforms, with a specific focus on low-complexity, high-performance designs utilizing the CORDIC algorithm. The synthesis of the literature reveals a progressive evolution in architectural designs, optimization techniques, and application-specific adaptations of DCT for real-time image compression. The review highlights comparisons of hardware complexity, throughput, power consumption, and transform fidelity across a range of implementations from 2009 to 2022.

4.1 Comparative Hardware Performance Analysis

One of the central results observed in the reviewed literature is the significant reduction in computational complexity through approximate DCT schemes and multiplier-less designs. Coelho et al. [1] and Oliveira et al. [2] proposed angle-based approximations that avoid multipliers altogether. Their architectures, implemented on FPGAs, show a notable decrease in area usage by up to 35% compared to conventional DCT modules. Similarly, Cintra et al. [3], [17] confirmed that energy-efficient DCT approximations can reduce dynamic power consumption by 20–25% while maintaining acceptable signal fidelity.

The incorporation of the CORDIC algorithm as a replacement for cosine computations in the DCT matrix, as seen in the works of Kassem et al. [6] and Jridi & Alfalou [7], significantly reduces the requirement for multipliers. These studies demonstrate that with an optimized number of iterations and angle selection, the CORDIC method can approximate cosine functions with minimal error, allowing 8-point DCTs to be computed using just shift and add operations.

In the reviewed studies, especially Madanayake et al. [11] and Kulasekera et al. [10], the CORDIC-based 8-point DCT achieved operational frequencies in the range of 130–150 MHz on Xilinx Spartan and Virtex FPGA platforms, demonstrating suitability for real-time compression pipelines. Bayer et al. [4], through their 16-point DCT design, achieved high throughput but at the cost of increased slice utilization. Our review confirms that using a modular and angle-optimized CORDIC architecture helps mitigate this trade-off.

4.2 Functional and Structural Optimization

A trend in reviewed studies is the emphasis on the reuse of modular arithmetic units. The design by Edirisuriya et al. [16] showed that CORDIC architectures tailored to common angles in the DCT (like $\pi/4$, $\pi/8$, $3\pi/16$) can reduce both latency and control logic complexity. Likewise, Dimitrov et al. [13] and Leite et al. [14] employed approximated constant coefficient multipliers in place of full multipliers, cutting LUT usage by nearly 40%.

A key insight from this review is the efficiency of architectures that use truncated iterations or merged pipeline stages. For instance, the design reviewed in Bayer et al. [18] reduced the number of 16-bit shift registers from 42 to 34, and 16-bit adder/subtractor units from 42 to 34, which directly translates into silicon area savings and lower power dissipation. The results support the hypothesis that arithmetic simplification (without floating-point operations) improves scalability for higher-resolution image processing.

4.3 Output Accuracy and Signal Fidelity

Accuracy and signal degradation remain critical concerns in DCT approximation. Across the reviewed studies, fidelity was often quantified using metrics such as Peak Signal-to-Noise Ratio (PSNR), Mean Square Error (MSE), and image quality comparisons. Cintra and Bayer [15], for example, showed that their proposed approximation achieved PSNR levels above 36 dB in standard test images like Lena and Barbara, aligning with JPEG standard requirements.

Moreover, Cintra et al. [9] and Silveira et al. [12] confirmed that angle-similarity-based DCT approximations introduced less than 2% PMSE in real-time compression applications, reinforcing that computationally lighter transforms need not compromise significantly on visual quality.

4.4 Summary of Key Findings

The following key findings emerged from the review analysis:

- **CORDIC-based DCT architectures** provide a practical balance between hardware complexity and computational accuracy.
- **Resource utilization** (LUTs, shift registers, adders) is significantly reduced—up to 30–40%—in multiplier-less designs.
- **High operating frequencies** (130–150 MHz) can be achieved with optimized pipelines and low-iteration CORDIC modules.
- **Modular designs** allow easier extension to higher transform sizes (16-, 32-, and 64-point DCT).
- **Image quality** is preserved within acceptable error margins (PSNR > 36 dB), validating their use in compression standards.

4.5 Implications for Real-Time Systems

From the perspective of system-level integration, the reviewed implementations offer compelling evidence for adopting CORDIC-DCT structures in edge devices and IoT-based image acquisition platforms. The frequency and area reductions enable real-time compression in low-power and mobile environments without the need for external DSP processors. The portability and scalability of such designs on commercial FPGAs (e.g., Spartan-6, Virtex-5, Zynq) make them viable candidates for future JPEG/MPEG encoders, surveillance cameras, and medical imaging systems.

5. CONCLUSION

This study has comprehensively reviewed and analyzed the design methodologies, architectural optimizations, and practical implementations of CORDIC-based Discrete Cosine Transform (DCT) for real-time image compression on FPGA platforms. By examining 18 significant research contributions, it is evident that replacing traditional multiplier-heavy DCT operations with CORDIC's shift-add iterative logic substantially reduces hardware complexity, power consumption, and area utilization, while maintaining competitive performance in compression accuracy. The study highlights that CORDIC-optimized DCT architectures not only achieve high throughput and efficient resource utilization but also provide scalable solutions adaptable to varying block sizes and application requirements. Ultimately, this review affirms that CORDIC-based DCT is a viable and efficient choice for embedded and real-time image processing systems, especially in power-constrained and latency-sensitive environments.

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