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DESIGN OF SAR ADC FOR GROUND PENETRATING RADAR APPLICATIONS

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Abstract: Analog-to-digital converters (ADCs) are a critical interface in modern sensor-centric electronic systems, playing an essential role in accurately digitizing analog signals for high-speed data processing. Ground Penetrating Radar (GPR) applications demand ADCs with high resolution, moderate to high sampling rates, and robust resilience to noise and environmental variations. This project presents the design and top-down behavioral modeling of a 12-bit, 40 MSPS Successive Approximation Register (SAR) ADC targeting GPR systems using SCL 180nm CMOS technology. The methodology adopts a modular design flow, beginning with architecture selection and the comparative study of various SAR sub-circuits—capacitive DACs, dynamic comparators, and sample-and-hold circuits—to optimize for power, area, and signal integrity. Behavioral modeling of each functional block is accomplished through Verilog-A, enabling rapid prototyping and architecture validation prior to transistor-level implementation. This approach overcomes common challenges in direct schematic-level design by facilitating early design space exploration and functional verification. The proposed ADC architecture aims to achieve high performance and energy efficiency suitable for demanding GPR sensor applications.

IndexTerms **- Ground Penetrating Radar (GPR), SAR, C-DAC, Resolution**

I. INTRODUCTION

An **Analog to Digital Converter (ADC)** is a type of device which helps us to process the chaotic real-world data in a digital standpoint. ADCs are fundamental building blocks in modern electronic systems, bridging the analog real world with the digital realm where processing, storage, and analysis are performed. Real-world data, such as sound, light, temperature, or electromagnetic signals, typically exist in continuous analog form. However, most modern devices— including computers, smartphones, and embedded systems— operate digitally. To use these signals, an accurate and efficient conversion from analog to digital is essential. ADCs perform this crucial role by sampling the continuous input signal, quantizing it into discrete levels, and encoding the result into digital binary values for further processing. Since their inception, ADC technologies have evolved remarkably to meet diverse application needs spanning speed, power, accuracy, and cost. Early ADC architectures included flash ADCs offering very high speed but limited resolution, and dual-slope ADCs with high accuracy but slower conversion times. Among the various architectures developed, the **Successive Approximation Register (SAR)** ADC has gained prominence for applications requiring a balanced trade-off between resolution, speed, and power consumption. SAR ADCs typically offer resolutions from 8 - 18 bits with moderate sampling rates in the range of several tens of mega samples per second, making them ideal for medium-to-high resolution use cases.

The operational principle of a SAR ADC is based on a binary search algorithm that iteratively approximates the input voltage by comparing it against a generated reference voltage. This process involves key components: a sample-and-hold circuit that stabilizes the input during conversion, a comparator that compares the input with the digital-to-analog converter output, a capacitive DAC that creates the reference voltages, and the SAR logic that controls the iterative binary search and records the result. The simplicity of the SAR architecture, coupled with its moderate speed and energy efficiency, enables its extensive use in battery-powered portable devices, industrial instrumentation, medical imaging systems, and communication electronics. Advancements in low-power design techniques, capacitor DAC architectures, and high-speed comparator designs have further enhanced SAR ADC performance, consolidating its position as an excellent choice for sensor interfaces and embedded systems needing precision without excessive power consumption or area overhead.

Ground Penetrating Radar (GPR) is a widely used, non-destructive geophysical technique designed to image subsurface structures and detect buried objects by transmitting electromagnetic pulses into the ground and analyzing the reflected signals. GPR finds applications in civil engineering, archaeology, environmental studies, and utility detection. The core principle relies on sending short high frequency electromagnetic pulses—typically from tens of MHz to several GHz—into the earth, where these pulses propagate and reflect off interfaces characterized by changes in dielectric properties such as soil layers, rocks, pipes, and voids. The GPR system consists of several critical components: the transmitter antenna which emits the electromagnetic pulses, the receiver antenna that collects the reflected signals, signal conditioning and amplification circuitry, an analog-to-digital converter

(ADC), and finally digital signal processing units that generate interpretable subsurface images. In this chain, the ADC plays a pivotal role by converting the constantly received analog reflections into precise digital data with high speed and resolution. The fidelity of this conversion directly influences the quality of the subsurface image and detection accuracy. High resolution ensures subtle variations in signal amplitude are captured, allowing better differentiation of closely spaced or weak reflections, while sufficient sampling speed permits real-time data acquisition and higher spatial resolution.

Selecting an ADC for GPR applications involves balancing numerous factors: resolution must be high enough (commonly 10 bits or more) to distinguish fine signal changes; sampling speed must support the desired depth resolution and real-time scanning (typically in the tens of MSPS), power consumption should be low for portable deployments and noise performance must preserve signal integrity despite environmental electromagnetic interference.

Among ADC architectures, the SAR ADC is particularly suitable for GPR due to its advantageous characteristics: it offers the necessary resolution and moderate speed while maintaining a low power profile and relatively simple architecture. These enable efficient digitization of radar echoes without excessively increasing system complexity or power budgets, which is crucial for field-usable GPR units. GPR systems require ADCs with high resolution and robustness. The SAR ADC plays a critical role in the GPR system by digitizing the reflected analog signals with high accuracy and speed.

The challenge in designing SAR ADCs tailored for GPR involves meeting application-specific performance criteria, including managing process variations, optimizing speed resolution trade-offs, minimizing power, and ensuring reliability under varying environmental conditions. GPR systems often require robust, high-performance ADCs that can operate in harsh environmental conditions, making the design of such an ADC a significant innovation in the field. This project aims to address these challenges by employing a modular design using behavioral Verilog-A modeling for early validation and iterative optimization before transistor level design, thereby creating an ADC architecture that is effective for GPR's demanding requirements.

II. Related Works

Over the years, the field of analog-to-digital converters (ADCs) has witnessed tremendous growth and innovation. Many researchers and engineers across the globe have contributed their expertise to develop new architectures, optimize existing designs, and address key challenges in resolution, speed, power consumption, and noise performance. The continued evolution of ADC technology reflects its foundational importance in enabling modern electronic systems to precisely convert real world analog signals into digital data, powering everything from mobile gadgets to sophisticated medical and radar instruments. In particular, Successive Approximation Register (SAR) ADCs have gained widespread attention due to their balanced trade-offs, making them suitable for medium-to-high resolution applications at moderate speeds. This makes SAR ADCs a natural fit for specialized sensing technologies like Ground Penetrating Radar (GPR), where high accuracy and timely data capture are critical. The rich body of existing research explores various innovations—from novel DAC structures to improved comparator designs—that aim to enhance SAR ADC performance tailored to the rigorous demands of GPR systems. In the following sections, key contributions from this ongoing research will be reviewed to provide insight into the current state of the art and identify areas that this thesis seeks to advance.

Paper [3] proposed that a high-precision comparator design tailored for use in 12-bit SAR ADCs, implemented using 180 nm CMOS technology combines an open-loop differential input stage with cross coupled pairs to enhance gain and employs a regenerative latch with positive feedback to improve response speed. A novel biasing circuit utilizing an external resistor for fine-tuning compensates for process variations in the bias current, improving stability and performance. Simulated results show the comparator achieves a resolution of 0.4 mV, suitable for 12-bit accuracy, with a dynamic power consumption of approximately 1.8 mW at a 3.2 MHz sampling frequency. The design also incorporates buffering inverters at the output stage for signal stabilization and drive capability. Likewise, in [4], a successive-approximation-register (SAR) analog-to-digital converter (ADC) featuring a gain-boosting dynamic comparator design and a low-delay SAR logic was proposed. The proposed comparator incorporates positive feedback in the pre-amplifier, which enables high gain during the integration phase, thereby improving energy efficiency. Meanwhile, to ensure sufficient settling time for the internal capacitive digital-to-analog converter (CDAC), an asynchronous SAR logic with low logic delay in the SAR logic loop is implemented. Accordingly, a prototype ADC is manufactured using 28-nm CMOS technology, which achieves a power consumption of 860 μW at a 75 MHz sampling frequency.

In [7], a novel DAC structure was proposed where a 10-bit SAR ADC operating at 70 MSPS with an innovative split-array capacitive DAC structure was designed to reduce both total area and parasitic capacitance effects. Their design uses smaller unit capacitors within the sub-DAC, achieving a 15.87% reduction in total capacitance and a 46.87% reduction in sub-DAC parasitic capacitance relative to traditional split-array DACs. The architecture maintains a constant common-mode voltage during conversion, which reduces comparator offset variation and enhances linearity.

Deepika et.al [9], proposed a low-power 10-bit SAR ADC implemented in 180 nm CMOS technology for implantable pacemaker applications, featuring an integrated capacitive DAC (CDAC) on the MSB portion combined with a C-MOSCAP DAC on the LSB portion. This hybrid DAC structure effectively balances the stringent requirements of linearity and capacitive matching while reducing area and power consumption. incorporates a dual-path bootstrapped switch to enhance linearity and speed, alongside a triple tail comparator providing low noise and offset characteristics. The work in [12] spoke about a 13b 40MS/s SAR ADC with a robust kT/C noise cancellation technique, which cancels the kT/C noise by forming negative feedback with an auxiliary amplifier, thereby making the noisy node to virtual ground. After kT/C noise cancellation, an independent SAR operation is performed with a kT/C noise-free signal. Since the auxiliary amplifier is only used at the end of the sampling phase, a duty cycled amplifier is used, resulting in low power consumption. Shetty et.al [13] proposed a high-speed, 14-bit SAR ADC implemented in 90nm CMOS technology, achieving a sampling rate of 125 MS/s with low power consumption through innovative architectural features. The design employs a novel Dual-Split-Array-Three-Section (DSATS) capacitive DAC to significantly reduce DAC area by approximately 59.76% and switching energy by minimizing the total capacitance from 824 pF to 824 fF. Bootstrap switching techniques improve linearity and reduce power consumption further, while a preamplifier-latch based comparator with rapid comparator delay of 250 ps enhances conversion speed and precision.

The Successive Approximation Register (SAR) ADC is one of the most widely used ADC architectures, particularly for applications requiring moderate speed and high resolution. It operates based on a binary search algorithm. The process begins by

comparing the analog input to a reference voltage using a digital-to-analog converter (DAC) and a comparator. The SAR logic starts by setting the most significant bit and checks whether the resulting voltage is above or below the input. Based on the comparator's result, it either keeps the bit or clears it and proceeds to the next bit. This process continues until all bits are resolved, typically taking one clock cycle per bit. SAR ADCs are popular in systems like data acquisition units, battery-operated devices, and industrial sensors due to their relatively low power consumption, high resolution (up to 18 bits), and decent sampling speeds (from hundreds of kSPS up to tens of MSPS).

The Flash ADC is the fastest type of ADC architecture and is typically used where extremely high sampling speeds are required, such as in radar systems, oscilloscopes, and RF signal processing. It works by using a large number of comparators in parallel, specifically, for an n-bit ADC, $2^n - 1$ comparators are needed. Each comparator checks whether the input voltage is above a specific reference level, and the set of outputs forms a "thermometer code" that is then encoded into binary. Because all comparisons happen simultaneously, the conversion is extremely fast, often in the giga samples per second (GSPS) range. However, flash ADCs are limited in resolution (usually 4 to 8 bits) because the number of comparators increases exponentially with resolution, leading to high power consumption and large area on silicon. Despite these limitations, flash ADCs are indispensable in applications where speed is the top priority.

Pipeline ADCs strike a balance between the speed of flash ADCs and the resolution of SAR or sigma-delta ADCs. The architecture consists of multiple stages arranged in a pipeline, with each stage resolving a few bits of the input signal. After a stage resolves its bits, it subtracts the corresponding analog voltage (using a DAC) from the input and amplifies the residue before passing it to the next stage. This pipelined operation allows the ADC to convert multiple samples at once—while one stage processes the current sample, another can handle the next. Although this introduces latency of a few cycles, it greatly improves throughput. Pipeline ADCs are typically used in video processing, communications systems, and digital imaging where both speed and resolution (commonly 8–14 bits) are important. They consume moderate power and provide conversion rates in the range of tens to hundreds of MSPS.

Sigma-Delta ADCs are well known for their exceptional resolution and noise performance, particularly at lower sampling rates. The architecture relies on oversampling the input signal at a rate much higher than the Nyquist rate, followed by noise shaping through a feedback loop containing an integrator and a quantizer. The result is a stream of 1-bit data which, after being filtered and decimated by a digital filter, provides a high-resolution output. The key strength of sigma-delta ADCs is their ability to push quantization noise out of the band of interest, making them ideal for applications such as audio recording, biomedical instruments, and other precision measurement systems. However, due to the digital filtering and oversampling requirements, these ADCs tend to have higher latency and are not suitable for high-speed applications.

The Dual Slope ADC is a type of integrating ADC known for its accuracy and noise immunity rather than speed. It works in two phases: during the integration phase, the input voltage is applied to an integrator for a fixed time, allowing the integrator output to ramp up; during the de-integration phase, a reference voltage of opposite polarity is applied and the time it takes to return the integrator output to zero is measured. This time is proportional to the input voltage. Since this architecture averages the input over time, it is inherently immune to noise and power supply fluctuations, making it a good choice for applications like digital multimeters and other slow, precision instruments. However, the method is quite slow and unsuitable for high-speed data acquisition.

Time-based ADCs are relatively modern and operate by converting an analog input into a time interval or frequency, which is then measured digitally. One common approach is to use a Voltage Controlled Oscillator (VCO) where the frequency of oscillation varies with the input voltage. By measuring the number of cycles within a fixed time window or measuring the time taken for a specific number of cycles, the ADC converts the input voltage into a digital code. These ADCs are particularly attractive in advanced CMOS technologies, where scaling of voltage and power is important. They offer potential advantages in terms of integration, power efficiency, and scalability but can suffer from nonlinearity and require careful calibration. They are increasingly being explored in low-power and IoT applications.

Table 1: Comparison of types of ADCs

ADC Type	Speed	Resolution		Power		Best For
Flash	Very High	Low		High		RF, Radar
SAR	Medium	High		Low		Data acquisition
Pipeline	High	High		Medium		Imaging, Video
Sigma Delta	Low-Medium	Very High		Medium		Audio, Precision
Dual Slope	Very Low	High		Very Low		Multimeters
Time Based	Varies	Varies		Very Low		Advanced CMOS

This review summarizes recent advancements in SAR ADC designs, emphasizing comparator and DAC architectures and evaluates their suitability for a 12-bit, 40 MSPS implementation in SCL 180nm CMOS. SAR ADCs operate on the principle of binary search

using a sample-and-hold circuit, a charge redistribution digital-to-analog converter (CDAC), a comparator, and SAR control logic. Each conversion begins by sampling the analog input onto the DAC, followed by N comparison cycles to resolve an N-bit digital output. The Verilog-A modelled architecture benefits from low power consumption, absence of operational amplifiers, and digital simplicity, which fits well with standard CMOS processes.

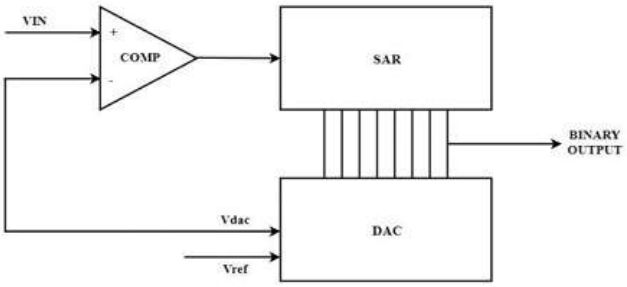

Figure 1. Block diagram of sar adc

III. OBEJCTIVES

- To design a 12-bit SAR ADC operating at 40 Msps.
- To analyze and identify suitable ADC architecture for Ground Penetrating Radar (GPR) application, based on their performance requirements and operational context.
- To design and implement transistor-level models of critical analog sub-blocks, including the comparator and SAR logic, verifying their performance in a standard 180nm CMOS process.
- To develop behavioral-level models for the DAC and sample and-hold circuits and performance validation.
- To measure and evaluate key performance metrics such as power consumption, speed, resolution, and functionality for individual sub-blocks—particularly the comparator and SAR logic—through comprehensive simulation.
- To adopt a modular design approach by developing and integrating individual SAR ADC components (comparator, DAC, SAR logic, sample-and-hold) as separate blocks to facilitate easier testing, debugging, and future upgrades.
- To establish a validated design and simulation flow that provides a robust foundation for subsequent research phases—such as power optimization and radiation-hardening techniques—which will be pursued in future work.

IV. PROPOSED WORK

One of the crucial components of an ADC is a comparator and its primary purpose is to compare two voltage levels and generate a logical output based on their relationship. Dynamic comparators have a significant advantage of being more power efficient than ordinary comparators. In this project, transistor level Strong-Arm latch comparator circuit is designed in 180nm CMOS technology in the Cadence tool. This architecture for a comparator is a crucial electronic circuit designed for high speed and precise comparison of two input signals. Its functional components include an input stage that receives signals for comparison, a Strong-Arm stage responsible for swiftly determining the larger input, a latch stage employing positive feedback to capture and maintain the comparison result and an output stage indicating the outcome. The strong-arm phase actively drives one input to hasten the comparison process, enhancing the response time. The strongarm latch comparator is a widely used dynamic comparator architecture in SAR ADCs due to its high speed, low offset, and zero static power consumption during operation. The schematic shown below represents the full transistor-level implementation of this comparator.

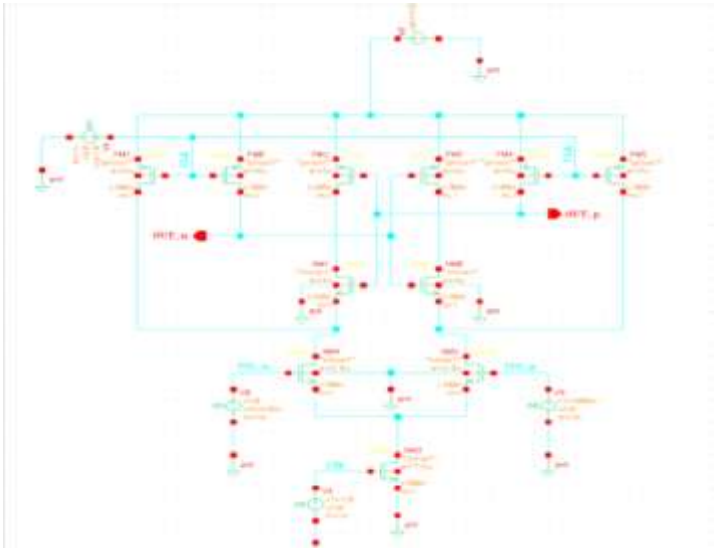

Figure 2. Strong arm latch comparator circuit

Another comparator was developed using Verilog-A behavioral modeling to capture its dynamic analog behavior while enabling faster simulation iterations compared to transistor level design alone. The model implements a three-stage amplifier architecture comprising a pre-amplifier, a high-gain stage, and a dynamic latch, reflecting typical SAR ADC comparator design. Key electrical parameters such as transconductance (gm), output resistance, gain, and load capacitance are explicitly parameterized to allow flexible tuning.

Noise effects are modeled comprehensively by including thermal noise, flicker noise, and kickback noise components, which impact comparator sensitivity and accuracy. Device mismatch and offset voltages are incorporated as model parameters to account for fabrication variations affecting comparator offset. The behavioral model simulates timing delays and output waveform transition characteristics, including propagation delays and rise/fall times, enhancing the realism of the comparison process. The latch operation is triggered by clock crossing events and accurately simulates regenerative behavior and rail-to-rail output switching.

Overall, this detailed Verilog-A comparator model strikes a balance between behavioral abstraction and physical realism, enabling efficient system-level design space exploration while capturing key analog phenomena necessary for SAR ADC performance assessment.

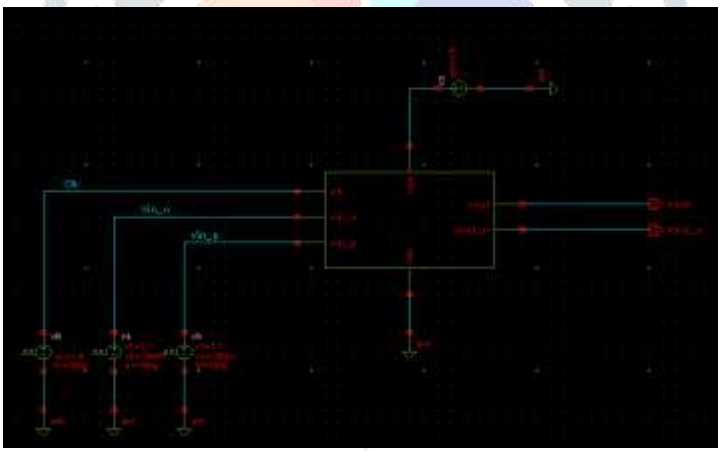

Figure 3. Behavioral modelled comparator

The objective is to design and simulate key building block of a SAR ADC, specifically focusing on the Sample-and-Hold (S/H) circuit and the clocked Comparator. The simulation is performed using Verilog-A models integrated within a schematic environment, and transient simulations are analyzed to verify functionality and performance. The Sample-and-Hold circuit is essential in ADC systems to capture and maintain a stable voltage level from the analog input during the conversion process. It ensures that the comparator evaluates a consistent voltage during each decision cycle. The S/H circuit feeds its output (vout) directly to the vin input of the comparator. Both circuits are driven by synchronized clock signals to ensure correct timing and sequencing of the SAR ADC operation. The Sample-and-Hold (S/H) and clocked comparator blocks were individually modelled in Verilog-A to capture their key timing and signal processing behaviours while maintaining manageable simulation complexity. The S/H model simulates the sampling of the input analog voltage on the rising edge of the clock and holds it steady during the hold phase. It incorporates parameterized timing features such as delays and transition times to realistically mirror circuit responses. The clocked comparator model performs a voltage comparison between the input voltage and a reference signal at each rising clock edge, outputting differential logic signals indicating comparator results. It also resets outputs on the clock's falling edge, preparing for the subsequent comparison cycle. Timing parameters provide realistic signal propagation and transition modelling. These two behavioural models were integrated to form a synchronized functional unit representing the sample-and-hold followed by clocked comparison operation, emulating the data acquisition and decision-making sequence within the SAR ADC conversion process. This integration facilitated early validation and system level simulation of the timing and functional correctness of these front-end blocks before transistor-level integration with other ADC components.

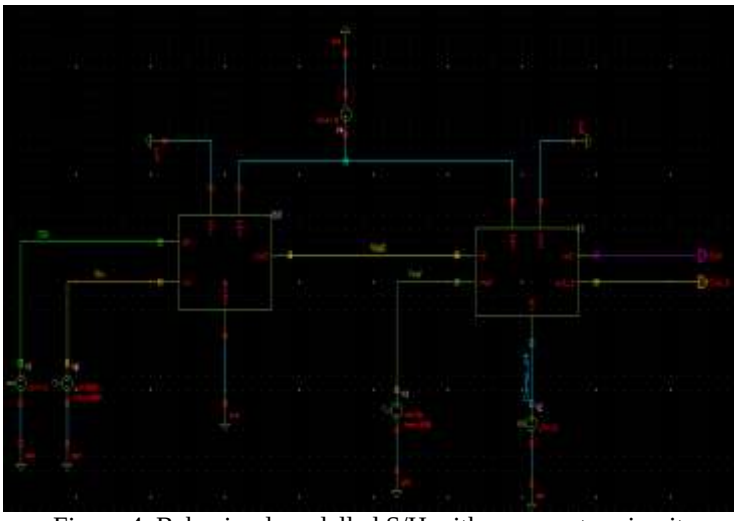

Figure 4. Behavioral modelled S/H with comparator circuit

The Successive Approximation Register (SAR) plays a crucial role in the operation of a SAR Analog-to-Digital Converter (ADC). The SAR logic controls the binary search algorithm that successively approximates the input analog voltage to a digital code. This segment discusses the design and implementation of the SAR logic using True Single-Phase Clock (TSPC) D Flip Flops, explaining the motivation behind the choice of flip-flop architecture, the construction of the SAR logic circuit, and the analysis of its working based on the obtained simulation waveforms. True Single-Phase Clock (TSPC) D flip-flop is a dynamic flip-flop that operates using a single-phase clock without the need for complementary clock signals. It combines latches and pass transistors in a way that eliminates the need for clock skew management between multiple phases. The TSPC D flip-flop, shown in the schematic below, is composed of several PMOS and NMOS transistors arranged to form dynamic logic stages. This topology operates efficiently using a single-phase clock, reducing clock routing complexity and power consumption compared to conventional master-slave flip-flop designs. The circuit supports SET and RESET functionalities, enabling flexible initialization and control during the SAR conversion cycles. Each flip-flop reliably latches the input data on the clock edge while dissipating minimal power, making it highly suitable for high-speed ADC logic.

Figure 5. TSPC d flipflop

This TSPC FlipFlop is chosen for their high-speed operation since they have faster switching capabilities compared to conventional static flip-flops due to fewer internal nodes and transistors, lower power consumption because dynamic operation reduces short-circuit currents and static power, reduced clock load because of its Single-phase clock it simplifies clock distribution, crucial for high-speed ADCs like the targeted 40 MSPS SAR ADC and its Compact Area, as the transistor count is lower, helping with area efficiency in dense digital circuits.

For 12-bit resolution, a chain of fourteen TSPC D flip-flops has been connected in sequence. This configuration implements the complete SAR register, with each flip-flop corresponding to a single bit and collectively realizing the required bit-wise control logic for the SAR algorithm. During each conversion step, the SAR logic updates and holds the appropriate bit decision, synchronizing with the comparator output and the clock, ensuring accurate and rapid successive approximation. This fully transistor-level SAR logic implementation provides robust performance at high conversion speeds and enables fine-grained analysis of timing, power, and signal integrity within the SAR ADC.

The SAR logic was designed as a 12-bit control unit, where each bit decision is stored and propagated using TSPC D flip-flops. The logic controls the switching of the internal DAC in the ADC and dictates the comparator decision at each clock cycle. Each flip-flop captures and holds the decision of each comparator cycle and shifts the control to the next bit in the subsequent cycle.

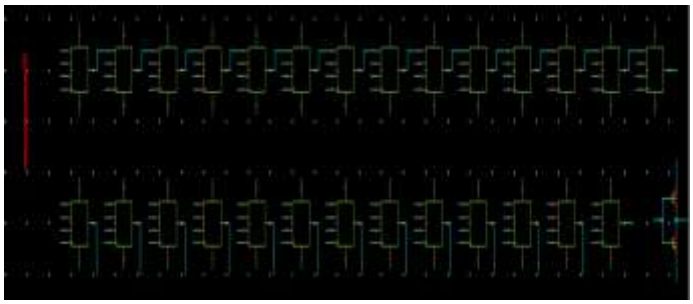

Figure 6. SAR logic chain

SAR ADCs operate on the principle of binary search using a sample-and-hold circuit, a charge redistribution digital-to-analog converter (CDAC), a comparator, and SAR control logic. Each conversion begins by sampling the analog input onto the DAC, followed by N comparison cycles to resolve an N-bit digital output. Their architecture benefits from low power consumption, absence of operational amplifiers, and digital simplicity, which fits well with standard CMOS processes. The DAC plays a central role in defining the linearity, resolution, and speed of the ADC. In SAR ADCs, capacitor-based DACs are preferred due to their monotonicity and inherent matching properties. However, switching schemes within the DAC have evolved to improve energy efficiency and reduce capacitor area.

The model operates in two phases: sampling and conversion. During the sampling phase (when the clock signal is high), the entire capacitor array samples the analog input voltage, generating a charge proportional to $C_{total} \times V_{in}$. In the conversion phase (clock is low), charge redistribution occurs as capacitors switch according to the digital input bits, adjusting the total charge and resulting voltage output. The output voltage is computed by balancing the total charge on the capacitor array and simulating the settling time based on the capacitor size and switching resistance.

This behavioral CDAC model accurately reflects the physical operation of charge redistribution DACs, capturing the switching dynamics, charge sharing, and settling behavior essential for realistic SAR ADC simulations. Integrating parameters such as parasitic capacitance and switching delays enables refined system-level evaluation of speed, linearity, and power efficiency.

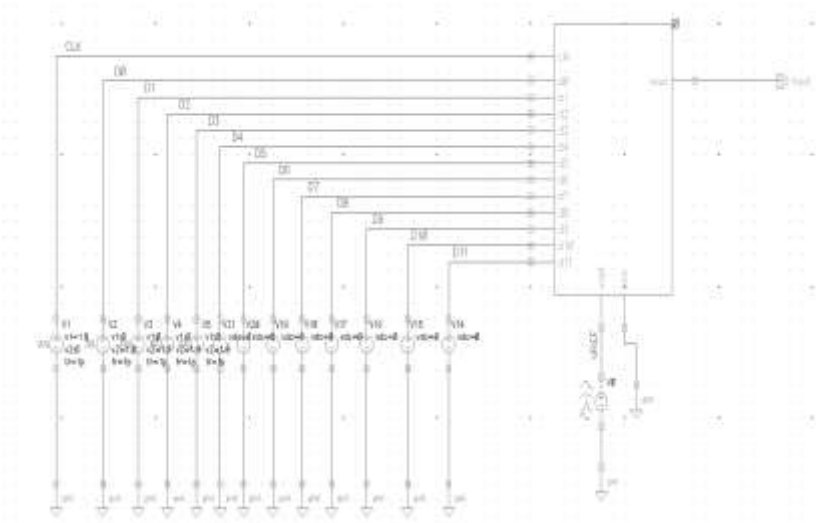

Figure 7. 12-bit capacitive dac

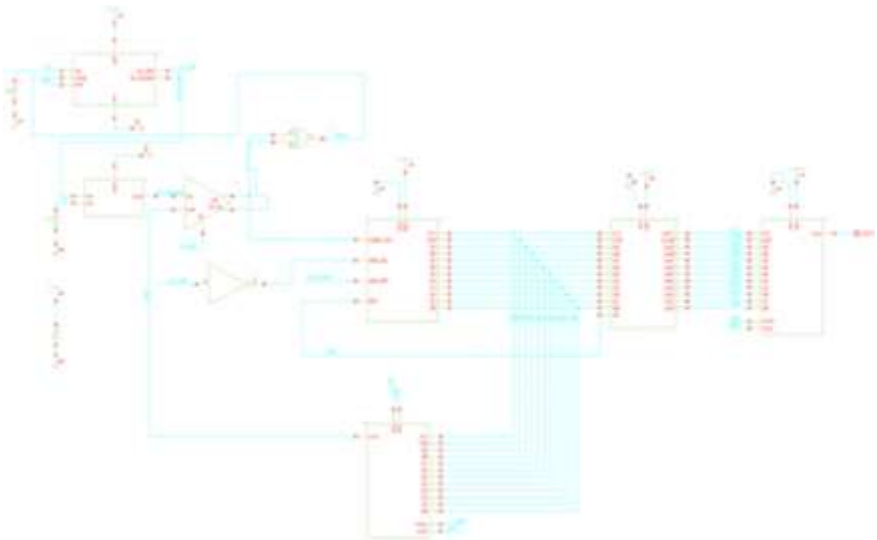

Figure 8. Proposed sar adc system

V. RESULTS AND DISCUSSIONS

Simulations for all the transistor-level and VerilogA modelled designs were done in SCL 180nm technology with a supply of 1.8 V and the outputs were analyzed alongside the required features for designing the 12-bit 40 Msps SAR ADC for GPR applications. The performance metrics were recorded and analyzed according the output waveforms obtained for all the designs.

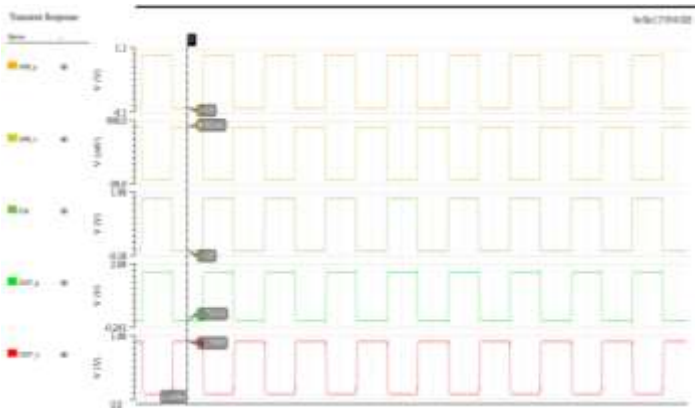

Figure 9. Output waveform of strong-arm design

All the W/L ratios were calculated using the drain current formula based on the drain current and region of operation, and the the Tail mosfet and Differential Pair being the major player, their W/L ratio were calculated to be, tail mosfet = 7.5u/0.18u and differential pair = 2.5u/0.18u; for a valid functioning to get the required output of 40 MHz and average power dissipation of 13.33uW and with a delay of 30.3 ns which was quite a value over than the least required delay. On the other hand, with the modelled comparator incorporating many features and its rail-to-rail design as described in the previous section, the results were out to be;

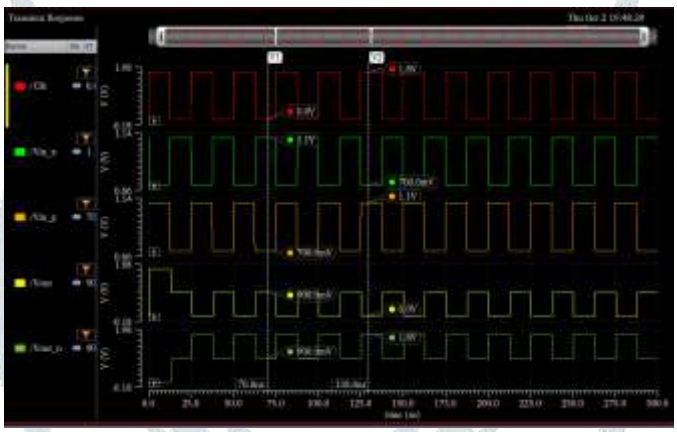

Figure 10. Output of behavioral modelled comparator

Figure 11. Output Power of the Modelled Comparator

with the performance metrics being, delay of 24 ns, within the required limit, sampling frequency of 40.355 MHz, and power consumption of 1.545 mW with with all features incorporated. Point to be noted is that, comparator is one among the most important module and it consumes more power than any other module in the design.

For the S/H design, with Vref being 900 mV, the complete system successfully samples the analog signal, holds it, and allows the comparator to make decisions based on the held value. The comparator outputs show accurate transitions corresponding to the sampled signal's relationship with the reference voltage.

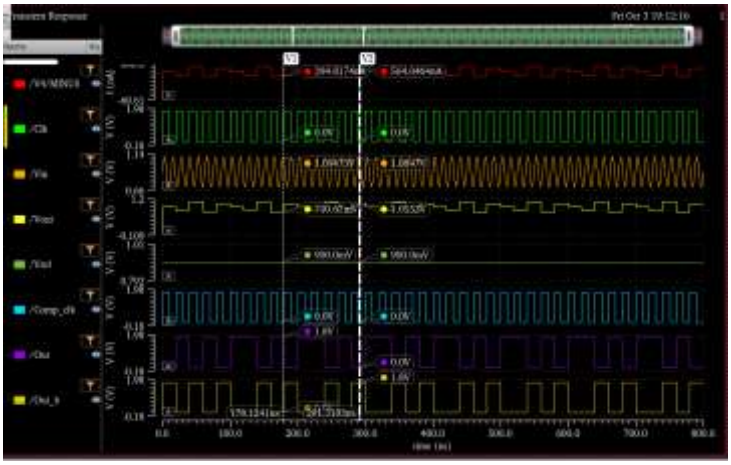

Figure 12. Waveform of S/H with Comparator

Figure 13. Average power of S/H with comparator

In the SAR logic design, the SAR clock (sar_clk) drives the entire logic sequentially, while asynchronous SET and RESET signals help in initializing the system. The SAR logic interfaces with the comparator output (comp_out) and the sampling clock to update the approximation bit-by-bit. The End of Conversion (EOC) signal is generated when the entire 12-bit sequence completes. EOC high after all 12-bit conversion. EOC signalled high well within 25 ns (24.45 ns) of the conversion as seen in the graph below;

Hence sampling rate = 1/25 ns = 40 MSPS, as required by the design is observed.

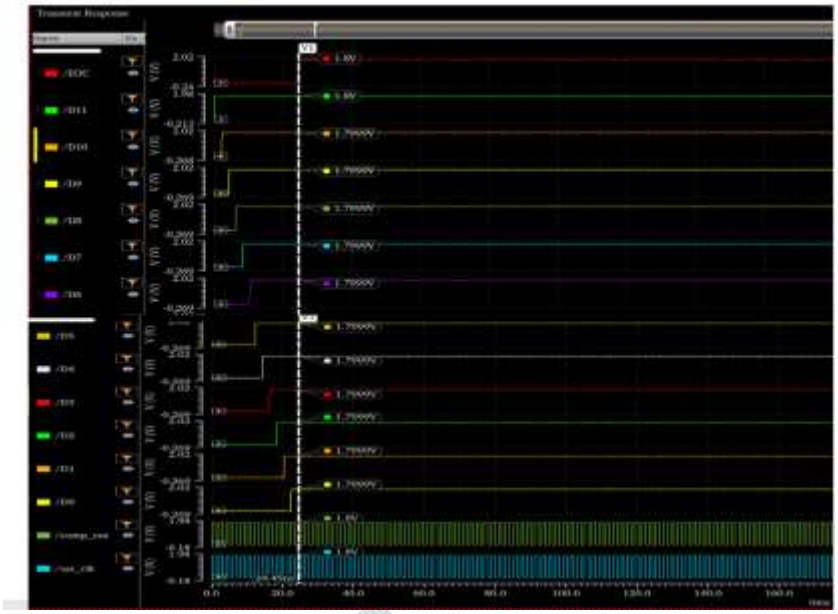

Figure 14. Sar logic conversion output

In another important module being the C-DAC, based on the Verilog model description and the DAC functionality with Vref 1.8 V, the results were observed and tabularized as below;

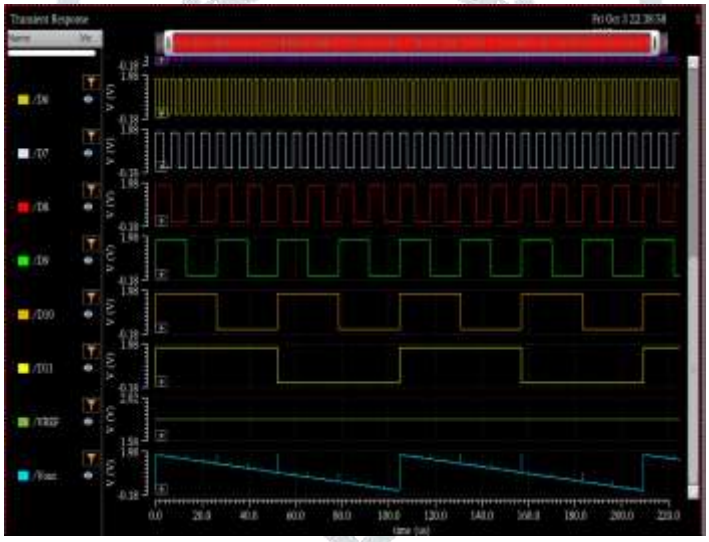

Figure 15. Output waveform of c-dac

Table 2: Tabularized Observation of C-DAC

Parameter	Ideal	Observed
Resolution	12 Bit	12 Bit
Vref	1.8 V	1.8 V
Linearity	DNL < ± 0.5 LSB	DNL < + 0.14 LSB
Full Scale	1.8 V	1.7996 V
Step-Size	0.4395 mV	0.5 mV

VI. CONCLUSION

Successive Approximation Register (SAR) ADCs continue to be highly favored in both industry and academia for applications requiring a balanced trade-off between speed, resolution, power consumption, and implementation complexity. This project comprehensively explored and developed key building blocks of a 12-bit, 40 MSPS SAR ADC suitable for ground penetrating radar (GPR) systems, where accuracy, high sampling rate, and power efficiency are paramount.

A strong-arm latch comparator was designed at the transistor level, leveraging a multi-stage architecture to achieve high speed and low offset, while the behavioral Verilog-A model provided realistic analog behavior including noise, power, offset, and timing effects. This comparator effectively meets GPR speed and accuracy requirements, offering a good balance between performance and power efficiency.

A charge-redistribution capacitive DAC (CDAC) was implemented with detailed parametric behavioral modeling, capturing the essential charge sampling and redistribution dynamics critical to SAR ADC operation. The CDAC design aligns well with the SAR topology, optimizing for high speed and low power, which are vital in constrained GPR environments.

The SAR logic was realized using transistor-level TSPC D flip-flops arranged in a chain to control the bit-wise successive approximation process. This design provides robust timing control and low power consumption necessary for rapid and accurate digital decision making in SAR conversion. Additional behavioral models for the sample-and-hold circuit and a clocked comparator were developed and integrated, allowing early system-level verification of timing and functional correctness. Simulation results across all building blocks validate the correctness and effectiveness of the design approach. The project demonstrates essential SAR ADC functionality: precise sampling, successive comparison, decision storage, and conversion completion signaling.

Overall, this work establishes a strong foundation for a complete, efficient, high-speed 12-bit SAR ADC tailored for demanding GPR applications.

VII. FUTURE SCOPE

Building on the foundation laid by this 12-bit, 40 MSPS SAR ADC design for GPR applications, the following key areas offer important directions for future work:

1. Post-Layout and Parasitic Analysis Advancing from behavioral and schematic simulations to physical layout, parasitic extraction, and post-layout simulations will provide precise characterization of delay, power, and noise effects critical for robust operation.

2. Robustness via Statistical and Corner Simulations Performing Monte Carlo and process-voltage temperature (PVT) corner analyses will quantify the influence of manufacturing variability and environmental conditions, enabling improved design yield and reliability.

3. System-Level Integration and Full ADC Implementation Integration of all designed blocks—comparator, CDAC, sample-and-hold, and SAR logic—into a complete SAR ADC system followed by hardware-level verification is crucial to validate interoperability. real-time performance and interoperability.

4. Power, Area, and Performance Optimization Further refinement through transistor-level optimization, supply scaling, and exploration of advanced CMOS nodes will enhance energy efficiency and reduce silicon area while sustaining required speed and accuracy.

5. Radiation Hardened Design Techniques Considering potential deployment in radiation-prone environments, incorporating radiation hardened design methods—such as enclosed layout transistors, guard rings, hardened flip flops, and error correction—will improve fault tolerance, ensuring reliable ADC function under ionizing radiation.

This streamlined future scope focuses on the pivotal next steps to transition your SAR ADC project towards a practical, reliable, and efficient system for GPR and similar high performance sensing applications.

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