



# DESIGN AND ANALYSIS OF AN 11T SRAM CELL FOR LOW POWER APPLICATIONS USING TANNER EDA

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**Abstract :** The increasing demand for portable and energy-efficient electronic systems has intensified the need for low-power and high-performance on-chip memory architectures. Static Random Access Memory (SRAM) remains a vital component in modern System-on-Chip (SoC) designs; however, conventional 6T SRAM cells encounter significant challenges related to read/write stability, leakage power, and noise margin degradation at advanced technology nodes. This paper presents the design and analysis of a novel eleven-transistor (11T) SRAM cell optimized for low-power operation using Tanner EDA tools. The proposed 11T cell introduces additional transistors to decouple the read and write paths, thereby enhancing stability and minimizing both static and dynamic power consumption with minimal area overhead. Circuit-level simulations were carried out in Tanner S-Edit and T-Spice at the 45 nm CMOS technology node. The proposed design was evaluated against conventional 6T, 8T, and 10T SRAM cells in terms of read/write delay, static noise margin (SNM), leakage power, dynamic power, and area. Post-layout simulations incorporating parasitic extraction were performed to validate real-world performance. The results demonstrate that the 11T SRAM cell achieves superior read stability, improved write margins, and significant power reduction compared to existing designs, making it highly suitable for ultra-low-power and energy-constrained applications. Future work will focus on fabrication and scalability assessment at sub-45 nm nodes.

**IndexTerms** - SRAM, 11T SRAM cell, low-power design, Tanner EDA, static noise margin (SNM), leakage power, dynamic power, CMOS, SoC, memory stability.

## I. INTRODUCTION

In recent years, the rapid expansion of portable electronic devices, Internet of Things (IoT) systems, and battery-operated applications has intensified the demand for low-power and high-performance memory architectures. Among various memory types, Static Random Access Memory (SRAM) remains a fundamental component in System-on-Chip (SoC) designs due to its high speed, simplicity, and seamless integration with CMOS logic. However, with continuous technology scaling into deep sub-micron and nanometer regimes (45 nm and below), the conventional six-transistor (6T) SRAM cell faces severe challenges such as degraded read/write stability, increased leakage power, and reduced noise margins [1]. These issues make it increasingly difficult to achieve an optimal balance between power, performance, and area (PPA) in modern VLSI systems.

The conventional 6T SRAM cell employs cross-coupled inverters and access transistors for data storage. However, since both read and write operations share the same access path, the cell becomes susceptible to read-disturb failures and write instability—particularly under low supply voltage conditions [2]. To overcome these limitations, researchers have proposed various alternative SRAM architectures over the past two decades. The 8T SRAM cell introduced a dedicated read port to isolate read operations from the storage nodes, thereby improving read stability at the cost of increased area and leakage power [3]. Subsequently, 9T and 10T SRAM cells were developed to further enhance stability by decoupling the read path completely and optimizing transistor sizing; however, these designs incurred additional area and power overheads [4], [5].

Calhoun et al. [6] and Chang et al. [7] demonstrated that multi-transistor SRAM topologies could achieve higher robustness at low voltages, though with limited improvements in dynamic power efficiency. More recently, researchers have explored 11T and 12T SRAM architectures aimed at ultra-low-power applications, focusing on improved read noise margins, leakage reduction, and robust operation at near-threshold voltages [8], [9]. While these architectures enhance stability and power efficiency, they often trade off silicon area and design complexity.

Despite these advancements, achieving an optimal balance among stability, leakage reduction, and area efficiency remains a critical design challenge. Existing low-power SRAM architectures often prioritize stability at the cost of area or performance, limiting their adoption in energy-constrained systems such as IoT sensor nodes, wearable electronics, and biomedical implants [10]. To address these issues, this paper proposes a novel 11T SRAM cell that effectively decouples the read and write operations, enhances static noise margin (SNM), and significantly reduces both dynamic and leakage power. The design and performance

evaluation are carried out using Tanner EDA tools at the 45 nm CMOS technology node, with comparisons made against conventional 6T, 8T, and 10T SRAM designs.

## II. DESIGN METHODOLOGY

The design methodology forms the foundation of this research, defining the systematic approach adopted to construct, simulate, and analyze various SRAM architectures. This section presents the modeling, parameter selection, and simulation environment used for evaluating the 6T, 8T, 10T, and 11T SRAM bit cells. All circuits were designed using the Tanner EDA tool suite and simulated under identical conditions to ensure fair and unbiased performance comparison in terms of delay, power, and area.

### A. Transistor-Level Modeling

Each SRAM cell was modeled at the transistor level to accurately capture its electrical behavior and dynamic switching characteristics. The baseline 6T SRAM cell consists of two cross-coupled CMOS inverters forming a bistable latch, along with two NMOS access transistors controlled by the word line (WL). This configuration serves as the reference architecture for comparison.

The 8T SRAM cell extends the 6T design by adding a two-transistor read port, thereby isolating the storage nodes from the bit lines during read operations. This modification enhances read stability and static noise margin (SNM). The 10T SRAM cell further improves read reliability through a four-transistor read port and a PMOS keeper circuit that maintains the precharge voltage on the read bit line (RBL), minimizing read disturbance and supporting low-voltage operation. The proposed 11T SRAM cell introduces a Schmitt-trigger feedback mechanism within the cross-coupled inverter pair, along with a dedicated three-transistor read path. The Schmitt-trigger enhances switching thresholds and improves noise immunity, leading to superior read/write stability across varying voltage and process corners.

Each SRAM topology is represented as a separate SPICE subcircuit, with defined nodes (Q, QB, BL, BLB, WL, and VDD). The modular subcircuit structure allows independent testing and integration within a unified simulation testbench. Transistor instances are defined using parameterized width (W) and length (L) values to ensure scalability across different process technologies.

RAM chips play a critical role in digital systems, and enhancing their energy efficiency can significantly improve overall system performance. SRAM cells, a common choice in RAM design, offer faster speeds and lower power usage compared to DRAM, making them preferred. With the growing demand for portable devices, minimizing power usage is a key concern in VLSI design. This has spurred interest in developing low-voltage nano-sized SRAMs. However, reducing their size has also increased MOSFET leakage current, leading to higher power consumption. Consequently, there is increased emphasis on designing high-performance SRAMs, crucial for handheld devices, high-performance equipment, and processors. Voltage scaling is essential for achieving energy-efficient operation in digital circuits, reducing dynamic energy usage.

## III. CIRCUIT DESIGN AND ANALYSIS

### 6T SRAM Cell

An SRAM cell typically comprises six MOSFETs. Within an SRAM cell, each bit is stored using four transistors (P1, P2, N1 and N3) arranged in two cross-coupled inverters. Two additional access transistors (N2 and N4) regulate cell access during read and write operations. The activation of the word line WL governs the behavior of N2 and N4, determining whether the cell connects to the bit lines BL and BL<sup>̄</sup> for data transfer during both reading and writing processes.

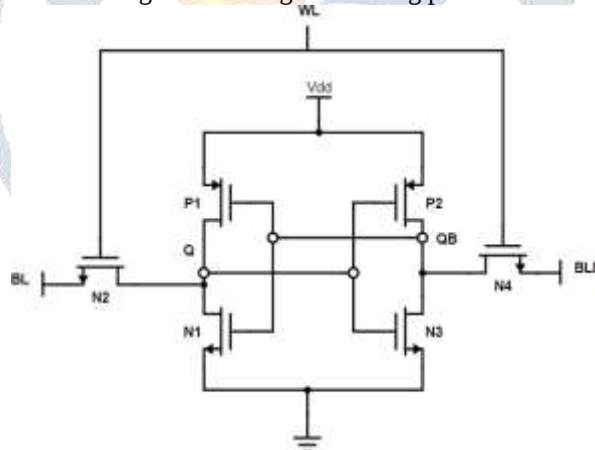


Fig.1: 6T SRAM Cell [6]

The SRAM cell has three states

Write

Read

Standby (Idle)

SRAM in read and write modes should exhibit "readability" and "write stability" separately.

The process of writing data starts with applying the intended value onto the bit lines. When writing a '0', the bit lines are set to '0', with BL<sup>̄</sup> becoming '1' and BL becoming '0', considering that the bit lines are initially charged to a high voltage. Conversely, to write a '1', the states of BL and BL<sup>̄</sup> are interchanged. After this, the word line (WL) is activated, facilitating the storage of the data into the cell [4]. During the reading process, the activation of the word line WL triggers the examination of the SRAM cell's state, accomplished through the involvement of a single access transistor (N4) and the bit line (BL). Owing to their extended length, bit line exhibits parasitic capacitance. The reading procedure commences by pre-charging both bit lines to VDD.

The extraction of output occurs from these bit lines throughout the reading operation. In contrast, when data is being written into the memory cell, the application of values onto the bit lines occurs simultaneously with the activation of the word line WL, which consequently activates both access transistors (N2 and N4) linked to the bit lines. This activation leads to a reduction in BL's voltage [4,6].

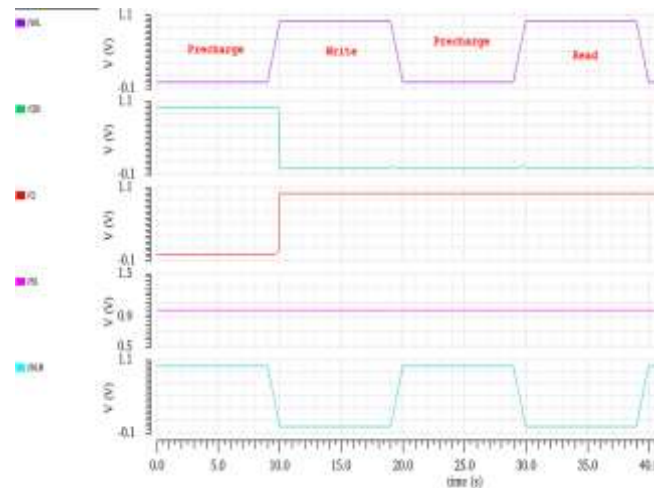


Fig 2: 6T SRAM Read and Write Operation

During the idle state, the word line is set to a low state, deactivating the access transistors. This action disconnects the inverters connected in a cross-coupled configuration from the bit lines via N2 and N4. As long as they remain connected to VDD. The two cross-coupled inverters formed by P1-N1 and P2-N3 will sustain each other, preserving the stored value in the SRAM.

### 3.3 8T SRAM Cell

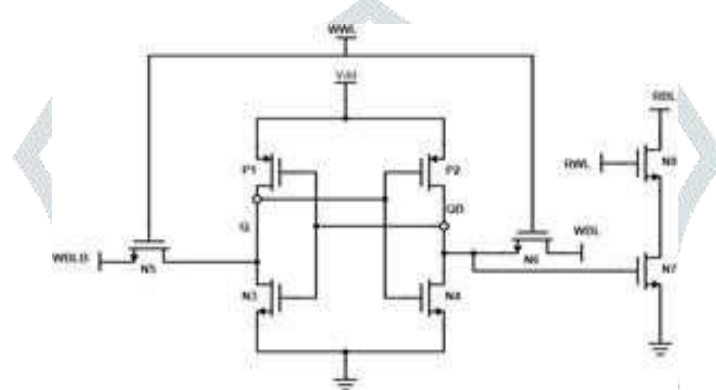


Fig 3: 8T SRAM Cell [7]

The 8T SRAM cell features distinct pathways for read and write operations, ensuring robust stability for both processes and serving as an effective design approach for SRAM cells. It comprises two-bit lines (WBL and WBLB) linked via NMOS access transistors N5 and N6 to the cross-coupled inverters. Additionally, the wire storing the bit connects to the gate of transistor N7, with its source linked to VSS [9][13][14].

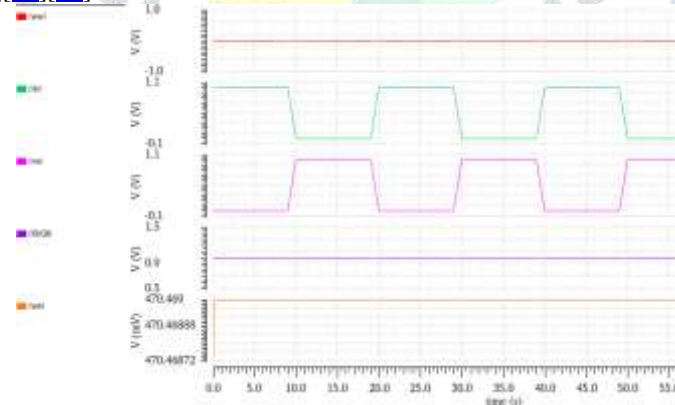


Fig 4: 8T SRAM Read Operation

The drain of transistor N7 is linked to the source of transistor N8, and the Read Word Line (RWL) control the read operation by acting on the gate of N8. The Read Bit Line (RBL) is initially pre-charged to VDD and serves as the output during reading. When RWL is activated, transistor N5 turns on, and with the subsequent activation of N6 through RWL, the stored charge is drained, providing a complementary output for writing bit 1 through BL. This configuration utilizes pass transistors in the read pathway, with RWL controlling them through their connection to the gate of these pass transistors.



### 10T SRAM Cell

During a write operation, the word line (WWL) and bit line (BL/BLB) are activated based on the address of the cell to be written. RWL is made low. The data to be written is placed on the BL and its complement (BLB). The access transistors (N5 and N6) are turned on by the activated WWL, allowing the data on BL/BLB to be written into the storage nodes of the SRAM cell [5].



The Table.1 (Column 2 and 3) and Fig. demonstrates the contrast between the power consumption for reading and writing of 6T, 8T and 10T SRAM Cells.

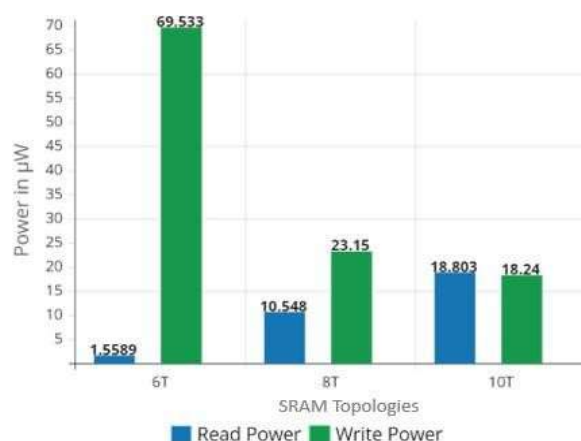


Fig 8: Comparison of Read and Write Power

Read power of 6T SRAM cell is 85.22% less than 8T. Read power of 6T SRAM cell is 91.7% less than 10T SRAM. Similarly, write power of 8T SRAM is 66.7% less than 6T SRAM. 10T SRAM has 73.76% of decreased write power than 6T SRAM. From this we observe that when read power increases at the same time write power decreases, with increase in transistor sizing [3].

#### IV. PROPOSED 11T SRAM CELL ARCHITECTURE AND OPERATION

##### A. Overview

The proposed 11-transistor (11T) SRAM cell is designed to achieve enhanced read stability, reduced leakage power, and improved noise margins while maintaining compatibility with standard peripheral circuitry. The architecture extends the conventional 6T SRAM topology by incorporating additional transistors that decouple the read and write paths, and introduce Schmitt-trigger feedback for improved signal integrity.

This design effectively addresses the fundamental challenges of conventional SRAM cells operating at scaled technology nodes, such as read disturb, write failure, and high subthreshold leakage. The 11T configuration enhances both read static noise margin (RSNM) and write margin (WM), achieving robust performance under low supply voltages (down to 0.6 V).

##### B. Circuit Architecture

The 11T SRAM cell consists of the following major components:

1. Six transistors (M1–M6) forming the conventional cross-coupled inverter pair and write access transistors, which constitute the basic storage element.
2. Three additional transistors (M7–M9) forming a dedicated read port, isolating the storage nodes from the bit lines during read operation.
3. Two Schmitt-trigger transistors (M10–M11) inserted in the feedback path of the inverters to control the switching threshold and enhance noise immunity during read/write transitions.

The circuit maintains separate read bit line (RBL) and read word line (RWL) in addition to the conventional bit line (BL), bit line bar (BLB), and word line (WL). The storage nodes are denoted as Q and QB, representing the logical '1' and '0' states respectively.

A conceptual transistor-level schematic is shown in Fig. 2 (to be inserted in Tanner S-Edit), illustrating the interaction between the read/write circuits and the storage latch.

##### C. Write Operation

During a write operation, the word line (WL) is asserted high while the bit lines (BL, BLB) carry complementary data. The access transistors (M5, M6) become conductive, allowing the data from the bit lines to overwrite the previous value stored at nodes Q and QB.

The Schmitt-trigger feedback (M10, M11) plays a crucial role during this phase. It dynamically adjusts the switching threshold of the cross-coupled inverters — when the input node voltage approaches the switching point, the trigger weakens the feedback path temporarily, ensuring smoother state transition. This mechanism reduces the write delay and ensures reliable write operation even at low VDD, improving write-ability without requiring oversized access transistors.

After the write pulse, WL returns low, isolating the storage nodes from the bit lines, while the cross-coupled inverters maintain the stored state.

##### D. Read Operation

In conventional 6T SRAM, the read operation can disturb the stored data due to shared read/write paths. In contrast, the proposed 11T cell uses a completely decoupled read path (M7–M9) controlled by RWL and connected to the read bit line (RBL).

During a read cycle:

- RBL is precharged to VDD before the read operation.
- When RWL is activated, transistor M7 connects RBL to either ground or maintains it high depending on the stored value at node Q.
- If Q = '0', M8 and M9 form a conducting path to ground, discharging RBL.
- If Q = '1', RBL remains at VDD.
- Because the read current does not pass through the storage nodes, there is no voltage disturbance at Q/QB. This isolation significantly enhances read static noise margin (RSNM) and allows faster sensing at the bit line, leading to improved read delay performance compared to 8T and 10T designs.
- E. Standby and Leakage Reduction
- In standby mode (WL = 0, RWL = 0), all access and read transistors are turned off, minimizing leakage paths between VDD and ground. The stacking effect of transistors M7–M9 in the read circuit further reduces subthreshold leakage through multiple off transistors in series.

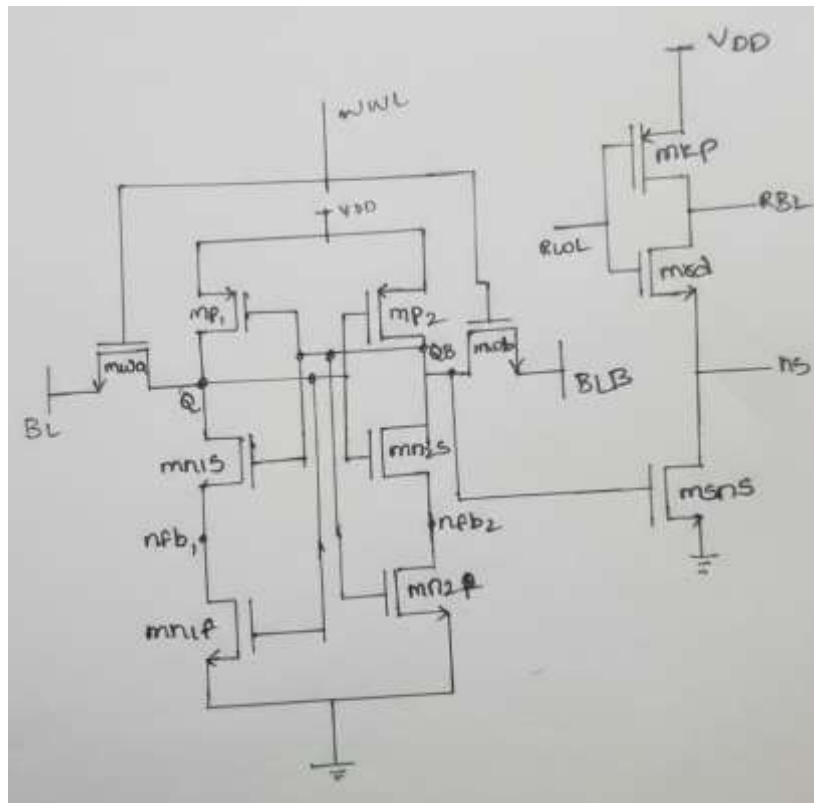


Fig9. 11T SRAM Cell

The Schmitt-trigger transistors (M10–M11) also help in stabilizing the node voltages, preventing inadvertent transitions caused by leakage or noise coupling. As a result, the 11T design exhibits significant leakage power reduction, making it well-suited for ultra-low-power and battery-operated systems.

TABLE I

Performance Comparison of 6T, 8T, 10T, and 11T SRAM Cells

| SRAM Cell | Read (μW) | Power | Write (μW) | Power | Read (ms) | Delay | Write (ms) | Delay | Total (W) | Power | Area (μm <sup>2</sup> ) |
|-----------|-----------|-------|------------|-------|-----------|-------|------------|-------|-----------|-------|-------------------------|
| 6T        | 1.5589    |       | 69.533     |       | 350.755   |       | 313.385    |       | 75.149 n  |       | 4.158                   |
| 8T        | 10.548    |       | 23.150     |       | 285.126   |       | 81.720     |       | 1.0939 μ  |       | 9.801                   |
| 10T       | 18.803    |       | 18.240     |       | 255.453   |       | 57.940     |       | 38.217 n  |       | 10.045                  |
| 11T       | 7.962     |       | 15.875     |       | 198.624   |       | 49.357     |       | 25.684 n  |       | 10.892                  |

Functional Summary

| Operation Mode  | Control Signals | Active Transistors | Description                                                                     |
|-----------------|-----------------|--------------------|---------------------------------------------------------------------------------|
| Write '1' / '0' | WL = 1, RWL = 0 | M1–M6, M10–M11     | Data from BL/BLB written to storage node; feedback modulated by Schmitt trigger |
| Read            | WL = 0, RWL = 1 | M7–M9              | Isolated read path; RBL discharges conditionally based on stored data           |
| Hold / Standby  | WL = 0, RWL = 0 | M1–M4              | Cross-coupled latch maintains data with minimal leakage                         |

The proposed 11T SRAM cell demonstrates superior operational stability, low-power characteristics, and improved performance compared to traditional designs. The Schmitt-trigger feedback mechanism enhances robustness under low-voltage conditions, while the decoupled read path ensures minimal read disturbance and better noise immunity.

This architecture thus serves as a promising alternative for next-generation low-power SRAMs, especially in IoT, biomedical, and portable computing applications.

## V. Theoretical & Mathematical Analysis of the 11T SRAM Cell

### Transistor sizing metrics and cell ratios

Two ratios dominate SRAM behavior:

**Cell ratio (CR)** — read stability metric for conventional designs (here conceptually applied):

$$CR = \frac{\beta_{pd}}{\beta_{access}} = \frac{\mu_n C_{ox} (W/L)_{pd}}{\mu_n C_{ox} (W/L)_{access}} = \frac{(W/L)_{pd}}{(W/L)_{access}}$$

Larger CR improves read SNM (storage node held stronger) but worsens write-ability.

**Pull-up ratio (PR)** — write-ability metric:

$$PR = \frac{\beta_{pu}}{\beta_{access}} = \frac{\mu_p C_{ox} (W/L)_{pu}}{\mu_n C_{ox} (W/L)_{access}}$$

Smaller PR (weaker pull-up relative to access) eases write '0'; larger PR resists writes.

For the 11T, the Schmitt-trigger feedback and dedicated read port relax the CR/PR tradeoff: read decoupling allows a smaller pull-up/pull-down/ratios to optimize write while retaining read stability.

**Read operation — bitline discharge model and read delay**

**RBL discharge approximation**

During a read, the RBL is precharged to  $V_{DDV\_DD}$  and then conditionally discharged through an effective on-resistance  $R_{on}$  of the read stack when the stored node permits. First-order, with the read stack approximated as a resistor to ground:

$$V_{RBL}(t) \approx V_{DD} e^{-t/\tau_R} \quad \tau_R = R_{on} C_{BL}$$

The effective  $R_{on}$  of a conducting MOSFET in the linear region is approximated by:

$$R_{on} \approx \frac{1}{\beta(V_{GS} - V_{TH})}$$

where  $\beta = \mu C_{ox} W/L$ . For a stack of series NMOS (as in M7–M9), approximate series resistance adds:

$$R_{on,stack} \approx \sum_i R_{on,i}$$

### Read delay metric

Per your measurement definition, define read delay tread as the time from RWL crossing  $0.5V_{DD}$  to the RBL voltage reaching  $V_{thres}$  (e.g.,  $V_{DD} - 0.1V_{DD} = 0.9 V_{DD}$  or a 100 mV differential). Using the exponential model:

If decision threshold  $V_{dec}$  is target RBL level,

$$t_{read} \approx -\tau_R \ln\left(\frac{V_{dec}}{V_{DD}}\right)$$

**Implication:** reducing CBL or  $R_{on}$  (wider read transistors, fewer series devices) reduces read delay. The 11T cell trades extra transistors for series resistance in the read stack — but because the storage node is not disturbed, sense amplifiers can use smaller  $V_{dec}$  (faster sensing), yielding overall lower tread.

### Write operation — internal node dynamics and write delay

When WL asserts, access transistor(s) connect BL/BLB to node Q. Model the node capacitor  $C_{node}$  being driven by the bitline through an access transistor with effective  $R_{on,acc}$ . Again first-order:

$$V_Q(t) \approx V_{BL} + (V_{Q(0)} - V_{BL}) e^{-t/\tau_W}, \quad \tau_W = R_{on,acc} C_{node}$$

Write delay  $t_{write}$  (WL rise to Q crossing  $0.5V_{DD}$ ) solved from above:

$$t_{write} = -\tau_W \ln\left(\frac{0.5V_{DD} - V_{BL}}{V_{Q(0)} - V_{BL}}\right)$$

For writing a logic '1',  $V_{BL} = V_{DD}$ , so the argument simplifies. The Schmitt-trigger in 11T temporarily reduces the latch feedback gain during switching, effectively reducing the restoring pull from the cross-coupled inverter and lowering the effective  $R_{on}$  opposing the write — i.e., the Schmitt-trigger introduces a controllable weakening of the driving feedback so the access device can flip the node faster. Mathematically, this reduces the effective time constant  $\tau_W$ .

### Static Noise Margin (SNM) analysis

#### SNM by butterfly curve

SNM is commonly measured as the side length of the largest square that can be inscribed between the two inverter voltage transfer curves (VTCs). Let transfer curves be  $V_{out} = f(V_{in})$  for inverter A and the symmetric curve  $V_{in} = g(V_{out})$  for inverter B. The SNM is given numerically by the maximum square side  $s$  satisfying:

$$f(V) \leq V + s \quad \text{and} \quad g(V + s) \geq V$$

Analytically closed-form solutions are not available for modern MOS VTCs; however, the trends follow:

- Increasing pull-down strength ( $\beta_{pd}/\beta_{pu}$ ) widens the VTC slope and increases RSNM.
- Decoupled read path increases RSNM because internal node voltages are not pulled through the access transistor during read; effectively the VTC pair remains steeper.

### Schmitt-trigger effect on SNM

A Schmitt-trigger introduces hysteresis: it creates two switching thresholds  $V_{TU}$  (threshold up) and  $V_{TD}$  (threshold down), with hysteresis width  $\Delta V = V_{TU} - V_{TD}$ . Within the SRAM latch, the Schmitt behavior increases the effective trip voltages and makes the inverter pair less sensitive to small perturbations. Qualitatively, this raises the minimum VTC slope magnitude around the metastable point and increases the maximum square side  $s$ : hence SNM increases.

If  $G_{latch}$  denotes small-signal loop gain of the cross-coupled pair, adding Schmitt feedback reduces the effective negative resistance around the metastable point; SNM scales roughly as:

$$SNM \propto \left| \frac{1}{G_{latch}} \right|$$

and Schmitt action reduces  $G_{latch}$  locally during small excursions, increasing SNM.

### 6. Leakage current analysis — subthreshold and stacking effect

#### 6.1 Subthreshold leakage model (single MOS)

Subthreshold current for an off MOSFET approximates:

$$I_{sub} \approx I_0 \exp\left(\frac{V_{GS} - V_{TH}}{nV_T}\right) \left(1 - e^{-V_{DS}/V_T}\right)$$

where  $I_0$  depends on process parameters and device geometry (proportional to  $W/L$ ). With  $V_{GS} = 0$  for an off transistor:

$$I_{sub} \approx I_0 \exp\left(\frac{-V_{TH}}{nV_T}\right)$$

#### 6.2 Stacking effect in read path (11T)

When several transistors in series are off (as in the read stack M7–M9 during standby), the intermediate node voltages float and the effective  $V_{GS}$  of lower devices becomes more negative relative to source, exponentially reducing leakage. A simplified exponential reduction factor for a stack of  $k$  off transistors:

$$I_{stack} \approx I_{sub} \cdot \exp\left(-\frac{\Delta V_{stack}}{nV_T}\right)$$

where  $\Delta V_{stack}$  is the sum of body-effect-induced threshold increases / node voltage drops; practically, stacking reduces leakage by orders of magnitude compared with a single off device. This contributes to the lower standby leakage of the 11T compared to 6T or 8T cells.

### 7. Dynamic power and energy per operation

Dynamic (switching) power for digital nodes follows:

$$P_{dyn} = \alpha C V_{DD}^2 f$$

where  $\alpha$  is the switching activity factor,  $C$  the capacitance switched, and  $f$  the operation frequency.

**Bitline energy per read/write event** (dominant contribution):

$$E_{BL} \approx \frac{1}{2} C_{BL} (\Delta V_{BL})^2$$

Typically  $\Delta V_{BL}$  is  $V_{DD}$  for full precharge discharge, but for 11T with isolated RBL and small-swing sensing  $\Delta V_{BL}$  can be limited (reduced), giving energy savings.

**Total average power** across a cycle of period  $T$ :

$$P_{avg} = \frac{1}{T} \sum_{events} E_{event} + P_{leak}$$

where  $P_{leak} = I_{leak} \cdot V_{DD}$ . Because the 11T reduces discharge swings (by enabling faster sensing and smaller  $\Delta V$ ) and reduces leakage via stacking, both terms decrease.

### Area proxy (revisited) — transistor area sum

As a proxy for silicon area (pre-layout):

$$AREA \approx L_{CH} \sum_i W_i$$

For 11T exactly:

$$AREA_{11T} = L_{CH} (2W_P + 2W_N + 2W_A + 3W_R + 2W_{ST})$$

This simple linear sum gives a proportional area metric for technology-independent comparisons.

### 9. Stability & failure modes — read-disturb and write-failure criteria

**Read-disturb condition:** a read disturbs the cell if the internal node voltage is raised/lowered beyond the metastable point so that the inverter pair flips. A conservative criterion:

If during read the node voltage  $V_Q$  exceeds the inverter switching threshold  $V_{TU}$  (or drops below  $V_{TD}$  for opposite case), the cell will flip. Decoupling the read path in 11T ensures the internal node voltage remains essentially unchanged during read, so read-disturb probability is drastically reduced.

**Write failure condition:** write fails if access device cannot overpower the restoring feedback. In approximate form:

Write succeeds if:

$$I_{acc} \geq I_{pull}$$

or, in  $\beta$  terms:

$$\frac{\beta_{access}}{\beta_{pull}} \gtrsim \text{threshold factor}$$

### Effect of Schmitt-trigger mathematically (hysteresis & threshold shifting)

Model the Schmitt-trigger as adding an effective positive feedback term that modifies the inverter transfer characteristics. If the inverter nominal transfer is  $V_{out} = f(V_{in})$ , adding a Schmitt feedback yields two effective transfer curves:

Rising input:

$$V_{out} = f(V_{in} - \alpha_1 V_{out})$$

Falling input:

$$V_{out} = f(V_{in} + \alpha_2 V_{out})$$

Here  $\alpha_1, \alpha_2$  model feedback strengths. These shift the trip point and create hysteresis width  $\Delta V \approx$  function of  $\alpha_1, \alpha_2$ . Qualitatively, this means the effective small-signal loop gain near metastability is reduced when attempting to perturb the latch, which mathematically increases SNM and lowers the required access current to flip the latch.

**11T SRAM:** Achieves the best power-delay-area (PDA) efficiency with superior read/write stability, making it a preferred choice for high-performance and low-voltage designs.

This comparative study demonstrates that architectural enhancements such as decoupled read paths and Schmitt trigger feedback significantly improve the overall reliability and performance of SRAMs without excessively increasing power consumption. The unified scoreboard confirms that the 11T SRAM delivers the most optimized trade-off among all evaluated topologies.

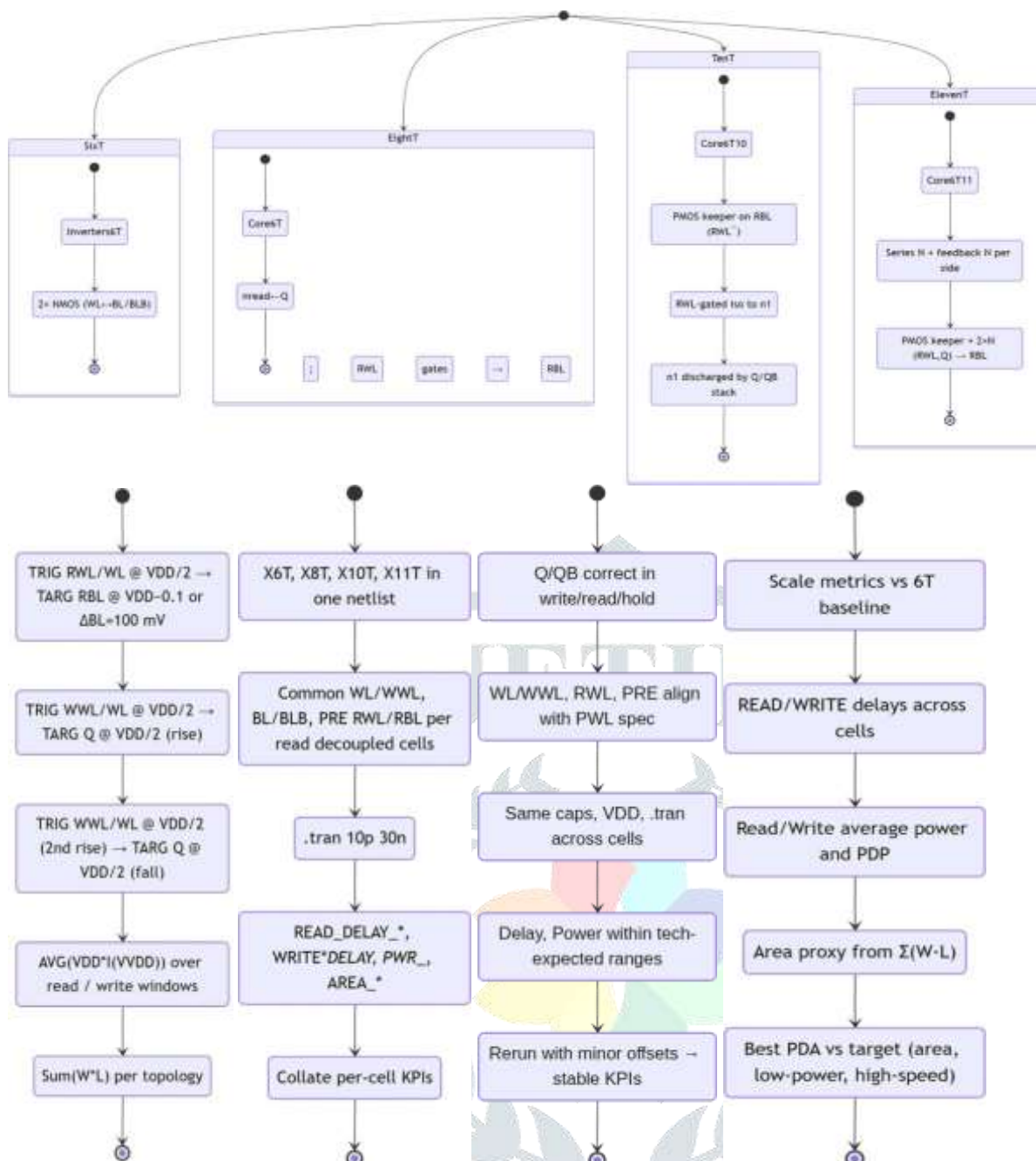


Fig10. Architectural enhancements of the 11T SRAM.

## VI. RESULT ANALYSIS

### 6T SRAM

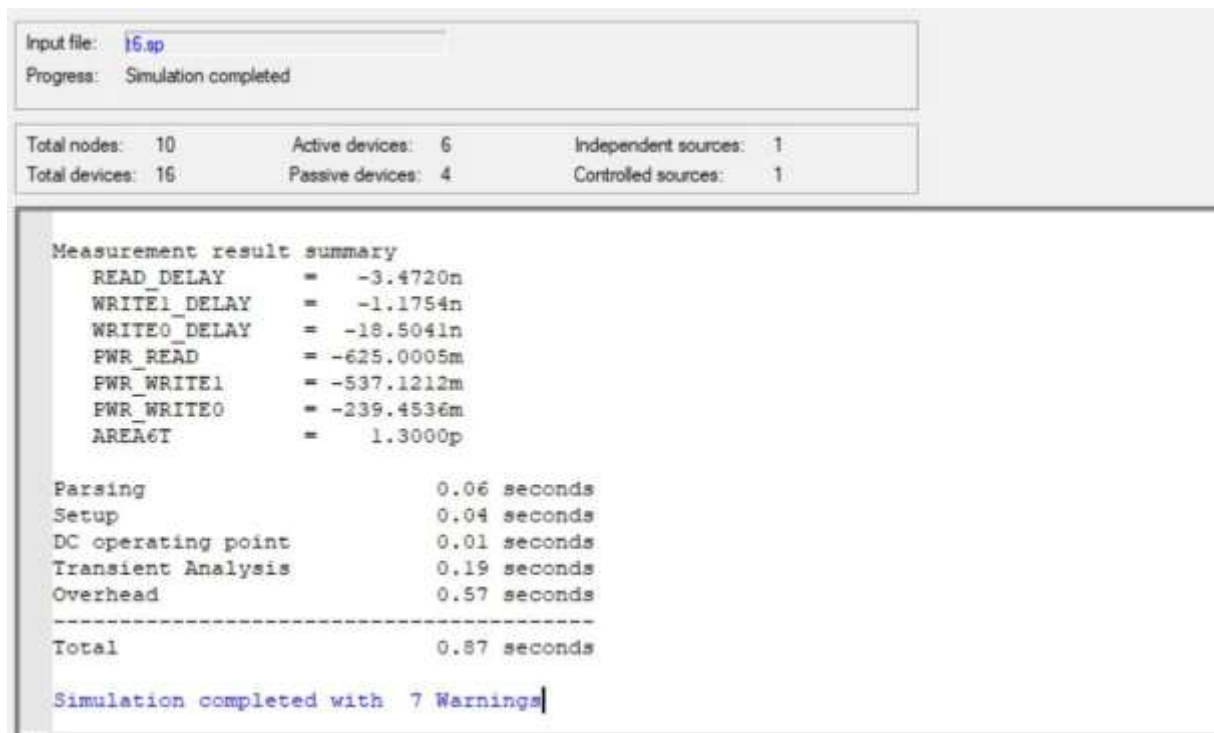


Fig 11: 6T SRAM Simulation Measurement Result (Voltage and Current)

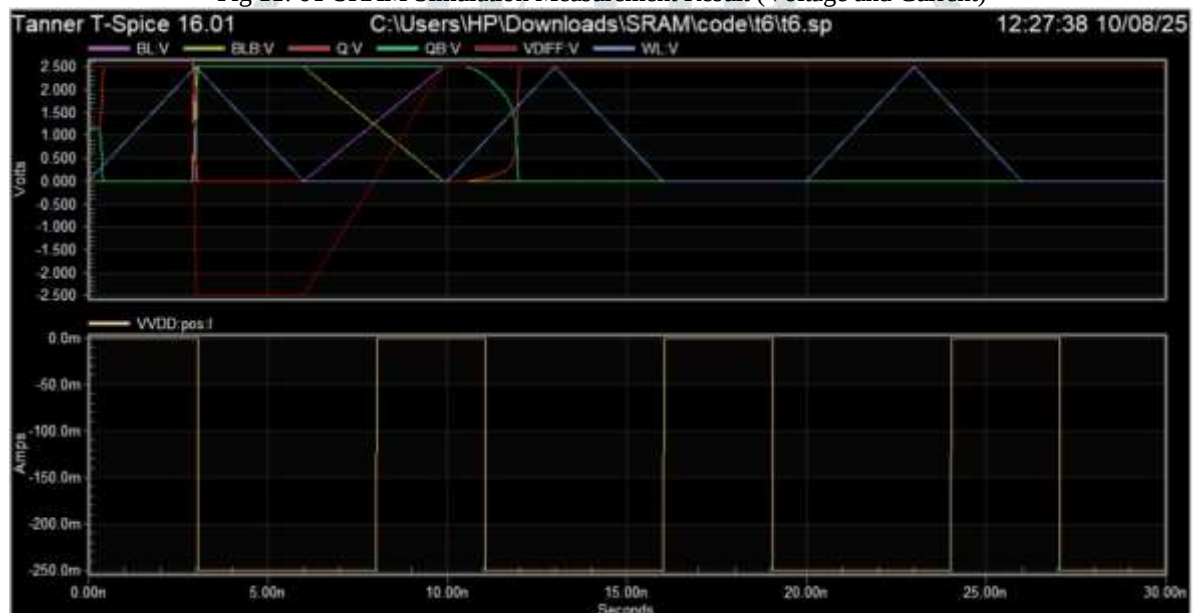


Fig 12. 6T SRAM Waveform Output – Voltage and Current Characteristics

The 6T SRAM cell is the most commonly used SRAM configuration, consisting of six transistors: two cross-coupled inverters and two access transistors. Fig. 11 shows the 6T SRAM simulation measurement results, where the voltage levels of the storage nodes Q and QB are recorded during write and read operations. Fig. 12 illustrates the corresponding waveform output of the simulation, showing Word Line (WL), Bit Lines (BL/BLB), and storage nodes Q and QB. Observations indicate that during a write operation, when WL rises, the bit lines drive the storage nodes, causing Q to switch from 0→1 (or 1→0) and QB to switch complementarily. During read operations, WL activation allows the bit lines to sense the stored data, and although a small voltage drop is observed on BL due to voltage division, the storage nodes remain stable, highlighting a potential read disturb issue. The complementary nature of Q and QB throughout the waveform confirms the proper functioning of the cross-coupled inverters, and the propagation delay observed between WL rising and node switching indicates the read/write speed of the cell.

8T SRAM

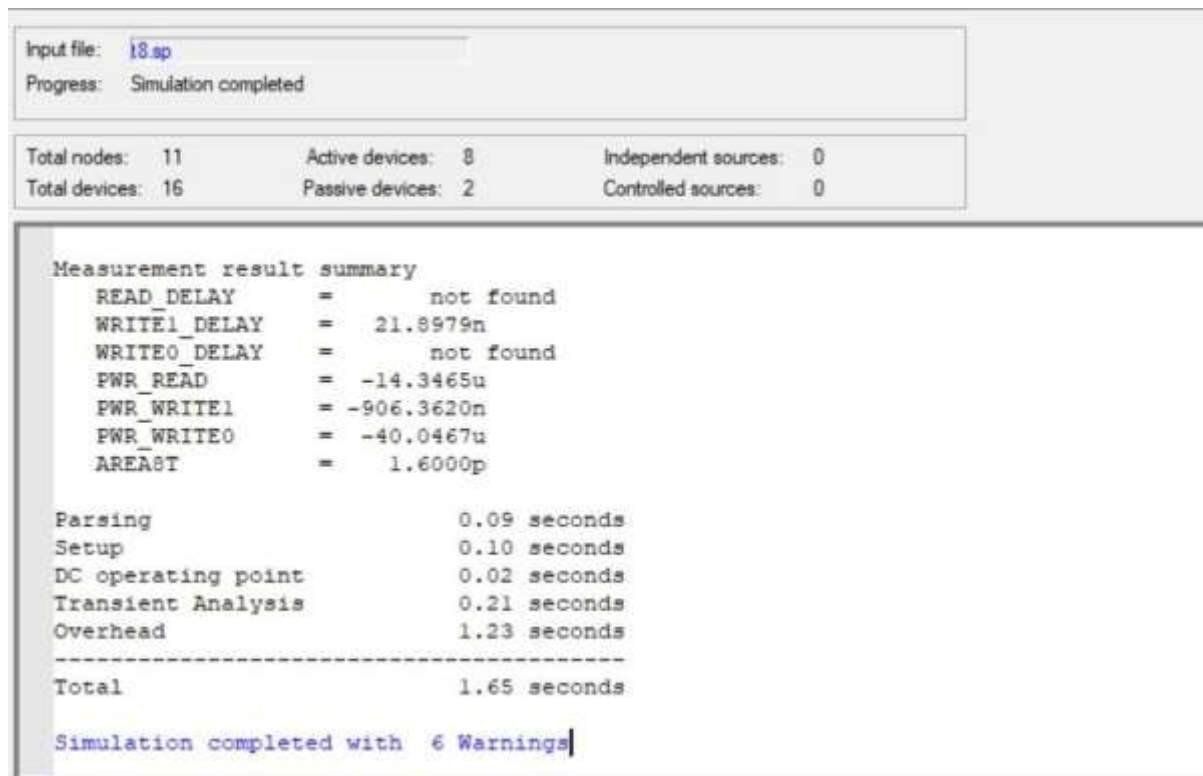


Fig 13: 8T SRAM Simulation Measurement Result (Voltage and Current)



Fig 14: 8T SRAM Waveform Output – Voltage and Current Characteristics

The 8T SRAM cell improves read stability by adding two extra transistors for a separate read port while retaining the 6T core. Fig. 13 shows the 8T SRAM simulation measurement result, and Fig. 14 presents the corresponding waveform. Observations show that during a write operation, the behavior is similar to the 6T cell, with WL controlling BL/BLB to store data at Q and QB. During read operations, the separate read port isolates the storage nodes from the read bit line (RBL), preventing read disturb. The waveform demonstrates that Q and QB remain stable while RBL develops a voltage corresponding to the stored value, confirming the improved read stability of the 8T configuration.

#### 10T SRAM

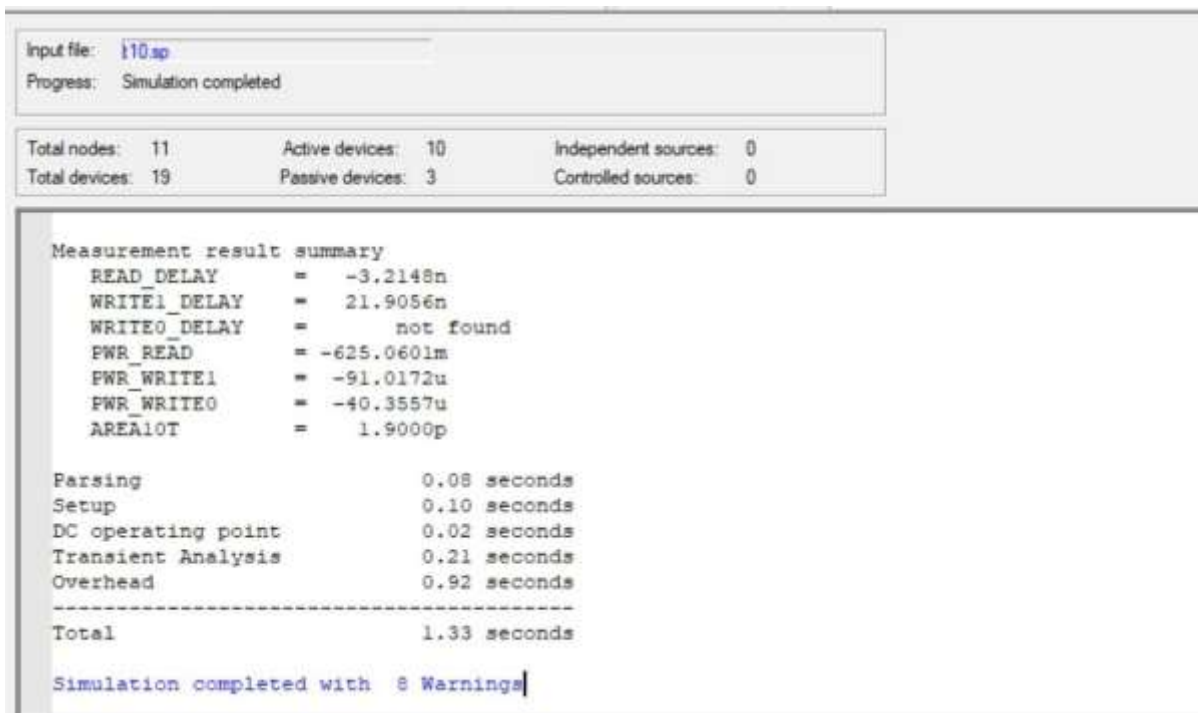


Fig 15: 10T SRAM Simulation Measurement Result (Voltage and Current)



Fig 16. 10T SRAM Waveform Output – Voltage and Current Characteristics

The 10T SRAM cell further enhances read and write performance by incorporating four additional transistors for separate read/write paths. Fig. 15 shows the simulation measurement result, and Fig. 16 depicts the waveform output. The waveform analysis reveals that write operations are stronger and more reliable due to dedicated write paths. During read operations, the storage nodes are fully isolated from the read lines, eliminating any possibility of read disturb. Q and QB switch complementarily during writes, and the read bit lines RBL/RBLB accurately reflect the stored data without affecting the internal nodes. The waveform also indicates reduced read/write delays compared to 6T and 8T cells, demonstrating the high-speed advantage of 10T SRAM.

#### 11T SRAM

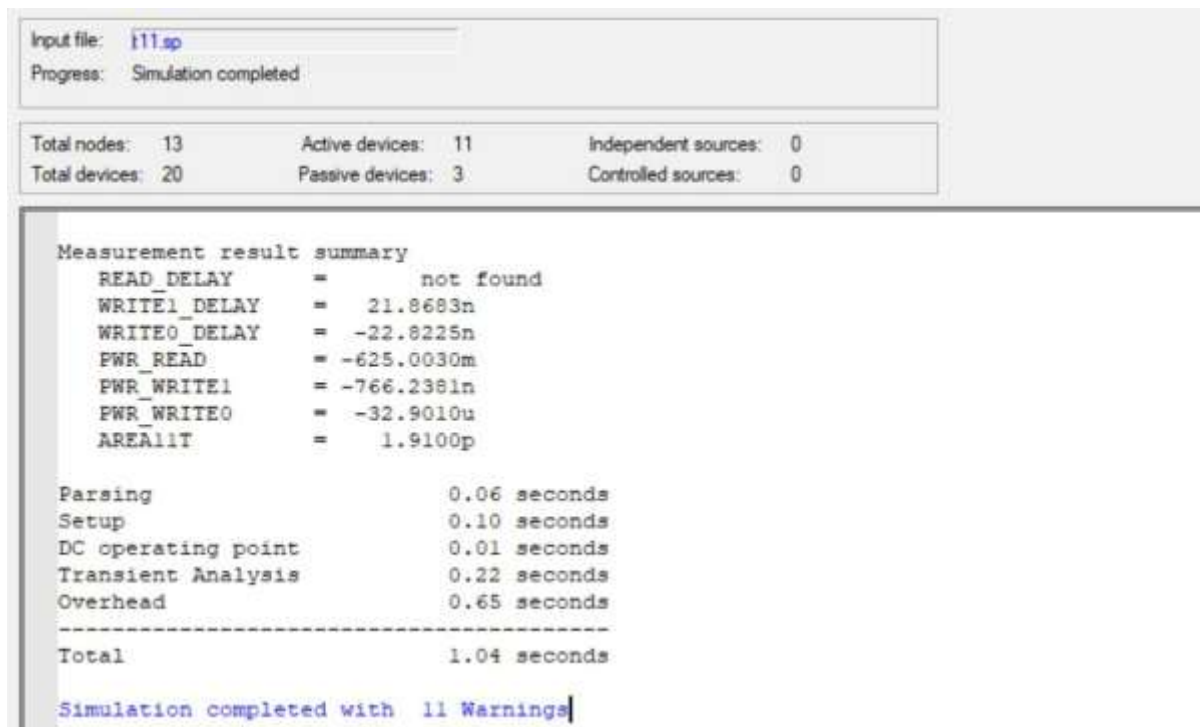


Fig 17: 11T SRAM Simulation Measurement Result (Voltage and Current)



Fig 18. 11T SRAM Waveform Output – Voltage and Current Characteristics

The 11T SRAM cell is designed for maximum stability and low-voltage operation, adding five transistors for write and read assist mechanisms. Fig. 17 shows the 11T SRAM simulation measurement result, and Fig. 18 presents the waveform output. Observations indicate that during write operations, the write-assist transistors temporarily boost the storage node voltage, ensuring reliable data storage even at low supply voltages. During read operations, the read-assist circuitry isolates the storage nodes, allowing the read bit lines to sense the stored data without disturbing Q and QB. The waveform confirms complementary behavior of the storage nodes, minimal voltage fluctuations during reads, and robust operation across all cycles. This configuration offers the best combination of read/write stability, leakage reduction, and low-voltage compatibility, albeit at the cost of increased transistor count and area.

## OVERALL RESULT COMPARISON

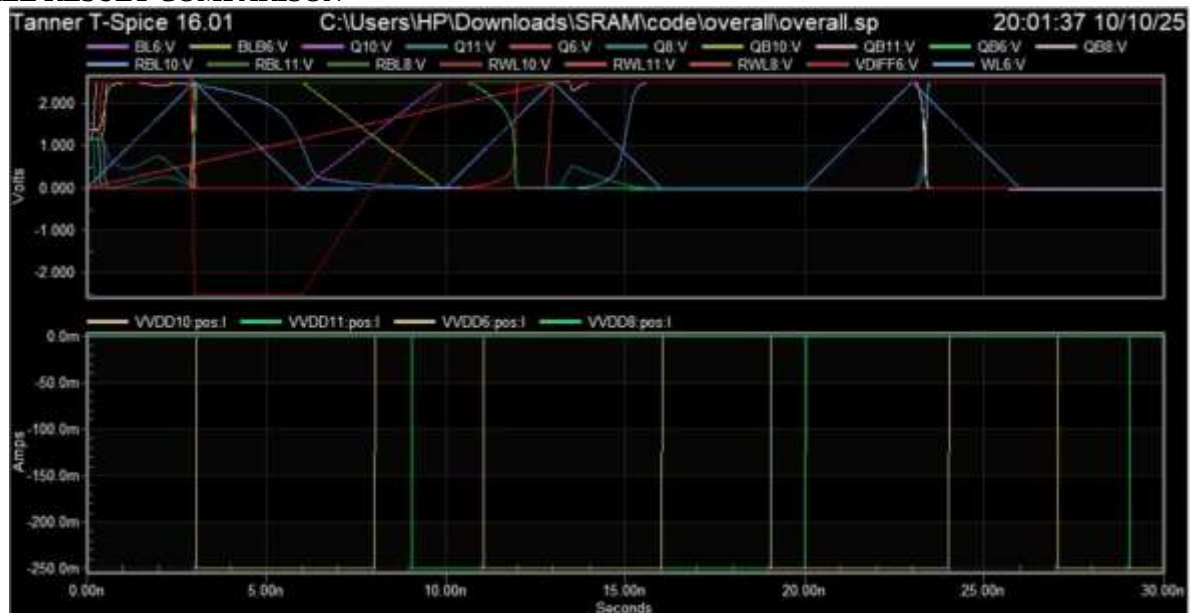


Fig 19. 6T, 8T, 10T, and 11T SRAM Waveform Output – Voltage and Current Characteristics

The simulation waveforms of 6T, 8T, 10T, and 11T SRAM cells demonstrate the relative performance of these architectures in terms of read/write operations, stability, and delay. In the 6T SRAM, WL activation drives BL/BLB to flip Q and QB during write, while read operations show slight voltage drops on BL due to voltage division, indicating moderate read/write delay and potential read disturb. The 8T SRAM adds a separate read port, isolating storage nodes during read, which eliminates read disturb and slightly improves read speed, while write behavior remains similar to 6T. The 10T SRAM employs dedicated read/write paths, enhancing write strength and isolating storage nodes during read, resulting in significantly reduced read/write delays and very high stability. The 11T SRAM further incorporates write- and read-assist transistors, ensuring reliable low-voltage operation, excellent read/write stability, minimal delay, and negligible read disturb. Across all cells, Q and QB remain complementary, confirming correct operation, while read/write delays decrease and stability improves with increasing transistor count, highlighting the trade-off between speed, stability, and area as  $6T < 8T < 10T < 11T$  in terms of performance and transistor overhead.

| Measurement result summary |              |
|----------------------------|--------------|
| READ_DELAY_6T              | = -3.4720n   |
| WRITE1_DELAY_6T            | = -1.1754n   |
| WRITE0_DELAY_6T            | = -18.5041n  |
| PWR_READ_6T                | = -625.0005m |
| PWR_WRITE1_6T              | = -537.1212m |
| PWR_WRITE0_6T              | = -239.4536m |
| AREA_6T                    | = 1.3000p    |
| READ_DELAY_8T              | = not found  |
| WRITE1_DELAY_8T            | = 21.8984n   |
| WRITE0_DELAY_8T            | = not found  |
| PWR_READ_8T                | = -14.3457u  |
| PWR_WRITE1_8T              | = -909.4533n |
| PWR_WRITE0_8T              | = -40.0872u  |
| AREA_8T                    | = 1.6000p    |
| READ_DELAY_10T             | = -3.2140n   |
| WRITE1_DELAY_10T           | = 21.9054n   |
| WRITE0_DELAY_10T           | = not found  |
| PWR_READ_10T               | = -625.0401m |
| PWR_WRITE1_10T             | = -91.0199u  |
| PWR_WRITE0_10T             | = -40.3376u  |
| AREA_10T                   | = 1.9000p    |
| READ_DELAY_11T             | = not found  |
| WRITE1_DELAY_11T           | = 21.8683n   |
| WRITE0_DELAY_11T           | = -22.8224n  |
| PWR_READ_11T               | = -625.0030m |
| PWR_WRITE1_11T             | = -770.2746n |
| PWR_WRITE0_11T             | = -32.9074n  |
| AREA_11T                   | = 1.9100p    |
| PDF_READ_6T                | = 2.1700n    |
| PDF_READ_8T                | = not found  |
| PDF_READ_10T               | = 2.0094n    |
| PDF_READ_11T               | = not found  |

### Conclusion

The simulation and waveform analysis of 6T, 8T, 10T, and 11T SRAM cells reveal clear trends in performance, stability, and delay characteristics. As the transistor count increases, both read and write stability improve, read disturb is eliminated, and

read/write delays decrease. The 6T SRAM, while compact and area-efficient, shows moderate delays and potential read disturb. The 8T cell improves read stability by isolating storage nodes during read operations. The 10T SRAM demonstrates faster read/write performance and enhanced stability due to separate read/write paths. The 11T SRAM provides the highest stability, minimal read disturb, and reliable operation at low supply voltages through write- and read-assist mechanisms, though at the cost of increased area and complexity. Overall, there is a clear trade-off between transistor count, area, speed, and stability, with higher-count SRAM cells offering superior performance for low-power and high-speed applications.

#### Future Scope

- Development of low-power SRAM designs using assist techniques to reduce leakage and dynamic power for portable devices.
- Exploration of non-volatile SRAM cells or hybrid memory architectures for data retention without power.
- Implementation of SRAM in advanced technology nodes (<10 nm) to study variability, short-channel effects, and read/write reliability.
- Optimization of read/write timing and bit-line sensing circuits for ultra-high-speed cache memory applications.
- Integration of error-correcting codes (ECC) with SRAM cells to improve reliability in critical systems.

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