



A CLOSED LOOP TEMPERATURE COMPENSATED FULLY TRIMMABLE ON-CHIP IC OSCILLATOR

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ABSTRACT

This project focuses on a design and simulation of an IC oscillator including a temperature compensation circuitry, a robust spread reduction technique and 8-bit digital trimming is described. The work begins by reviewing a baseline 3.3 MHz oscillator implemented in 65nm CMOS technology, which utilizes an analog 1.2 voltage bandgap reference for temperature and supply compensation, achieving a frequency stability in between temperature of -40°C to 125°C.

KEYWORDS: Voltage Reference circuit, Comparator, Latch, Differential amplifier, Closed loop 8-bit Digital Trimming circuit, ADC Circuit, Cadence, CMOS technology.

1. INTRODUCTION

On-chip integrated circuit (IC) oscillators serve as the fundamental clock source for virtually all digital systems. As electronic devices become more complex and integrated, the demands on these oscillators for accuracy, stability, and low power consumption continue to increase. Maintaining a stable and precise clock signal is a significant challenge due to a variety of factors, including wide operating temperature ranges, fluctuations in the power supply, and variations inherent in the manufacturing process.

The purpose of this report is to detail the design and performance of a temperature-compensated, on-chip IC. A popular method for realizing digital-output VCOs in CMOS technology is a subclass of the CMOS relaxation oscillator family, the constant-current charge and discharge type or IC oscillator where current sources are used to charge and discharge the timing capacitor and the output frequency is inversely proportional to the capacitor value. One of the most important considerations when designing an IC oscillator is its frequency stability with temperature. The frequency steadiness depends basically on: (i) the internal current sources variation with temperature; (ii) the voltage reference drift across the temperature range; (iii) the comparator offset voltage and bias current deviations due to temperature changes; (iv) the temperature coefficient of switching delays of the comparator and latch; and (v) the capacitor variation with process, voltage and temperature oscillator. This document first outlines an existing design, a 12.8 MHz relaxation oscillator that employs analog compensation and digital trimming to achieve a frequency stability of less than ±5%. It then proposes a series of significant enhancements to this architecture.

The proposed method incorporates key circuit upgrades, including high-speed Strong-Arm Latch comparators and a higher-gain differential amplifier, and integrates them into a sophisticated hybrid closed-loop control system. This advanced architecture utilizes an 8-bit Analog-to-Digital Converter (ADC) for both coarse and fine frequency tuning, enabling dynamic, real-time control. This approach aims to demonstrate superior performance in terms of precision, noise immunity, and programmability, providing a clear pathway for designing robust and scalable clock sources for next-generation System-on-Chip (SoC) applications.

2. IC OSCILLATOR DESIGN

The SR latch is in its reset state and transistor M1 is off whereas transistor M2 is on, maintaining C2 discharged. In this state the constant current I_{ch1} charges linearly the timing capacitor C1 until the voltage V_{c1} across C1 reaches V_{bg} , the band gap reference voltage. Then the comparator cmp 1 output goes to high and set the SR latch turning M1 on and M2 off. When M1 is on, C1 is very quickly discharged and the linear charge of C2 starts. After V_{c2} attains V_{bg} , the cmp2 output clears the SR latch turning M1 off and M2 on and driving the circuit to its initial state. This completes one period of oscillator and the process begins again. Disregarding switching delays of comparators, latch and transistors M1-M2, and assuming that $I_{ch1} = I_{ch2} = I_{ch}$ and $C1 = C2 = C$, the oscillator frequency is

$$f = \frac{1}{2} \left(\frac{1}{V_{bg}} \right) \left(\frac{I_{ch}}{C} \right)$$

The complete circuit design with all the components such as voltage reference circuit, band gap voltage circuit, differential amplifier, comparators, latch, 8-bit trimming circuit as shown below fig.

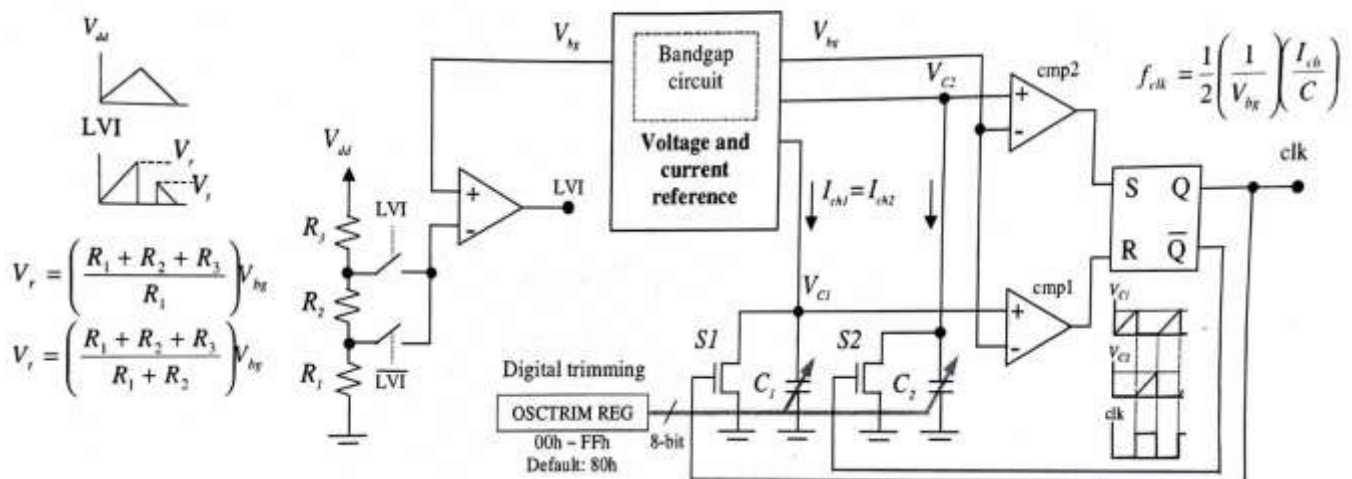


Fig.1.IC Oscillator Block Diagram

3.DESIGN AND IMPLEMENTATION:

The proposed design enhances the core oscillator and integrates a comprehensive digital control feedback loop. The primary functional blocks are the Strong-Arm Latch Comparator, the High-Gain Voltage Reference, and the Hybrid 8-bit Control System (ADC and Digital Coder).

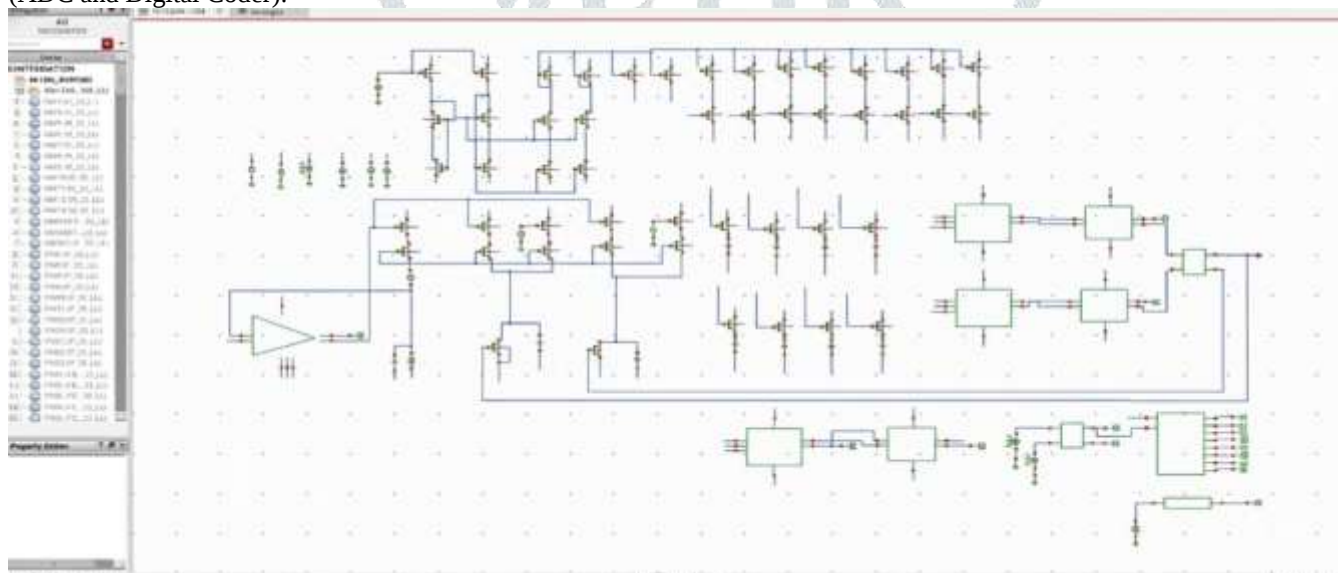


Fig.2. IC oscillator schematic

3.1 Strong-Arm Latch Comparator

The static comparators in the baseline design were replaced with a high-speed, low-offset **Strong-Arm Latch comparator** to minimize jitter and improve timing precision.

Switching Operation: The comparator functions in two phases controlled by the clock signal (ϕ). In the **Pre-charge Phase** (ϕ low), the outputs are reset to a high voltage. In the **Evaluation Phase** (ϕ high), the latch provides positive feedback, rapidly amplifying the small differential input voltage (V_{in+} vs. V_{in-}). The simulation confirms this rapid switching action is key to generating a clean, sharp clock edge.

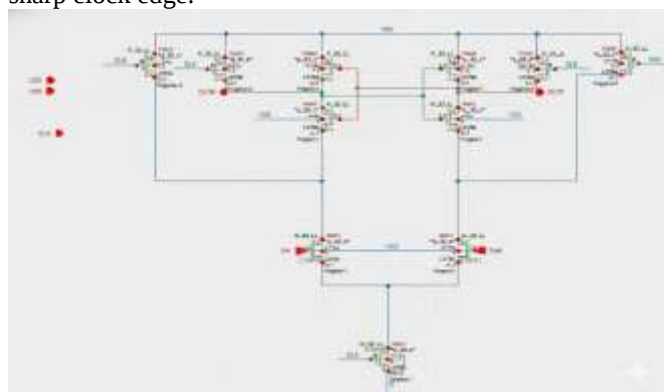


Fig.3.1.a. Comparator schematic

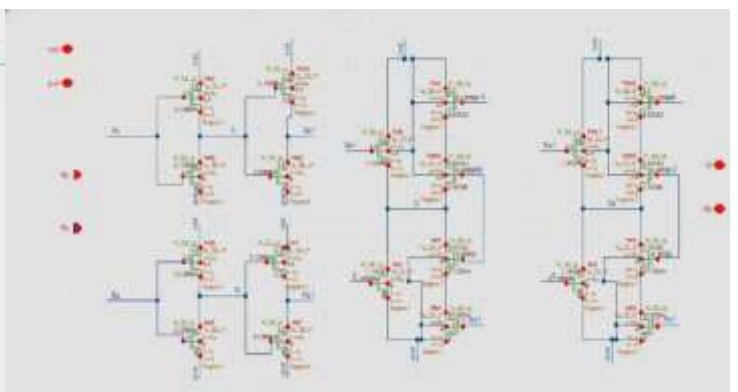


Fig.3.1.b. latch schematic

3.2. High-Gain Voltage Reference Circuit

The frequency stability of the oscillator relies heavily on a precise and temperature-independent charging current, which is derived from the voltage reference.

Bandgap Principle: The core circuit utilizes the bandgap principle, combining a voltage with a **Negative Temperature Coefficient (NTC)** (e.g., VBE) and a voltage with a **Positive Temperature Coefficient (PTC)** (e.g., voltage proportional to absolute temperature). The scaled sum of these two opposing coefficients results in a stable reference voltage, crucial for maintaining frequency from -40°C to 125°C .

Differential Amplifier: The differential amplifier in your circuit is the core of the **voltage reference circuit**. Its primary function is to create a highly accurate and stable reference voltage that does not change with temperature or power supply variations. This stable voltage is crucial for your oscillator because it controls the charging current of the timing capacitors, which directly determines the oscillation frequency.

The amplifier in your design is a **two-stage operational amplifier**, a common and effective topology for achieving high gain.

How the Amplifier Works and design

First Stage: This is the input stage, a differential pair. It takes two input signals and amplifies the **difference** between them. This stage provides the initial gain and converts the differential signal into a single-ended output.

Second Stage: This stage provides the majority of the voltage gain. It takes the output from the first stage and further amplifies it to achieve the total high gain of the amplifier.

To ensure the circuit doesn't become unstable or oscillate, a **Miller compensation capacitor** is added between the two stages. This capacitor is essential for stabilizing the amplifier's frequency response, guaranteeing a clean and reliable output. The schematic diagram of the differential amplifier as shown in the below fig in this circuit Inp, Inm are the input pins which is connected to the vcas and pcas which gives high gain of 90db by changing the multipliers and fingers in the transistors in the circuit diagram.

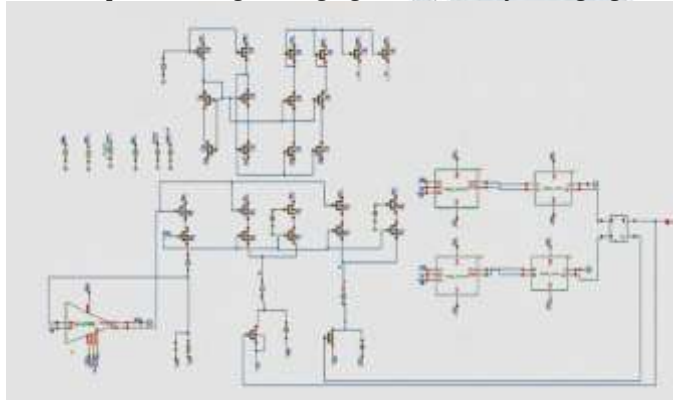


Fig.3.2.a. Voltage Reference circuit schematic

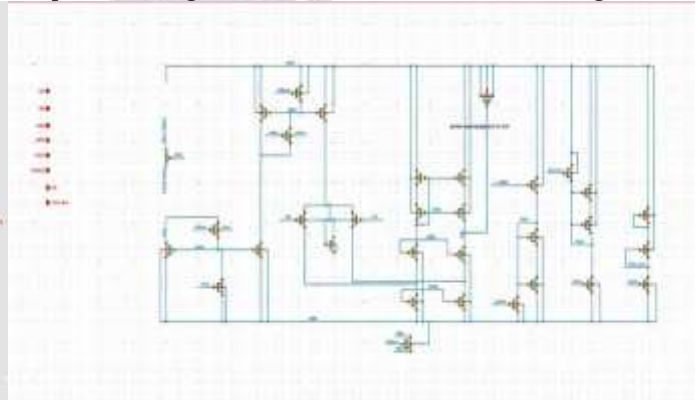


Fig3.2.b. Two stage Differential Amplifier schematic

3.3 Hybrid Closed-Loop Control System

The control system replaces the static digital trimming with dynamic, real-time feedback via an 8-bit ADC.

8-bit ADC Use: The ADC continuously monitors an analog signal proportional to the oscillator's output frequency and converts it into a fresh 8-bit digital word. This digital output provides a measurement of the instantaneous frequency error.

Digital Coder and Hybrid Tuning: This 8-bit word is processed by a digital coder (DAC-based) to implement the hybrid tuning strategy:

Coarse Tuning (MSBs): The Most Significant Bits (MSBs) are used for large adjustments, primarily to control the oscillator's reference voltage. This provides a **wide tuning range** to compensate for large process variations.

Fine Tuning (LSBs): The Least Significant Bits (LSBs) are used for small, precise adjustments, typically controlling a digitally-switched capacitor array. This provides the **high resolution** necessary to precisely lock the frequency to the target value.

This can be achieved using Time sequence word- time generator. the word-time signal to be generated must stay on for a period of 256 clock pulses. a counter circuit that accomplishes this task as shown in the figure3.3. 38-bit counter is cleared to 0. A start signal will set d flip-flop . The schematic of the word- time generator by using the RS flipflop, d counter the output clk is given as input to this circuit and generate outputs as D0,D1,D2,D3,D4,D5,D6,D7

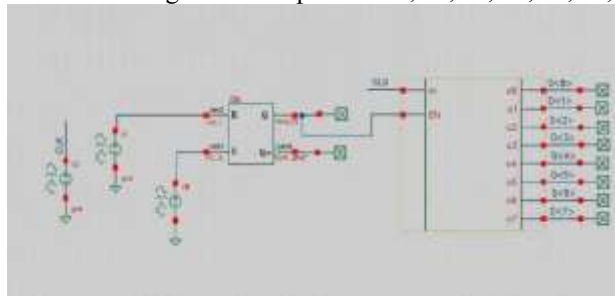


Fig.3.3.a. Word-time generator schematic

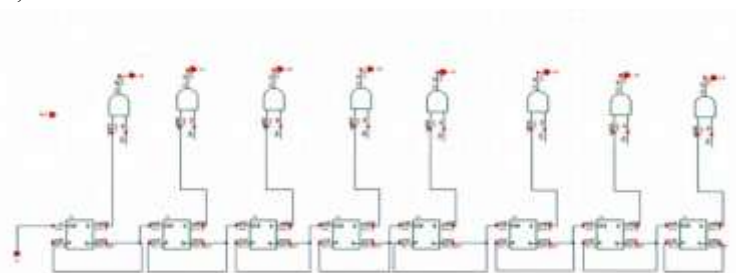


Fig.3.3.b. D-counter schematic

4. Design Parameter:

The proposed circuit was designed and simulated using cadence virtuoso with spectre simulation. The simulation employed the 65nm cmos technology with proper design parameters given below.

DESIGN PARAMETERS	VALUES
VDD	3.3
GAIN	1K
VCONTROL	3.3
IDC	10u
C	0

Va	0-256
Tclk	8u
Tdelay	10u

5.SIMULATION AND RESULTS

The simulation aimed to validate the theoretical behavior of the comparator, voltage reference circuit, differential amplifier, closed loop control system. The output of your temperature compensation circuit is the core of your oscillator's stability. It's a key part of the project, especially for operating from -40°C to 125°C . The circuit achieves this stability by expertly combining two types of components: those with a positive temperature coefficient and those with a negative one. By the cancelling the positive and negative feedback we get stability in the temperature.

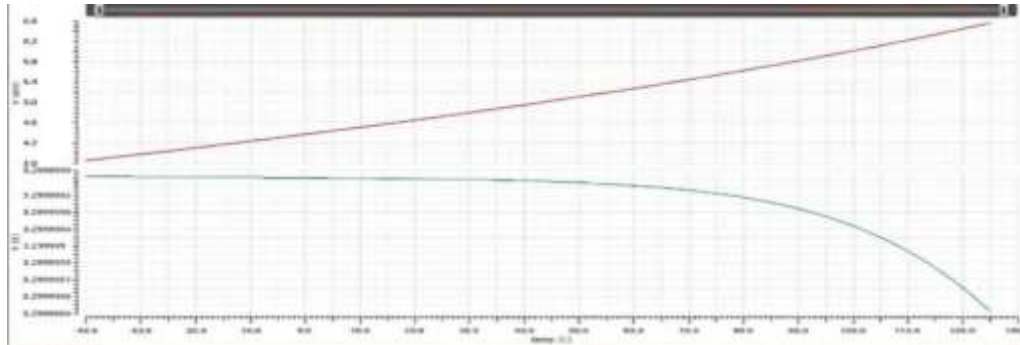


Fig.5.a. Temperature Coefficient plot (DC analysis)

The differential amplifier's output is crucial for confirming its high-performance characteristics. The plot shows the amplifier's output voltage versus time. The key takeaway from this graph is the extremely stable, near-flat DC voltage. Despite any potential noise or fluctuations on the power supply, the high **90dB gain** ensures that the output voltage remains constant. This high gain is what allows the amplifier to reject any noise, resulting in an output voltage with minimal ripple. This stable reference voltage is essential for ensuring the oscillator's frequency does not fluctuate due to variations in the power supply, thus contributing significantly to the overall stability of your system. The phase also shown below

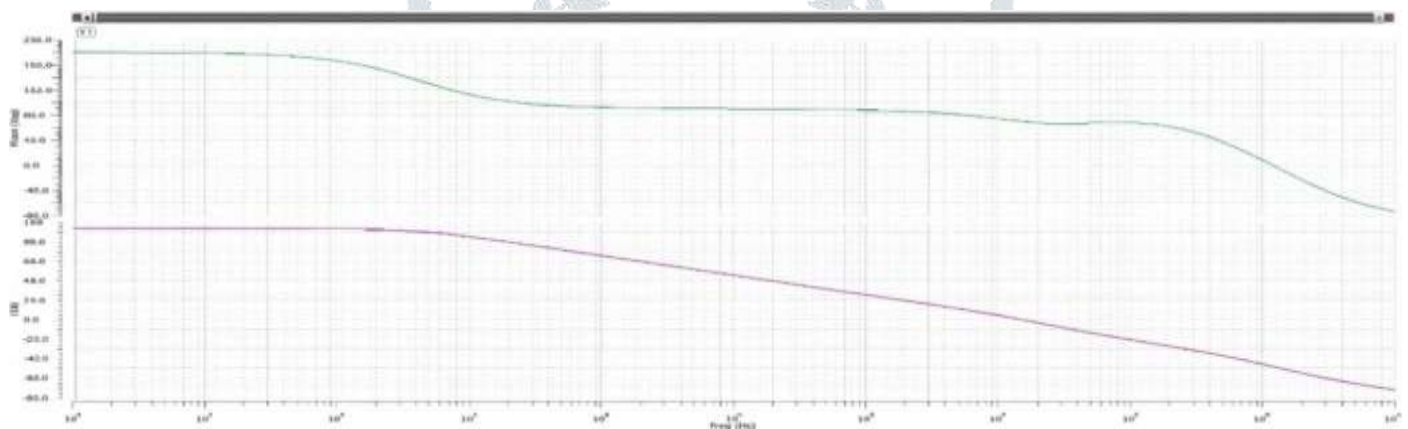


Fig.5.b. Frequency Response (AC analysis) plot from a differential amplifier circuit simulation

To ensure proper timing and hold the comparator's output for a specific duration at 1.2volts, an additional latch circuit is connected to the comparator's output. This circuit acts as a buffer and provides a clean, stable digital signal to the rest of the system and the transient analysis of the complete circuit as shown the below.

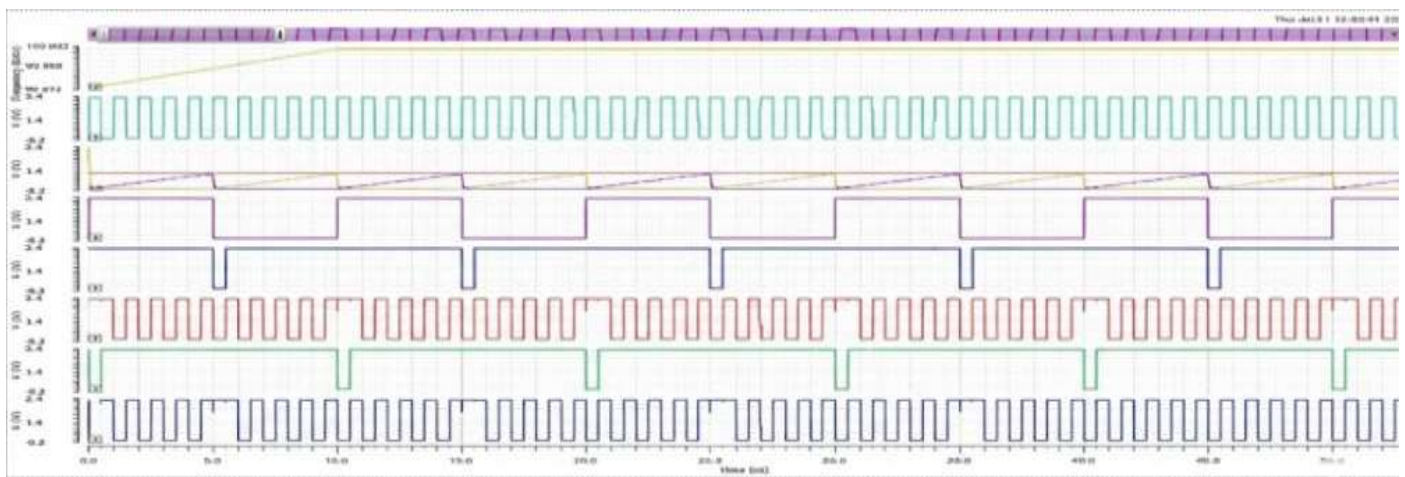


Fig.5.c. Transient Response plot from a circuit simulation

The plot, with the digital control input on the x-axis and frequency on the y-axis, shows a clear and predictable relationship. The distinct steps in the frequency curve demonstrate the wide tuning range provided by the MSBs (coarse tuning) and the small, granular steps within each of those large steps, which are a result of the LSBs (fine tuning). This simulation confirms that the hybrid tuning scheme successfully provides both the wide range needed to lock onto a target frequency and the high resolution required for precision. When we are changing the values of V_a from the 0 to 256 as we are using it 8-bit counter we get the frequency plot by using parametric analysis as shown in below.

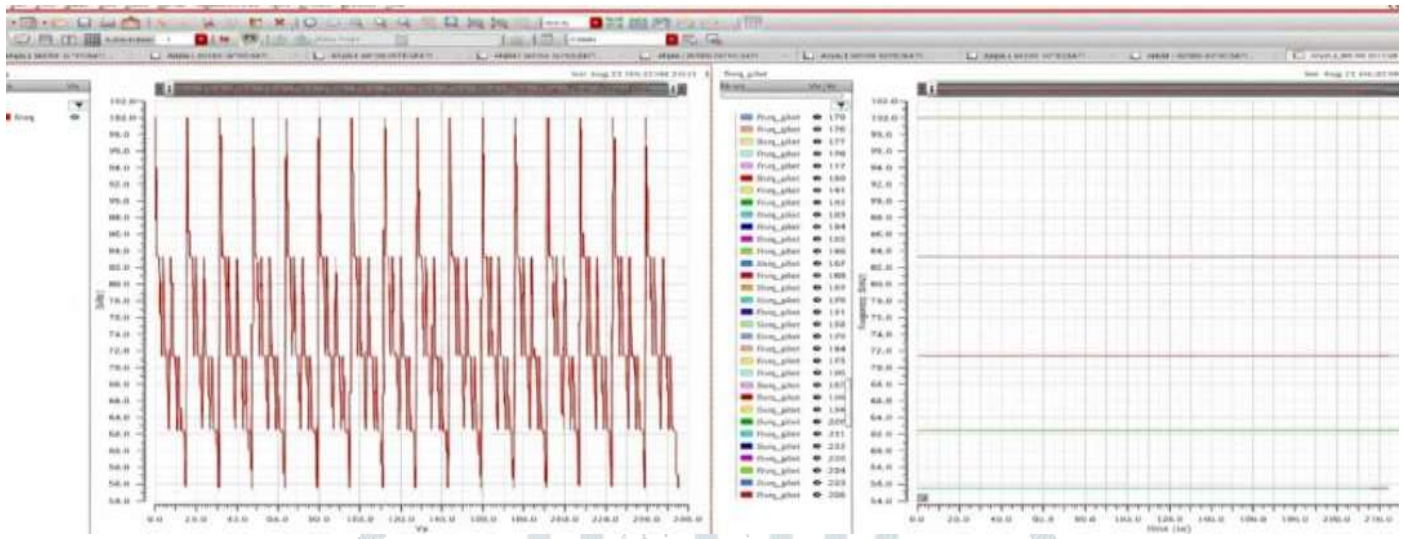


Fig.5.d.Parametric frequency response plot from a circuit simulation

5. CONCLUSION

The study has detailed the design and proposed improvements for a temperature-compensated, on-chip IC oscillator. By replacing the static comparators with high-speed Strong-Arm Latch comparators, upgrading the voltage reference with a high-gain differential amplifier, and, most importantly, implementing a novel hybrid closed-loop tuning system with an 8-bit ADC, the oscillator's performance has been significantly enhanced. The proposed design provides real-time, dynamic frequency control that is superior to the static trimming used in the baseline design. This advancement results in improved frequency stability, lower phase noise, and a more robust and programmable clock source suitable for next-generation SoC applications. Future work may focus on implementing a more complex control algorithm to further reduce jitter and exploring different CMOS technologies for further performance and power efficiency gains.

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