JETIR.ORG ISSN: 2349-5162 | ESTD Year : 2014 | Monthly Issue
JOURNAL OF EMERGING TECHNOLOGIES AND INNOVATIVE RESEARCH (JETIR)
An International Scholarly Open Access, Peer-reviewed, Refereed Journal

A SENSE-AMPLIFIER-BASED FLIP-FLOP (SAFF) SUITABLE FOR LOW-POWER HIGH-SPEED OPERATION

[1]Guduru Vishnu Pranav Teja,[2]Dr Sreenivasulu P, [3]Prasad Rao Mangalapuri
[1]M.tech Scholar, Dept. Of ECE,Audisankara College of Engineering and Technology, Gudur, Andhra Pradesh
[2] Professor, Dept. Of ECE, Audisankara College of Engineering and Technology, Gudur, Andhra Pradesh
[3] Assistant Professor, Dept. Of ECE,Audisankara College of Engineering and Technology, Gudur, Andhra Pradesh

Abstract: In this paper, a sense-amplifier-based flip-flop (SAFF) suitable for low-power high-speed operation is proposed. With the employment of a new sense-amplifier stage as well as a new single-ended latch stage, the power and delay of the flip-flop is greatly reduced. A conditional cut-off strategy is applied to the latch to achieve glitch-free and contention-free operation. Furthermore, the proposed SAFF can provide low voltage operation by adopting MTCMOS optimization. Post-layout simulation results based on a SMIC 55 nm MTCMOS show that the proposed SAFF achieves a 41.3% reduction in the CK-to-Q delay and a 36.99% reduction in power (25% input data toggle rate) compared with the conventional SAFF. Additionally, the delay and the power are smaller than those of the master-slave flip-flop (MSFF). The power-delay-product of the proposed SAFF shows 2.7× and 3.55× improvements compared with the conventional SAFF and MSFF, respectively. The area of the proposed flip-flop is 8.12 µm2 (5.8 µm × 1.4 µm), similar to that of the conventional SAFF. With the employment of MTCMOS optimization, the proposed SAFF could provide robust operation even at supply voltages as low as 0.4 V.

1. Introduction

High speed and low power is the theme of digital circuits. As basic storage elements, the delay and power of the flip-flops directly determines the performance and power of digital systems. As described in [1], flip-flops contribute a significant portion of the power consumption of the digital system. Moreover, the setup-time and CK-to-Q delay of the flip-flop directly affects the maximum clock frequency of the system. Therefore, optimizing the delay and power of flip-flops can directly improve the performance and reduce the power consumption of digital systems. The most commonly used flip-flop in digital systems is the master–slave flip-flop (MSFF). The schematic of the C2MOS [2] master-slave flip-flop in the SMIC 55 nm standard cell library provided by the foundry is shown in Figure 1. As shown in Figure 1, the data should pass through the first latch before the rising edge of CK, which ensures that the flip-flop can capture the correct data at the rising edge of CK. Therefore, the setup time in the MSFF is relatively long. At the same time, the CK-to-Q delay involves several logics and is also relatively large.

The pulse-triggered flip-flop (PFF) has been considered to be a kind of fast flip-flop. Several PFFs have been proposed in previous work [3–6]. PFF is

composed of a single latch and a clock pulse generator. The data in the PFF could be captured right after the rising edge of CK, and the setup time of the PFF is decreased to near-zero or negative. The main trouble with the PFF is the determination of the clock pulse width. A too narrow pulse width cannot guarantee the accuracy of the captured data, while a long pulse width will increase the hold time. Since the PFF should be able to work correctly at different temperatures and corners, the longest pulse width should be applied to the PFF, and the hold time of PFF is increased. This so-called sizing problem limits the application of the PFF. The sense-amplifier-based flip-flop (SAFF), first appearing in [7], is another fast flip-flop with a near-zero or negative setup time. The SAFF is composed of a sense-amplifier (SA) stage and a slave latch. The SA stage could capture the data right after the rising edge of CK, and the output of the SA stage could be maintained during the positive half cycle of CK. Thus, the sizing problem in the PFF is removed. With a near-zero or negative setup time and a reduced hold time, the SAFF is a good candidate to substitute MSFF in the standard cell library for high-speed design. Even though these features are attractive, the SAFF has several problems. The pre-charge operation of the SAFF will increase power consumption, and a fast latch structure is needed to reduce the CK-to-Q delay. Moreover, the low voltage operation problem in the conventional SAFF should be resolved to guarantee that the SAFF can be applied to low voltage designs

LITERATURE SURVEY:

A 200 MHz 13 mm/sup 2/ 2-D DCT macrocell using sense-amplifying pipeline flip-flop scheme

The two-dimensional discrete cosine transform (2D DCT) has been widely recognized as a key processing unit for image data compression/decompression. In this paper, the implementation of a 200 MHz 13.3 mm/sup 2/ 8/spl times/8 2-D DCT macrocell capable of HDTV rates, based on a direct realization of the DCT, and using distributed arithmetic is presented. The macrocell, fabricated using 0.8 /spl mu/m base-rule CMOS technology and 0.5 /spl mu/m MOSFET's, performs the DCT processing with 1 sample-(pixel)-per-clock throughput. The fast speed and small area are achieved by a novel sense-amplifying pipeline flip-flop (SA-F/F) circuit technique in combination with nMOS differential logic. The SA-F/F, a class of delay flip-flops, can be used as a differential synchronous sense-amplifier, and can amplify dual-rail inputs with swings lower than 100 mV. A 1.6 ns 20 bit carry skip adder used in the DCT macrocell, which was designed by the same scheme, is also described. The adder is 50% faster and 30% smaller than a conventional CMOS carry look ahead adder, which reduces the macrocell size by 15% compared to a conventional CMOS implementation.

A 160-MHz, 32-b, 0.5-W CMOS RISC microprocessor

This paper describes a 160 MHz 500 mW 32 b StrongARM(R) microprocessor designed for low-power, low-cost applications. The chip implements the ARM(R) V4 instruction set and is bus compatible with earlier implementations. The pin interface runs at 3.3 V but the internal power supplies can vary from 1.5 to 2.2 V, providing various options to balance performance and power dissipation. At 160 MHz internal clock speed with a nominal Vdd of 1.65 V, it delivers 185 Dhrystone 2.1 MIPS while dissipating less than 450 mW. The range of operating points runs from 100 MHz at 1.65 V dissipating less than 300 mW to 200 MHz at 2.0 V for less than 900 mW. An on-chip PLL provides the internal clock based on a 3.68 MHz clock input. The chip contains 2.5 million transistors, 90% of which are in the two 16 kB caches. It is fabricated in a 0.35-/spl mu/m three-metal CMOS process with 0.35 V thresholds and 0.25 /spl mu/m effective channel lengths. The chip measures 7.8 mm/spl times/6.4 mm and is packaged in a 144-pin plastic thin quad flat pack (TQFP) package.

Improved sense-amplifier-based flip-flop: design and measurements

Design and experimental evaluation of a new sense-amplifier-based flip-flop (SAFF) is presented. It was found that the main speed bottleneck of existing SAFF's is the cross-coupled set-reset (SR) latch in the output stage. The new flip-flop uses a new output stage latch topology that significantly reduces delay and improves driving capability. The performance of this flip-flop is verified by measurements on a test chip implemented in 0.18 /spl mu/m effective channel length CMOS. Demonstrated speed places it among the fastest flip-flops used in the state-of-the-art processors. Measurement techniques employed in this work as well as the measurement set-up are discussed in this paper.

A novel high-speed sense-amplifier-based flip-flop

A new sense-amplifier-based flip-flop is presented. The output latch of the proposed circuit can be considered as an hybrid solution between the standard NAND-based set/reset latch and the NC-/sup 2/MOS approach. The proposed flip-flop provides ratioless design, reduced short-circuit power dissipation, and glitch-free operation. The simulation results, obtained for a 0.25-/spl mu/m technology, show improvements in the clock-to-output delay and the power dissipation with respect to the recently proposed high-speed flip-flops. The new circuit has been successfully employed in a high-speed direct digital frequency synthesizer chip, highlighting the effectiveness of the proposed flip-flop in high-speed standard cell-based applications.

Sense-Amplifier-Based Flip-Flop With Transition Completion Detection for Low-Voltage Operation

A novel high-speed and highly reliable sense-amplifier-based flip-flop with transition completion detection (SAFF-TCD) is proposed for low supply voltage (V_{DD}) operation. The SAFF-TCD adopts the internally generated detection signal to indicate the completion of sense-amplifier stage transition. The detection signal gates the pull-down path of the sense-amplifier stage and the slave latch, thus overcoming the operational yield degradation, current contention, and glitches of previous SAFFs. The operational yield, speed, hold time, energy consumption, and area of the proposed and previous FFs are quantitatively compared for a wide range of V_{DD} with 22-nm FinFET technology. It is shown that the minimum V_{DD} of the SAFF-TCD is 573 mV lower than that of previous SAFFs, which means the SAFF-TCD can operate even when V_{DD} is in the near-threshold or subthreshold region. At 0.3-0.4 V, the SAFF-TCD operates twice as fast as the master-slave-based FF (MSFF) with a practical hold time. Even with these benefits, the energy consumption overhead is limited to less than 20% compared with that of MSFF, and the area is similar to that of previous SAFFs.

PROPOSED SYSTEM:.

In this paper, a low-power high-speed SAFF is proposed. A new sense-amplifier stage with a smaller pre-charge load is applied to reduce the power consumption of the pre-charge operation. A new single-ended latch is employed to achieve fast, low-power and glitch-free operation. Furthermore, MTCMOS optimization is employed in the proposed SAFF to achieve robust low voltage operations.

The schematic of the proposed SAFF is shown in Figure 5. As shown in Figure 5, the SAFF is composed of a SA stage and a slave latch, similar to the previous SAFFs. As described in previous sections, the SA stage could capture the data right after the rising edge of CK and the slave latch is applied to maintain the output during the negative half cycle of CK. The SA stage in the conventional SAFF needs to charge all the internal nodes during pre-charge operation, and some of the nodes such as n1, n2 and n3 in Figure 2a are discharged to VSS during the data-capturing operation no matter what the input data are. Actually, the pre-charge operation of n1, n2 and n3 has no practical effect on the function of the SA and is a waste of power. As shown in Figure 6a, the voltages of n1, n2, and n3 are charged close to the power supply voltage during pre-charge operation, and the sizes of the transistors MN3 and MN4 are large to decrease the propagation delay, so the pre-charge operation of these nodes is a large waste of power consumption. In this paper, the structure of the SA is changed; the NMOS controlled by CK (MN5 in Figure 2) is split into two (MN5 and MN6 in Figure 5) and moved to connect directly to the back-to-back inverter, as shown in Figure 5. Through the conversion, the nodes related to MN3 and MN4 no longer need to charge during pre-charge operation since the transistors MN5 and MN6 are off when CK is low. As shown in Figure 6b, the voltages of n1 and n2 in Figure 5 remain low throughout the operation. Thus, the powerof the pre-charge operation is greatly reduced. Since pre-charge power is an important part of the power consumption of the SAFF, the power consumption of the proposed SAFF can be greatly reduced.

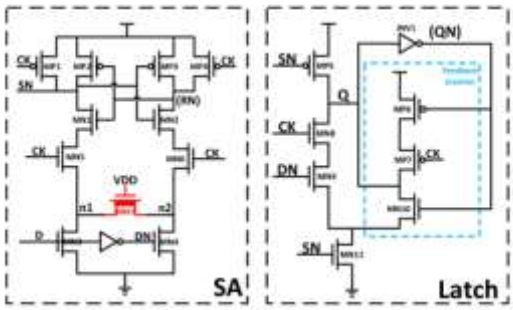

Figure 5. Schematic of the proposed SAFF

The proposed SA structure can also improve the hold time of the proposed SAFF. The new SA stage can capture the input data faster at the rising edge of CK. This is mainly because the internal nodes n1 and n2 remain low during the operation, and the discharge time of the internal nodes is reduced. Thus, the hold time of the proposed SAFF is reduced. Even though faster data capture increases the setup time of the proposed SAFF, the increase is very small because the discharge time of the internal nodes is short. A new single-ended latch is applied to the proposed SAFF. The proposed latch combines the advantages of Strollo's latch and Lin's latch to achieve fast and energy efficient operation. The first stage of the latch shown in Figure 5 is similar to that of Strollo's latch to achieve glitch-free operation. As shown in Figure 7b, the glitch of Lin's latch shown in Figure 7a is perfectly removed. This is mainly due to the insertion of MN9. When D is high, DN is low and the pull down path is totally cut off by MN9. Thus, the glitch is removed. The back-to-back inverters used for data storage are modified to overcome the current contention. For the output Q's transition from low to high, which means the voltage of SN is low, the feedback inverter is cut off by MN11. Similarly, for the output Q's transition from high to low, the feedback inverter is cut off by MP7. As a result, the effect of the feedback inverter on the output transition is completely eliminated. Since the latch has nothing to do with RN, the sizes of the transistors related to RN generation in the SA stage could be reduced to reduce power consumption. The 1× inverter INV1 in the latch could provide complementary output QN when necessary, and the delay difference between Q and QN is the same as MSFF, an inverter delay.

RESULTS:

The proposed SAFF has been designed based on **45** nm technology. In order to verify the validity of the proposed SAFF, the MSFF, the conventional SAFF, Nikolic's SAFF, Lin's SAFF and Jeong's SAFF have also been designed based on the same technology for comparison. With the same settings is adopted to perform all post-layout simulations for comparisons. The performance comparisons such as of the area, power consumption, CK-to-Q delay, setup time and hold time of the various flip-flops are described in detail below table.

Power and delay comparison of Existing and Proposed SAFF

Type of SAFF	Power	Delay	Area
Nikolic's SAFF	5.54mw	9.84ms	28
Strollo's SAFF	7.12mw	9.60ms	24
Jeong's SAFF	130mw	9.90ns	26
Lin's SAFF	2.21mw	1.143ms	20
Proposed SAFF	2.40mw	1.02ns	22

Designs, waveforms and output screenshots:

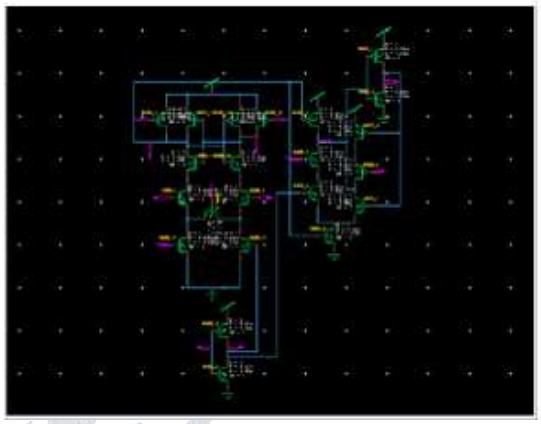

FIGURE 2 : Schematic of the proposed SAFF is shown in the figure

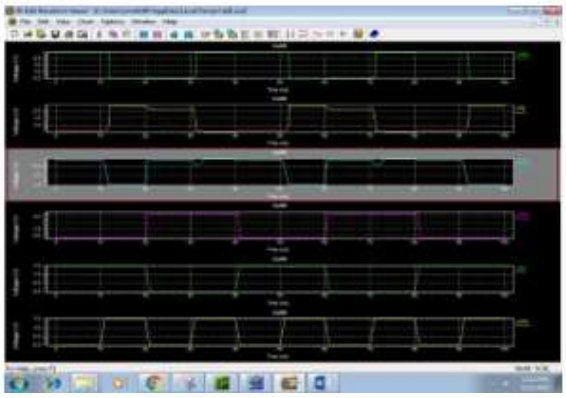

Figure 3 :Wave forms for proposed SAFF

FIGURE 4:VALUES OF POWER AND AREA

Conclusions

A low-power high-speed SAFF is proposed in this paper. A new structure for the SA stage is proposed to minimize the pre-charge power of the SAFF. Additionally, a glitch-free and contention-free single-ended latch is proposed. With the employment of the new SA stage and the single-ended latch, the delay and power of the SAFF are greatly optimized. The power-delay-product of the proposed SAFF shows a 2.7× improvement compared with that of the conventional SAFF at a 25% input data toggle rate. The improvement is 3.55× when compared with the MSFF, which indicates that the proposed SAFF is a good choice for replacing MSFFs in digital systems to provide low-power, high-speed operation. Author Contributions: conceptualization, H.Y.; methodology, H.Y.; data curation, H.Y., J.Y. and Z.Y.; writing—original draft preparation, H.Y.; writing—review and editing, H.Y., J.Y. and W.T.; supervision, J.Y.; project administration, S.Q. All authors have read and agreed to the published version of the manuscript. Funding: This research received no external funding. Conflicts of Interest: The authors declare no conflict of interest.

References

1. Teh, C.K.; Fujita, T.; Hara, H.; Hamda, M. A 77% energy-saving 22-transistor single-phase-clocking D-flip-flop with adaptive-coupling configuration in 40nm CMOS. In Proceedings of the IEEE Int. Solid-State Circuits Conf, San Francisco, CA, USA, 20–24 February 2011.

2. Suzuki, V.; Odagawa, K.; Abe, T. Clocked CMOS calculator circuitry. IEEE J. Solid-State Circuits 1974, 8, 462–469.

3. Partovi, H.; Burd, R.; Salim, U.; Weber, F.; Digregorio, L.; Draper, D. Flow-through latch and edge triggered flip-flop hybrid elements. In Proceedings of the IEEE International Solid-State Circuits Conference, Digest of TEchnical Papers, ISSCC. San Francisco, CA, USA, 8–10 February 1996.

4. Naffziger, S.D.; Colon-Bonet, G.; Fischer, T.; Riedlinger, R.; Sullivan, T.J.; Grutkowski, T. The implementation of the Itanium 2 microprocessor. IEEE J. Solid-State Circuits 2002, 37, 1448–1460.

5. Alioto, M.; Consoli, E.; Palumbo, G. General strategies to design nanometer flip-flops in the energy-delay space. IEEE Trans. Circuits Syst. I, Reg. Papers 2010, 57, 1583–1596.

6. Pan, D.; Ma, L.; Cheng, H.; Min, H. A Highly Efficient Conditional Feedthrough Pulsed Flip-Flop for High-Speed Applications. IEEE Trans. Very Large Scale Integr. (VLSI) Syst. 2020, 28, 243–251.

7. Matsui, M.; Hara, H.; Uetani, Y.; Kim, L.; Nagamatsu, T.; Watanabe, Y.; Chiba, A.; Matsuda, K.; Sakurai, T. A 200 MHz 13 mm 2D DCT macrocell using sense-amplifying pipeline flip-flop scheme. IEEE J. Solid-State Circuits 1994, 29, 1482–1490.

8. Montanaro, J.; Witek, R.; Anne, K.; Black, A.; Cooper, E.; Dobberpuhl, D.; Donahue, P.; Eno, J.; Hoeppner, W.; Kruckemyer, D.; et al. A 160-MHz 32-b 0.5-W CMOS RISC microprocessor. IEEE J. Solid-State Circuits 1996, 31, 1703–1717.

9. Nikolic, B.; Oklobdzija, V.G.; Stojanovic, V.; Jia, W.; Chiu, J.K.-S.; Leung, M.M.-T. Improved sense-amplifier-based flip-flop: Design and measurements. IEEE J. Solid-State Circuits 2000, 35, 876–884.

10. Kim, J.-C.; Jang, Y.-C.; Park, H.-J. CMOS sense amplifier-based flip-flop with two N-C2MOS output latches. Electron. Lett. 2000, 36, 498–500.

11. Lin, J.-F.; Hwang, Y.-T.; Wong, C.-S.; Shey, M.-H. Single-ended structure sense-amplifier based flip-flop for low-power systems. Electron. Lett. 2015, 51, 20–21.

12. Strollo, G.M.; De Caro, D.; Napoli, E.; Petra, N. A novel high-speed sense-amplifier-based flip-flop. IEEE Trans. Very Large Scale Integr. (VLSI) Syst. 2005, 13, 1266–1274.

13. Jeong, H.; Oh, T.W.; Song, S.C.; Jung, S.-O. Sense-amplifier-based flip-flop with transition completion detection for low-voltage operation. IEEE Trans. Very Large Scale Integr. (VLSI) Syst. 2018, 26, 609–620.

14. Jeong, H.; Park, J.; Song, S.C.; Jung, S.-O. Self-Timed Pulsed Latch for Low-Voltage Operation With Reduced Hold Time. IEEE J. Solid-state Circuits 2019, 54, 2304–2315.