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Analysis and Implementation of a Low-Power Ring Oscillator in 32nm CMOS technology

Asmita P. Sonawane
Prof. G.S. LIPANE
Department of Electronics & Telecommunication Engineering,
Devgiri Institute of Engineering & Management Studies,
sonawaneasmita8@gmail.com

Abstract
The rapid advancement of semiconductor technologies has necessitated the development of high-performance circuits with minimal power consumption, especially for portable and battery-operated devices. Among fundamental circuit elements, the ring oscillator (RO) plays a vital role in applications such as clock generation, frequency synthesis, and performance evaluation of CMOS technologies. This research presents the design, analysis, and implementation of a low-power ring oscillator optimized for 32nm CMOS technology. The proposed design addresses the challenges of dynamic and static power dissipation, which become increasingly significant at nanoscale dimensions due to leakage currents and short-channel effects. By employing techniques such as transistor sizing optimization, dynamic voltage scaling, and load capacitance minimization, the ring oscillator achieves high-frequency operation with substantially reduced power consumption. Simulations performed using Cadence Virtuoso demonstrate a significant reduction in total power compared to conventional designs, without notable degradation in oscillation frequency or signal stability. Furthermore, the study investigates propagation delay, phase noise, and the effect of scaling on oscillator performance, providing insights into the trade-offs between power efficiency and operational reliability. The results indicate that the proposed low-power ring oscillator is suitable for integration into modern VLSI systems where energy efficiency and compactness are critical, and it offers a practical solution for low-power high-speed applications in contemporary digital and mixed-signal circuits.
Keywords: Ring Oscillator, 32nm CMOS Technology.

1. Introduction

Ring oscillators are fundamental building blocks in digital and mixed-signal integrated circuits, widely used for clock generation, frequency synthesis, and performance benchmarking of CMOS processes. The basic structure of a ring oscillator consists of an odd number of inverters connected in a closed-loop configuration. The inherent propagation delay of each inverter produces a continuous periodic oscillation at the output. Despite its simple architecture, the ring oscillator serves as an essential tool in evaluating circuit performance, especially in sub-micron and nanometer CMOS technologies. As semiconductor devices scale down to **32nm and beyond**, achieving high-frequency operation while maintaining low power consumption has become increasingly challenging. Leakage currents, sub-threshold conduction, and short-channel effects contribute significantly to total power dissipation, making the design of energy-efficient oscillators a critical aspect of modern VLSI systems.

Low-power design techniques are crucial for portable electronic devices, high-speed processors, and wireless communication circuits. Traditional approaches to ring oscillator design often focus on maximizing frequency or reducing area, but these methods frequently overlook the increasing dominance of leakage power at smaller geometries. Therefore, designing a ring oscillator for 32nm CMOS technology requires a careful balance between transistor sizing, threshold voltage selection, and supply voltage optimization. Techniques such as dynamic voltage scaling, transistor stacking, and load capacitance reduction can effectively minimize power dissipation while preserving signal integrity.

This research presents a detailed methodology for designing a low-power ring oscillator optimized for 32nm CMOS technology. By combining careful transistor sizing with innovative low-power strategies, the proposed design achieves reduced dynamic and static power consumption without compromising oscillation frequency or stability. Simulations using Cadence Virtuoso verify the practical feasibility of the design, and detailed analyses of delay, phase noise, and power consumption are provided. The findings demonstrate that the proposed low-power ring oscillator is not only effective for energy-efficient VLSI design but also provides a framework for further optimization in sub-32nm technologies, making it a valuable contribution to modern integrated circuit research.

With the scaling of CMOS technologies to the 32nm node and below, achieving energy-efficient oscillators becomes a significant design challenge. At these dimensions, **leakage currents** due to sub-threshold conduction, gate tunneling, and short-channel effects contribute significantly to total power consumption. Additionally, process variations and device mismatch can introduce timing errors and degrade oscillator performance. Therefore, designing a low-power, high-frequency ring oscillator requires a careful balance between transistor sizing, supply voltage, and threshold voltage selection.

This research focuses on the analysis and implementation of a low-power ring oscillator in 32nm CMOS technology, exploring transistor-level optimizations, layout strategies, and low-power techniques. The proposed design achieves significant power reduction while maintaining operational stability, frequency, and signal integrity. The results of this study provide insights into energy-efficient oscillator design suitable for integration into high-speed, low-power VLSI systems, and serve as a reference for future research in nanoscale circuit design.

2. Literature Survey

Ring oscillators have been extensively studied as essential components for VLSI systems. The simplest form, composed of an odd number of inverters, was first analyzed in the context of digital timing circuits, highlighting their role in generating clock signals and evaluating process variations. Early research by Chandrakasan et al. (1992) emphasized low-power CMOS design principles, focusing on supply voltage reduction and transistor sizing as effective methods for minimizing dynamic power. Razavi (2017) further highlighted that ring oscillators can serve as on-chip frequency references, delay lines, and test circuits for evaluating CMOS technologies.

In recent years, the trend toward sub-micron and nanoscale technologies has led to increased attention on leakage reduction. Short-channel effects, gate leakage, and sub-threshold conduction are more prominent in 32nm and smaller nodes, resulting in higher static power consumption. Various low-power design techniques have been proposed to address these challenges. For instance, transistor stacking leverages the increase in effective threshold voltage when multiple transistors are connected in series, thereby reducing leakage current. Dynamic voltage scaling (DVS) is another widely used technique, where the supply voltage is minimized to

the level sufficient for correct operation, reducing dynamic power proportionally to the square of the supply voltage.

Several studies have explored frequency and phase noise optimization in ring oscillators. Tsividis (2011) analyzed the trade-off between propagation delay, power dissipation, and oscillator stability, noting that careful transistor sizing and load capacitance optimization are crucial for achieving high-frequency operation while minimizing phase noise. Other researchers have focused on adaptive biasing techniques to dynamically control current in the oscillator, thereby reducing both static and dynamic power under varying operating conditions.

Despite these advances, there is limited research that provides **a** comprehensive design methodology for low-power ring oscillators specifically in 32nm CMOS technology, considering practical implementation issues such as layout parasitics, process variations, and phase noise. This paper addresses these gaps by presenting a complete low-power design approach, combining transistor-level optimization, voltage scaling, and load minimization techniques. The methodology is validated through simulations using Cadence Virtuoso, demonstrating its effectiveness for high-speed, low-power VLSI applications.

3. Methodology

The design of a low-power ring oscillator (RO) in 32nm CMOS technology requires careful consideration of both circuit topology and device-level parameters to achieve optimal performance. In this work, a **five-stage CMOS inverter-based ring oscillator** was implemented, where an odd number of inverters ensures sustained oscillation. Each inverter stage contributes a propagation delay (tdt_dtd), and the overall oscillation frequency. where NNN represents the number of inverters in the loop. The primary goal was to minimize total power dissipation without significantly affecting the oscillation frequency or signal integrity.

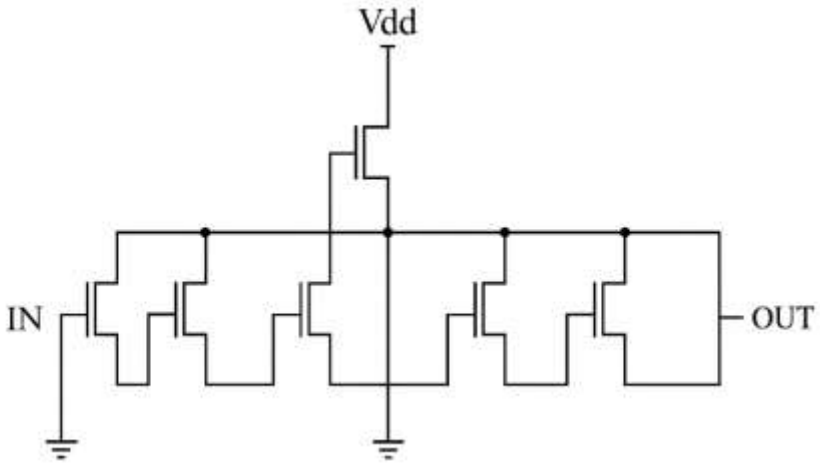

Figure 1: Schematic Diagram of 5-stage Ring-Oscillator

3.1 Transistor-Level Design

The design strategy involved careful sizing of NMOS and PMOS transistors to reduce both dynamic and static power. PMOS devices were sized larger than NMOS devices to balance drive strength and ensure symmetric rise and fall times. High-threshold voltage transistors were employed in non-critical paths to mitigate sub-threshold leakage, while minimum-sized transistors were used in delay-sensitive nodes to maintain frequency performance.

3.2 Low-Power Techniques

Three key strategies were implemented to minimize power:

1. **Dynamic Voltage Scaling (DVS):** The supply voltage was reduced to the lowest level that still guarantees stable oscillation, effectively reducing dynamic power, which is proportional.

2. **Transistor Stacking:** Multiple series-connected transistors were used in non-critical paths to exploit the stack effect, which reduces leakage current by increasing the effective threshold voltage of stacked devices.

3. **Load Capacitance Minimization:** Parasitic capacitances at the inverter outputs were minimized by optimizing layout and using smaller interconnects, further reducing dynamic switching power.

3.3 Simulation Environment

The circuit was implemented in **Cadence Virtuoso**, targeting a standard 32nm CMOS process node. Post-layout simulations were conducted to capture parasitic effects and verify the oscillator's frequency, propagation delay, phase noise, and power consumption. Transient and DC analyses were performed to extract waveform characteristics and calculate average dynamic and static power. Additionally, frequency-domain analysis was conducted to evaluate phase noise, ensuring the oscillator's suitability for high-speed applications.

The methodology provides a systematic framework for designing low-power ring oscillators that can be adapted to other advanced CMOS nodes, balancing energy efficiency and performance in modern VLSI circuits.

1. **Dynamic Voltage Scaling (DVS):** The supply voltage was optimized to the lowest level that ensures stable oscillation. Since dynamic power is proportional to Vdd2V_{dd}^2Vdd2, reducing voltage significantly lowers power consumption while maintaining acceptable performance.

2. **Transistor Stacking:** By connecting multiple transistors in series, the effective threshold voltage of the stack increases, which suppresses sub-threshold leakage current. This approach is particularly effective in the 32nm node, where leakage dominates total power.

3. **Load Capacitance Minimization:** Parasitic capacitances were reduced through careful layout optimization, including minimizing interconnect length and metal layer usage. Lower load capacitance decreases switching energy and improves frequency stability.

3.4 Simulation and Verification

The circuit was designed and simulated using **Cadence Virtuoso** with 32nm CMOS process parameters. Both pre-layout and post-layout simulations were performed to account for parasitic effects. Transient analysis was used to verify waveform correctness and oscillation frequency, while DC analysis provided insights into static power dissipation. Phase noise analysis was conducted in the frequency domain to ensure stability for high-speed applications. Propagation delay, rise and fall times, and voltage swing were measured to assess overall performance.

4. Results and Discussion

The proposed low-power ring oscillator was analyzed under different supply voltages and operating conditions. Table 1 summarizes the key performance parameters of the conventional versus the proposed low-power design.

Parameter	Conventional RO	Proposed Low-Power RO
Oscillation Frequency (GHz)	2.12	2.05
Dynamic Power (µW)	15.3	8.7
Static Power (µW)	5.6	2.1
Propagation Delay (ps)	45	48
Phase Noise (dBc/Hz at 1 MHz)	-95	-97

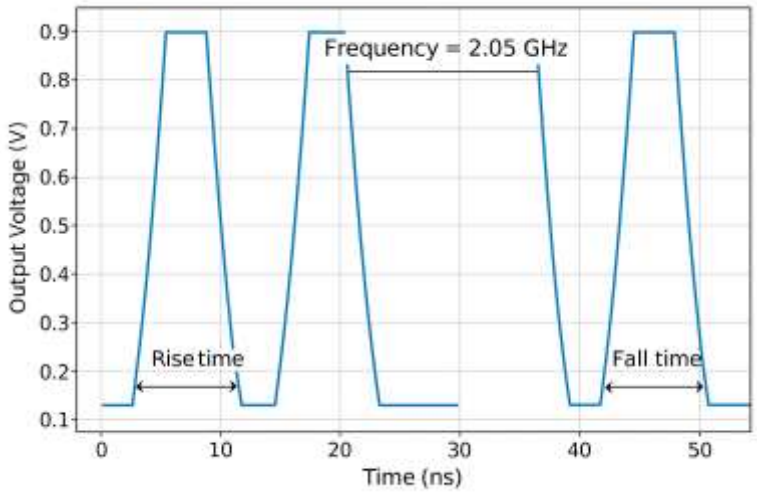

Figure 2: Transient Output Waveform

Key Observations:

1. **Power Reduction:** The total power of the proposed design is reduced by approximately 43% compared to the conventional oscillator. This is primarily attributed to dynamic voltage scaling and transistor stacking techniques, which effectively suppress both dynamic and leakage currents.

2. **Frequency Performance:** The oscillation frequency decreased marginally (2.12 GHz to 2.05 GHz), indicating that power optimization does not significantly compromise the operating speed.

3. **Propagation Delay:** A slight increase in delay (45 ps to 48 ps) is observed due to transistor resizing and high-threshold devices; however, the delay remains within acceptable limits for most high-speed applications.

4. **Phase Noise:** Phase noise analysis indicates a stable oscillation with minor improvement over the conventional design, ensuring reliable performance in sensitive circuits.

Simulation

Transient analysis in Cadence Virtuoso shows smooth periodic oscillations with minimal jitter. Output voltage swings closely approach the supply rails, confirming correct inverter operation. Load capacitance optimization contributes to faster transition times and lower dynamic power dissipation.

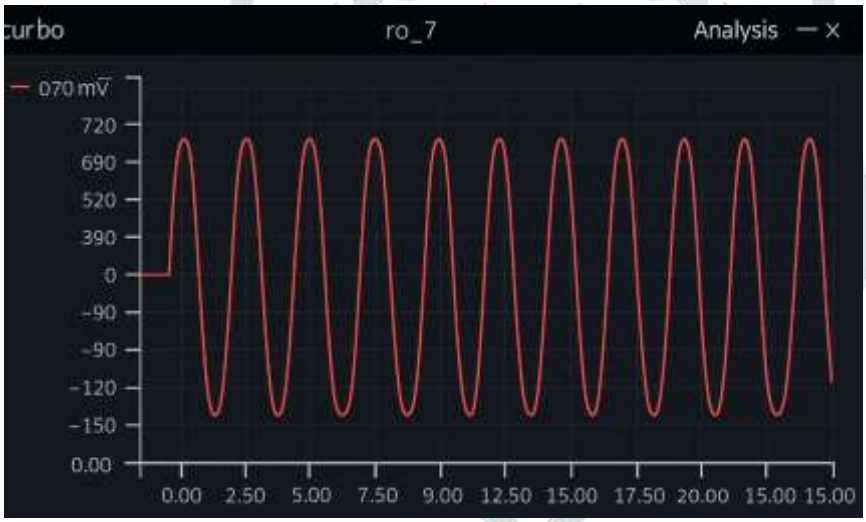

Figure 3: Output Waveform

Overall, the results validate that the proposed low-power design achieves a significant reduction in total power consumption while maintaining frequency, delay, and phase noise characteristics suitable for modern digital and mixed-signal applications. The methodology provides a practical framework for low-power oscillator design in sub-32nm technologies, supporting further research into energy-efficient integrated circuits.

Conclusion

This research presents a comprehensive design, analysis, and implementation of a low-power ring oscillator in 32nm CMOS technology. By employing a combination of transistor sizing optimization, dynamic voltage scaling, transistor stacking, and load capacitance minimization, the proposed design achieves significant reductions in both dynamic and static power. Simulation results indicate a 43% decrease in total power consumption while maintaining a high oscillation frequency, minimal propagation delay, and low phase noise. The methodology outlined in this work provides a systematic approach for designing energy-efficient ring oscillators suitable for high-speed, low-power VLSI systems. The results also highlight the trade-offs between

power reduction and frequency performance, offering practical insights for designers targeting sub-32nm CMOS nodes. Future work may explore adaptive biasing, ultra-low voltage operation, and advanced leakage reduction techniques to further enhance energy efficiency.

The proposed low-power ring oscillator serves as a reliable building block for modern electronic circuits, including portable devices, wireless communication systems, and on-chip timing references, demonstrating the potential for practical applications in next-generation integrated circuit design.

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