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Heterogeneous Integration of Flexible VLSI: Combining Near-Threshold Computing with Advanced Materials for Ultra-Low-Power Bioelectronic Systems

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Abstract
Traditional electronics, mechanical rigidity and power limitations pose serious challenges for wearable and implantable devices (WIDs). This work introduces a heterogeneous flexible VLSI integration strategy that uses Near-Threshold Computing (NTC) in conjunction with mechanically compliant materials to achieve ultra-low-power operation. Battery-less WIDs powered by harvested energy are made possible by our demonstration that NTC architectures operating at VDD ≈ VT provide orders of magnitude energy reduction when compared to super-threshold operation. For high-density digital processing (>1000 cm²/Vs mobility), the integration uses thinned silicon CMOS dies (15µm thickness, bendable radius R ≥ 9mm) on flexible substrates (50µm polyimide/LCP). Meanwhile, hybrid organic-inorganic semiconductors (ZnO nanosheets: 200 cm²/Vs mobility, Ion/Ioff ~10⁹) and carbon nanotubes (100-1000s cm²/Vs) offer superior mechanical compliance for analog front-ends and stretchable interconnects. Al buffer layers used in structural engineering allow for 6000 bending cycles at a radius of 12 mm while maintaining ferroelectric performance (2Pr = 29.5µC/cm²). In 2mm × 1.7mm packages, commercial biomedical front-end integrated circuits have an active power consumption of 50µA. The main obstacles are long-term biocompatibility, NTC variability mitigation, and manufacturing yield (75% for printed devices, 60% failures from interface defects). The basis for intricate, flexible bioelectronic systems that enable individualized health monitoring is provided by this diverse approach.

Keywords: Flexible VLSI, Near-Threshold Computing (NTC), Wearable Electronics, Bioelectronics, Heterogeneous Integration, Organic Semiconductors, Low-Power CMOS.

1. Introduction and Contextualization of Flexible VLSI

Currently, advanced electronics are undergoing a paradigm shift: from focusing solely on rigid miniaturization to fabricating soft and conformable macro-electronics [1]. This is fundamentally driven by the growing needs of so-called Wearable and Implantable Devices, which call for electronics that can function during bending, stretching, or intimate conformity with biological surfaces, like the skin or human internal organs [2]. Traditional

microelectronics pursue integration density and ultimate performance within a rigid framework; their macro-electronic counterparts, using flexible and stretchable substrates, will be oriented toward large-area and low-cost applications, as well as new form factors that will be required for electronic paper, smart packages, and skin-like sensors [1]. This technological transition is based on a very important motivation that does not relate to mechanical robustness but rather to the power limitations associated with WIDs. Miniaturization has progressed very fast, but these devices are now limited by a power limit rather than a physical limit [3]. The total size of a WID is often dominated by the battery, whose fixed energy density and limited lifetime provides challenging design constraints for complex, multi-task continuous computing applications [3]. Smaller and smarter devices with extended functionality will have to be developed with the implementation of aggressive power reduction strategies in the VLSI components. This need toward power efficiency and mechanical flexibility in conjunction creates a symbiotic relationship between ultra-low-power circuit design and flexible fabrication techniques. Possible power consumption reduction via flexible VLSI enables extremely limited harvested energy from thermoelectric generators, piezoelectric devices, or RF harvesting and thus creates the potential for truly battery-less WIDs [3]. This report presents a rigorous assessment of the convergence required between advanced flexible materials, extreme low-power circuit design, namely Near-Threshold Computing, and heterogeneous integration strategies to achieve reliable high-performance bioelectronics.

2. Foundations of Flexible VLSI Integration: Substrates and Fabrication Techniques

Successful development of flexible VLSI systems is closely related to the selection of compliant substrates and perfection of techniques for integrating high-performance electronic components on such soft foundations.

2.1 High-Performance Substrate Materials

Substrates must meet very challenging requirements regarding mechanical compliance, environmental stability, and electrical performance. Some of the common substrate materials used are double copper clad polyimide and LCP films; these are around 50mu thick [4]. Of these, LCP is of special interest because of its low moisture absorption and very good characteristics at high frequency [4]. These characteristics are of key importance for integrated RF components that enable wireless communication of wearable devices, IoT/WSN, providing reliable and efficient data transmission from a biosensor to an external receiver [4, 5]. Because of this, the substrate choice is by no means a matter of mechanical support only but affects the system-level aspects of wireless data links.

2.2. Silicon Thinning and Transfer Techniques for High-Density VLSI

In order to achieve the high computational density required for VLSI signal processing, leveraging mature silicon technology is often necessary. The heterogeneous integration strategy of thinning the conventional rigid silicon dies and transferring them onto flexible substrates has been the dominant approach for the integration of high-performance VLSI [4].

In this process, ultra-thin silicon chips ("flex-chips") as thin as ~15µ have been successfully produced; often these chips are quite large, with widths as wide as 4mm and lengths from 8mm up to 36mm [6]. The process for fabricating thin chips requires several labor - intensive steps: substrate fabrication, patterning of the copper circuitry, and the critical step of die thinning [4]. One major process incompatibility encountered in the development process was chemical compatibility. Acrylic-based polymers used in the thinning process, for example, are dissolved by cleaning solvents such as APTEK, which necessitates the use of special chemical protocols for wafer bonding and pre-transfer cleaning of the devices.

2.3. Mechanical Resilience and Reliability Engineering

Mechanical compliance refers to the radius of curvature, R, which a chip can support without failure. Ultra-thin chips have been tested successfully in the bendable range, with radius of curvature as small as 9mm and above [6].

However, relying solely on flexibility of the materials is often inadequate, especially when it involves integrating advanced functional layers such as ferroelectric memory devices, which are necessary in low-power edge

computing for IoT applications [7]. In this regard, structural layer engineering is utilized to handle mechanical stresses. It has been found that the addition of an ultra-thin Al buffer layer at the backside has significantly improved the durability of the device [7]. The buffer layer of Al creates and transmits additional stress to the fragile silicon substrate, thus mitigating the bending stress that the ferroelectric thin films experience, which effectively suppresses crack growth and degradation of ferroelectricity therein [7]. Such a method allows Si-based ferroelectric devices to maintain functional performance, attaining a 2Pr value of 29.5muC/cm^2 even after 6000 bending cycles at a 12mm outward radius [7]. What this epitomizes is that, in order to be able to preserve the electrical performance of advanced material systems under strain, it requires a sophisticated approach to mechanical stress management via optimized structural layers.

2.4. Advanced Manufacturing: Printed and Large-Area Electronics

Printing processes represent an attractive route to scale up flexible and stretchable electronics, possibly enabling low-cost, large-area manufacturing for macroelectronics applications [1].

While the fabrication of fully printed devices using complex geometries-sensors, wires, patterns-has shown a yield of up to 75% [8], critical reliability issues remain. The primary source of device failure (60% of failures) is identified in poor interfacing between the printed conductors (e.g., copper wire) and the activated paths [8]. This high rate of failures with unreliable interfaces creates a significant bottleneck for mass production and commercial industrialization [9]. Stable, robust, and repeatable electrical interfaces of various printed layers are a major material science and process engineering challenge that must be resolved if printed flexible VLSI is to attain economic scaling.

3. Ultra-Low-Power Circuit Design for Energy-Constrained Wearables

Integration of flexible substrates needs to be associated with circuit design methodologies that reduce power consumption in order to solve the power bottleneck issue of WID.

3.1. Basics of CMOS Power Management in Flexible Systems

Complementary Metal-Oxide-Semiconductor technology is indispensable because it has inherent low power characteristics [10]. In CMOS, there are two components of power consumption: static and dynamic. Static power consumption is due to the leakage current flowing through the transistors in the off state, which increases as transistors shrink and process technology advances. Dynamic power consumption occurs in switching transistors; it is due to the charging and discharging of load capacitances. Critically, dynamic power is directly proportional to the square of the supply voltage VDD^2. This quadratic relationship provides the fundamental rationale for aggressively scaling VDD as the most effective path toward extreme energy efficiency [11].

3.2. Near-Threshold Computing (NTC) Architectures

NTC, on the other hand, exploits this VDD^2 dependence by lowering the supply voltage into the NTV regime where VDD approximates the transistor threshold voltage, VT [12]. The absolute minimum energy consumption for many CMOS designs is achieved within this regime, often representing orders of magnitude improvement in energy efficiency compared to standard super-threshold operation [12].

In general, operating integrated circuits in the NTV regime can enable fundamentally batterless WIDs, as power consumption drops low enough to be sustained solely by limited energy harvesting mechanisms [3]. The benefits of NTC also scale effectively with Moore's law, confirming substantial energy improvements in advanced process nodes, for instance, Intel's 32-nm, 22-nm, and 14-nm technologies [12]. This will continue to amplify the energy benefits afforded by NTC in the near future, enabling more complex digital VLSI architectures on flexible substrates without draining the generally limited power supply.

However, such aggressive voltage scaling is not without substantial engineering challenges. Operating at NTV has several negative consequences: loss of silicon frequency, increased performance variations due to both process and temperature sensitivity, and higher functional failure rates in both memory and logic circuits. Thus, energy-efficient heterogeneous SoCs employ dedicated NTV-optimized IP blocks-e.g., CPU and interconnect

fabrics-and resilient adaptive computing mechanisms that ensure reliable operation over the large voltage range from nominal down to the NTV regime.

Architectural heterogeneity in those flexible VLSI systems is often dictated by the required power-performance tradeoffs: for instance, deploying only NTC cores for background monitoring and all non-critical tasks, reserving only higher-voltage, higher-frequency blocks to support bursts of high-priority computation or wireless transmission. A comparison of operational regimes is presented below in table 1.

Table 1: Comparative Analysis of CMOS Operation Regimes

Operating Regime	**Supply Voltage (VDD) Relation to VT**	**Energy Efficiency**	**Primary Challenge**	**Performance (Frequency)**	**Application Suitability**
Super-Threshold (ST)	VDD > VT	Low (High Dynamic Power)	High Energy Consumption	High (Maximum Speed)	Desktop/Server Computing
Near-Threshold (NT)	VDD ~VT	Maximum (Energy Peak)	Variation, Reliability, Speed Degradation	Low to Moderate	Wearables, IoT Edge Computing, WIDs [12]
Sub-Threshold (SubT)	VDD < VT	Very Low Energy (High Leakage Ratio)	Extremely Slow, High Variability	Very Low	Ultra-low Power Sensing/Sleep Modes

3.3. Low-Power VLSI Benchmarks

Practical implementation benchmarks illustrate the low power consumption requirements for a front-end bioelectronic. Commercial flexible biomedical front-end ICs, for example, the AD8233, exhibit an active low-power consumption of 50 mA in an ultra-small 2mm times 1.7mm WLCSP package [5]. This level of performance is necessary to enable extended battery life for projects that may involve continuous ECG monitoring. Interfacing such low-power front-ends with flexible biosensors, and in many cases IoT edge nodes, demands integrated signal processing [5, 7].

4. Novel Material Candidates for Flexible High-Performance Devices

While thinned silicon offers high performance, alternative materials can offer superior mechanical characteristics and stability, often driving hybrid integration strategies.

4.1. Two-Dimensional (2D) and Carbon Nanomaterials

Nanomaterials have attracted significant interest in this field because they often offer significantly better performance than traditional organic semiconductors while remaining easier to process than amorphous silicon (a-Si) or polysilicon.

Carbon nanotubes, in single-wall networks, hold great promise for flexible electronics. CNTs have very high carrier mobility, excellent mechanical flexibility, and stability, rendering them applicable as channel semiconductors in flexible thin-film transistors and as highly stretchable conductors in several sensors. Besides, 2D materials of graphene and MXene are among the primary candidates for flexible electronics and integrated conductors on flexible substrates.

4.2. Organic and Hybrid Organic-Inorganic Semiconductors (HOIS)

Traditional large-area semiconductors are low cost (e.g. amorphous silicon, a-Si) but have poor carrier mobility and limited flexibility, severely restricting their utility in complex, high-performance flexible VLSI [13]. The performance metrics of organic semiconductors are typically worse than those made of inorganic materials.

A strong alternative is represented by Hybrid Organic-Inorganic Semiconductors (HOIS). Research on flexible circuits with the introduction of high-quality Zinc Oxide (ZnO) nanosheets as active semiconducting elements has shown outstanding electrical characteristics [14]. These hybrid devices systematically show high field-effect mobility (meff) over 200 cm^2/(Vs), a very high on/off current modulation ratio (Ion/Ioff) of about 10^9, and excellent operational stability, including very low hysteresis and negligible threshold voltage shifts after prolonged electrical stressing-up to 340 minutes [14].

Moreover, perovskite blend-based HOIS are also being investigated, especially for applications in integrated flexible optoelectronics such as LEDs, which exploit the excitonic energy transfer effects.

The comparison shows that hybrid materials like CNTs and ZnO nanosheets represent a strong balance of high mobility, comparable to polysilicon, but exhibit superior mechanical robustness combined with excellent switching. 1, 14 This suggests a hierarchical approach in VLSI design wherein thinned silicon CMOS, optimized with NTC, is used for high digital density (processor/memory) while hybrid CNT or ZnO FETs are deployed for analog front-end circuitry, high current drive structures, and stretchable interconnects on account of their mechanical advantage. Table 2 summarizes the comparative performance metrics of these key flexible semiconductor technologies.

Table 2. Comparative Performance of Key Flexible Semiconductor Technologies

Technology Platform	**Key Material**	**Typical Mobility (meff, cm^2/Vs)**	**Ion}/Ioff} Ratio**	**Flexibility/Bending Limit**	**Integration Maturity**	**Relevant Application**
Thinned Inorganic Si (Monolithic)	Monocrystalline Silicon Die	Very High (>1000)	Excellent (>10^9)	Moderate (R ~ 5-15mm) [6, 7]	High (Industry Standard)	High-density Logic, Memory [7]
Carbon Nanotubes (CNTs)	SWCNT Networks	Extremely High (100–1000s) [1]	High	Superior (Stretchable) [1]	Medium	High-speed Flexible TFTs, Conductors
Hybrid Organic-Inorganic (HOIS)	ZnO Nanosheets on Substrate	High (>200) [14]	Exceptionally High (~ 10^9) [14]	Excellent (Low Hysteresis/Stress)	Medium	High-Stability Switches, Active Matrices
Amorphous Silicon (a-Si)	a-Si:H Thin Film	Low (<1) [13]	Low to Moderate	Moderate	High (Large-Area Displays)	Low-Performance Displays, Passive Sensing

5. Flexible VLSI Systems for Biomedical and Wearable Applications

Flexible VLSI translates the advances made in material science to functional, clinically relevant devices, especially in biosensing and signal acquisition.

5.1. Flexible Biosensing Platforms

The integration of flexible materials with different optical sensing technologies has greatly contributed to advancements in personalized medicine and health monitoring. Mechanisms of transduction involved in flexible optical biosensors include, but are not limited to, SPR, optical fiber sensing, fluorescence sensing, and SERS. New materials explored to increase functionality and wearability include nanostructured materials, MXenes, hydrogels, and textile-based integrated platforms. These platforms have been designed for enhancing sensitive and selective detection of biomarkers, environmental pollutants, and physiological parameters continuously in real time.

5.2. Flexible Front-End Integrated Circuits (ICs) for Signal Acquisition

Collected sensor data has to be processed as soon as possible. The flexible VLSI components have to be capable of running advanced signal conditioning and processing tasks, often as an edge node processor for an IoT environment [5, 7]. Integrated logic and highly reliable, low-power flexible memory are required for immediate data storage and analysis, such as the durable HZO ferroelectric devices [7].

This includes the challenge of integration: from advanced sensing elements, such as MXenes or hydrogels [16], all the way to high-performance, low-power VLSI readout circuitry, represented by NTC CMOS or hybrid FETs. What used to be a flexible system that only monitored (passive sensing) is now turning into active data processing at the edge that needs to be energy-efficient to execute complex tasks without offloading data continuously [5, 17].

5.3. Implantable Devices and Biocompatibility

Applications of flexible and stretchable bioelectronics are broad, ranging from skin-worn sensors for a variety of modalities to neural implants for diagnosis or therapy. For these systems, successful integration presents significant challenges due to the chronic biological environment. Major challenges include the long-term stability and functionality of materials within dynamic biological conditions and reliable biocompatibility during sustained skin contact or implantation. It is under these conditions that the VLSI system needs to be designed with a required computational throughput.

6. Reliability, Mechanical Integrity, and Scaling Challenges

Despite significant advances, several critical engineering and material science challenges remain before flexible VLSI attains widespread commercial and clinical deployment.

6.1. Mechanical Stress and Fatigue Analysis

The future of flexible electronics places a high emphasis on the fact that the whole system needs to be able to sustain not just bending but stretching, too [18]. This demand requires another approach in material selection, structural design, and the development of specialized components such as stretchable conductors, crucial in the connection between working circuits across deformable platforms [18]. Fundamental structural designs and mechanisms need to be used to achieve the property of stretchability, such as optimizing the position of the neutral mechanical axis and adopting tactics from flexible layouts [18]. Quantifiable benchmarks are paramount for mechanical endurance, such as the 6000 bending cycles at a radius of 12mm that some flexible ferroelectric Si devices have been capable of [7]. Indeed, this implies that extreme flexibility-aka, full stretchability-can tolerate only interconnects and low-density sensors, while high-performance VLSI components use engineered mechanical encapsulation and structural layers to sustain their operational resilience under conditions of moderate bending.

6.2. Device Reliability and Long-Term Stability

Apart from mechanical fatigue, device reliability is at risk for electrical instability and interaction with the environment. Though hybrid materials like ZnO nanosheets have exhibited very good short-term stability, with threshold voltage shifts being negligible even after hours of electrical stress [14], long-term operation-over

months or years-in dynamic biological environments is a big question, mainly for implantable devices that demand robust encapsulation [2].

In addition, in wearable biosensing applications, motion artifacts and environmental fluctuations are common sources of interference signals that compromise the accuracy of biomarker detection [16]. The VLSI design must therefore implement advanced integrated signal conditioning and filtering circuitry to mitigate these external noise sources and ensure data fidelity and robustness [16].

6.3. Fabrication Yield and Industrialization Bottlenecks

Yield issues, especially, are a problem in printed electronics that impedes the transition to high-volume manufacturing. Poor interfacing between different material layers, for instance, contact points of printed copper conductors and active device paths, is often the cause of low yield observed in fully printed complex devices [8]. In this regard, substantial development of materials synthesis, process techniques, and cost reduction should be elaborated at each link along the supply chain to actually drive the industrial application of flexible electronics [9]. The ultimate flexible VLSI system must achieve multi-dimensional resilience, simultaneously dealing with electrical noise, mechanical strain, and process variability. Table 3 summarizes the key challenges and associated mitigation strategies.

Table 3. Key Reliability Challenges and Mitigation Strategies in Flexible VLSI

Challenge Domain	Root Cause/Metric	Impact on System Performance	Mitigation Strategy (VLSI/Structure)	Source Reference
Mechanical Strain/Fatigue	Bending Radius (R ~ 5-15 mm), High Cycle Count (6000)	Degradation of electrical performance (e.g., 2Pr in ferroelectrics), Crack growth [7]	Structural Buffer Layers (e.g., Al), Optimized layout (Neutral axis design) [7]	[7]
Energy/Power Density	Fixed energy density of batteries; Limited harvested energy [3]	Limits functionality (complex tasks), Dominates total WID size [3]	Near-Threshold Computing (NTC) methodology, Optimized low-power IPs [12]	[3]
Electrical Stability	Hysteresis, Threshold Voltage Shift, Prolonged Stress	Unreliable switching, functional failure in logic/memory [14]	High-quality hybrid dielectrics, Optimized active layers (e.g., ZnO Nanosheets) [1]	[14]
Manufacturing Scalability	Poor interfacing failure (60% of failures), High cost [8]	Low yield, hinders industrial adoption and cost reduction	Improved interfacing protocols, optimization of printing/processing techniques [8]	[8]
System Accuracy	Motion Artifacts, Environmental Fluctuation [16]	Signal interference, reduced detection accuracy for biomarkers [16]	Integrated signal conditioning/filtering VLSI, robust encapsulation	[16]

7. Challenges and Directions

Even with great advancements, a number of basic issues need to be resolved before broad clinical and commercial implementation. Mainly, manufacturing scalability because of unstable material interfaces, current fabrication yields especially for printed electronics (~75%) remain insufficient for economical mass production. long-term

reliability, although short-term electrical stability has been shown to exist (with negligible threshold shifts after 340 minutes of stress), reliable encapsulation techniques and additional validation are needed for long-term operation over months to years in dynamic biological environments, particularly for implantable applications. Lastly, electromechanical interdependence due to the intricate relationship among mechanical strain, electrical performance (especially important in the NTV regime where margins are small), and environmental factors necessitates the development of comprehensive predictive modeling capabilities.

8. Conclusion

This work has shown that in order to achieve wearable and implantable devices that are practical, we need to move away from traditional monolithic approaches and toward carefully architected heterogeneous systems that strategically utilize the strengths of various material platforms. Three crucial technological fields, ultra-low-power circuit design, advanced flexible materials, and heterogeneous integration strategies converge fundamentally in the development of flexible and stretchable VLSI systems for bioelectronic applications.

According to the analysis in this work, the main limitation for wearable and implantable devices is now the power bottleneck rather than actual miniaturization limits. When paired with energy harvesting mechanisms, Near-Threshold Computing architectures operating in the NTV regime (VDD ≈ VT) can achieve orders of magnitude improvements in energy efficiency, potentially enabling truly battery-less operation. Significant difficulties are brought about by this aggressive voltage scaling, though, such as decreased operating frequencies, performance variability, and heightened vulnerability to temperature and process changes.

In order to overcome these obstacles, our heterogeneous integration framework combines complementary material systems that offer better mechanical compliance with thinned silicon CMOS (15μm thickness, bendable to R~9mm) optimized for NTC operation. Stable hybrid organic-inorganic semiconductors like ZnO nanosheets (>200 cm^2/Vs, Ion/Ioff ~10^9) and high-mobility carbon nanotubes (100-1000s cm^2/Vs) provide remarkable mechanical robustness for analog front-ends, sensor interfaces, and stretchable interconnects while preserving the computational density required for intricate signal processing tasks. Important engineering advancements include substrate selection that prioritizes low-moisture absorption materials like LCP for RF functionality, optimized buffer layers for structural stress management (exemplified by Al backside layers that enable 6000 bending cycles at a 12mm radius), and advanced electrical interface engineering to address the predominant failure mode (60 percent of failures) in printed flexible electronics.

9. References

1. Cai, L., & Wang, C. (2015). Carbon nanotube flexible and stretchable electronics. Nanoscale Research Letters, 10(1), 320.
2. Chitrakar, C., Hedrick, E., Adegoke, L., & Ecker, M. (2022). Flexible and stretchable bioelectronics. Materials, 15(5), 1664.
3. Martinez, R. V. (2015). Flexible electronics. Micromachines, 6(4), 607-620.
4. Banda, C., Bower, K., & Salama, K. N. (2008). Flexible electronics: Thin silicon die on flexible substrates. Proceedings of the Electronics Components and Technology Conference, 2109-2114.
5. Wang, C. K. (n.d.). Flexible ECG front end IC also serves as IoT edge node signal processor. Analog Dialogue.
6. Dahiya, R. S., & Gennaro, S. (2013). Bendable ultra-thin chips on flexible foils. IEEE Sensors Journal, 13(10), 4030-4037.
7. Pandey, A. C., & Karnik, S. (2024). Flexible and stretchable electronics for wearable health monitoring: Review. Electronics, 13(1), 24.
8. Mohammed, M. G., & Kramer, R. (2017). All-printed flexible and stretchable electronics. Advanced Materials, 29(19).
9. [Authors not specified]. (n.d.). Flexible electronics for smart sensing. [Details from PMC pending for full citation.]
10. [Authors not specified]. (n.d.). CMOS technology in processors explained. AI Future School.
11. [Authors not specified]. (n.d.). CMOS power consumption. Cadence Design Systems.

12. Wang, Q., Wang, J., Li, W., & Wang, S. (2019). Flexible electronics: Integration processes for organic and inorganic semiconductor-based thin-film transistors. Micromachines, 10(2), 16.
13. Kim, D.-H., Viventi, J., Molina, J. J. A., et al. (2017). Stretchable electronics: From skin to brain. Nature Biomedical Engineering.
14. [Authors not specified]. (n.d.). [Review Article]. [Details from PubMed pending for full citation.]
15. Vassilakopoulou, A., Papadatos, D., Zakouras, I., & Koutselas, I. (2016). Mixtures of quasi-two- and three-dimensional hybrid organic-inorganic semiconducting perovskites for single layer LED. arXiv preprint.
16. [Authors not specified]. (n.d.). Flexible electronics: A platform for smart devices. [Details from PMC pending for full citation.]
17. Yin, Z., Zhou, H., Choppali, C., Sudarshan, V., Chabria, J., & Gu, J. (2025). Toward lifelong-sustainable electronic-photonic AI systems via extreme efficiency, reconfigurability, and robustness. arXiv preprint.
18. Wu, W. (2019). Stretchable electronics: Functional materials, fabrication strategies and applications. Science and Technology of Advanced Materials, 20(1), 187-224.