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Design and analysis of low power CMOS SAR-ADC for Bio-Medical Applications

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ABSTRACT:

Accurate biological signal acquisition depends on very efficient SAR ADCs. This work collects biological signals using an 8-bit CMOS 45 nm SAR-ADC. This study proposes high energy efficiency in the nanowatt region using a DAC. Energy efficiency increases significantly because this technology allows comparisons to be made without using any energy. The investigation indicates that specific offset cancellation methods are not necessary; merely altering the transistor size could potentially optimize the comparator. We successfully realized the SAR-ADC design using 45 nm CMOS semiconductor technology. The ADC achieves a Spurious-Free Dynamic Range (SFDR) of 64.12 dB at a power consumption of 1.89 microwatts. It is powered by a 1voltage supply and has a sampling rate of 1.1 megahertz.

Keywords: SAR-ADC, DAC, CMOS

1. INTRODUCTION

Advancements in CMOS technology have created a demand for implantable cardiac healthcare equipment like defibrillators and pacemaker devices. Implanted technological gadgets require non-rechargeable batteries to function for approximately ten years. They can accomplish this by surreptitiously and consistently monitoring physiological indicators as a person carries out their everyday activities. In order to provide continuous data recording over a long period of time, it is crucial to use low-power technologies. The authors often refer to the use of advanced technology for collecting and analyzing low-power bio-signals as a physiologically observable analog front-end (AFE) [1, 2].

ADCs, or analog-to-digital converters, play a crucial role in implanted sensors' ECG detection. Their energy requirements are high. Low-frequency analog electrical impulses and cardiac signals do not require fast conversion. One of the biggest challenges is to build a low-power ADC for cardiac implants that transforms signals accurately. The biomedical industry widely uses SAR ADCs due to their low power consumption, middling resolution, and slow speeds. The simple construction of SAR ADCs makes them ideal for cardiac implantation. While SAR ADCs utilize energy efficiently, comparator distortions and capacitor mismatches reduce them level of resolution [3, 4]. Dithering is another way to reduce mistakes and improve linearity in DACs. We use latched comparators in combination with capacitance DACs to reduce power consumption inside the SAR ADC. Using pre-existing concepts of a latched dynamic comparator alongside a functional capacitive DAC, the study built a low-power SAR-ADC. A significant upgrade to the DAC architecture, which reduced internal capacitance, resulted in lower power consumption and a smaller DAC size.

This study has successfully constructed a non-binary weighing system (DAC). This converter uses redundancy throughout the conversion process. We have normalized the capacitance measurements of the arrays within the DAC to the closest integer to maintain consistent geometry. Furthermore, rearranging the latching comparator reduces clock feedthrough, charge injection, and power consumption [5, 6]. The section 2 covers the literature survey and the methodology of SAR ADC has been discussed in section 3. The simulation results of proposed SAR ADC are discussed in section 4 followed by conclusion in section 5.

2. LITERATURE REVIEW

Taeju Lee et. al. [8] have created an 8-channel configurable multifunctional neural-recording ASIC IC. This IC improves the availability and utilization of recording channels for

scientific applications. Each channel's design dictated whether its purpose was to collect voltage or current. While the number of channels remains constant, the experiment's goals, conditions, and setups can alter their current or voltage levels, thereby enhancing the channels' usability and accessibility. The authors built an integrated circuit using 180-nanometer CMOS semiconductors to test the suggested method.

Liu et al. [9] improved speed and conversion using a typical reconfigurable SAR-ADC. A capacitance-preserving digital-to-analog converter (CDAC) enables several conversion modes, reducing the time required for pre-charging procedures and the energy consumption of switches. The authors have adjusted the controller circuits to reduce the chip's size while maintaining its reconfigurability capability.

Shuenn-Yuh Lee et al. [10] assessed the analysis of implanted data from a single integrated circuit using novel low-power methods. To run this approach, the power management system needs the most power. Sung-Hun Jo and colleagues presented an adaptable and flexible Internet of Things (IoT) sensor analog front end (AFE). With its adjustable analog front-end and 1-bit bond pad, the device can handle several sensor outputs. The flexible method of obtaining and modifying the sensor output enables reliable measurement across a broad range of amplitudes. Applying the two-fold sampling technique would reduce the impact of low-frequency noise on the sensor output. Within the allowed range of sensor output, the proposed device has a tolerance of 1% of error. The idea utilizes 0.25-micron CMOS technology from TSMC. Long Yan and colleagues [12] investigated low-power cardiac rhythms using an integrated circuit and a 13 uA conventional signal processor. This method utilizes an ASIC for DSP processing that runs on low power to improve bio-impedance monitoring speed and provide accurate cardiac arrhythmia detection. Most of these features should reduce weight, improve transmission evaluations, and boost power capacity in the next pacemaker devices.

Rezaeiyan et al. [13] designed a 4.2-MHz integrated circuit for cell stimulation, bio signal evaluation, and bioimpedance detection. To record cardiac pulses, they used an energy/frequency converter with a body voltage approximation. The proposed system employs volume control pipelines and two stages to produce PWM signals. Technology and architecture are the two main areas into which the literature review divides techniques. The architectural approach modifies circuits to support scaling technologies, while the technical approach necessitates a new circuit-building process. The literature covers many strategies for addressing the design issues related to low supply voltages. The authors have developed modern technological advancements and effective circuit designs to address CMOS submicron technology problems without adding complexity.

M. Ashraf et al. [14] demonstrated the effective energy conversion and use of an implanted pacemaker. Functional block-based (FBB) technology enables circuit construction. The circuit shows a 2.5 V output even with a large load. Provided with an input voltage of 40 mV, the circuit should show an approximate current voltage of 40 mV. The HSPICE measurements show that the suggested circuit is feasible and constantly agrees with framework expectations. Xu and colleagues [15] built a front-end circuit. Dynamic DC coupling increases the IA electrode's power and efficiency. At 50 Hz, the CMFF system maintains a constant CMRR of approximately 102 dB. Biological signals were analyzed using inter-variable procedures. By reducing the complexity and cost of computers, integrated circuits become very adaptable.

Yi-Ju Roh and colleagues [16] suggested using a faster ADC to shorten the MSB's decision time. We provide a lookup table-free approach to reducing metastability in non-binary SAR-ADCs. At 1 V, the 0.0128 mm ADC core draws 1.9 mW of power. Kiho Seong et al. corrected harmonic-related variations in sub-ADC sampling distortion [17]. Using a number of methods, one can modify the comparison offset. While guaranteeing that the ADC performance is unaltered, the proposed calibration technique successfully reduces noise, especially spurious signals. The authors used background noise for every calibration.

Jaehoon Lee et al. [18] designed the SAR ADC, which uses both fine and coarse comparator circuits in a two-step consecutive approximation register. This design maximizes the utilization of comparators and reduces the standard speed requirements through clock generator synchronization, resulting in energy conservation. Shruti Konwar et al. [19] developed a 12-bit binary-weighted SAR-ADC that uses self-subtractive randomized dithering to identify capacitor differences. Shruti Konwar and colleagues constructed a 12-bit SAR-ADC using 180-nanometer CMOS technology. The authors obtained an ENOB of 11.7 by sampling the ADC at an 8-megahertz frequency.

3. DESIGN OF SAR ADC FOR BIO-MEDICAL APPLICATIONS

The suggested 8-bit SAR ADC is made up of many parts, which are shown in Figure 1. These include a comparator, a sample and hold circuit, a digital-to-analog converter (DAC), and a SAR logic unit. Concurrent testing of the comparator design and the S/H circuits is necessary. The method aims to reduce power consumption and achieve 8-bit precision within the 1V voltage range.

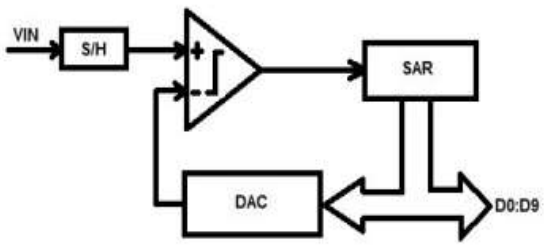

Figure 1: Description of SAR ADC

A. SAMPLE AND HOLD CIRCUIT:

Figure 4 displays an appropriate S/H circuit. The MOSFET transistors Mn1,2 and Mp1,2 act as switches. When the clock signal rises, the primary flipping transistor MnSW changes its gate supply voltage, and when the clock signal decreases, it loads the imbalance capacitors. Anytime its source potential

changes due to a large quantity of V_{GS}, the transistor MNSW retains full conductivity beyond the threshold voltage V_{TH}. MnSW and Mp2 gates have connections due to sampling; source voltages Vg and Mp2 typically surpass V_{DD}. Connecting the gate voltage to Vg, the circuit's threshold value, completely disables Mp2. By holding V_G to the circuit's lowest value, Mn4 disables MnSW. You can provide Mn3, but the Mn4 transistor stays inactive to prevent a high voltage drop. Because of its V_{DD} gate voltage, the Mn3 transistor is not very good as a pass transistor. As a result, V_{DD}-V_{TH} must equal Mn4's maximum drain voltage. A MOSFET, which becomes more and more important, can keep Vc constant throughout the sampling operation, but it needs a bigger area.

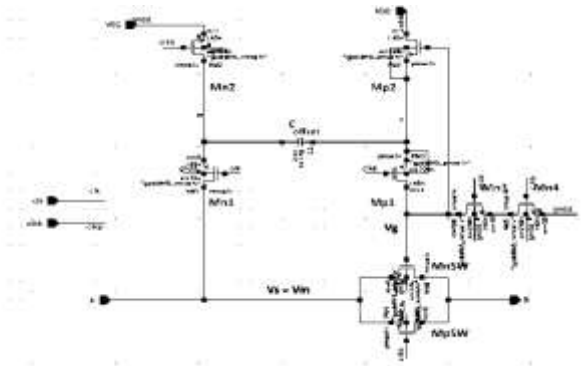

Figure 2: S/H Circuitry

B. DAC

A DAC converts digital information into an analog voltage level using SAR hardware. The comparator measures the voltage level. Traditional capacitance DACs employ charge dispersion. To achieve this, we employ a binary-weighted set of N capacitors. n Figure 3, there are two array capacitive differential operation digital-to-analog converters. DAC switches contain CMOS transmission gates, similar to input sampling switches. A switching network selects the DAC code and samples the input signal. Researchers often increase the width of NMOS and PMOS transistors to lower the transmission gate resistance (R_{ON}). But this approach is limited by growing parasitic capacitances. In a DAC, thermal effect noise and capacitance quantity are reciprocal. Increasing the unit capacitance, however, slows down the system. V_{XP} and V_{XN} are connected in the DAC design by more common-mode switches. Employing the bottom capacitance plates for every capacitor in the first stage of the conversion, the S switching sample is an input V_{IN} electrical signal. Connected to VCM is top plate Node V_X. The total charge of capacitors equals V_{IN} times for all available capacitance. The VCM and V_{IN} broke off the capacitors' top and bottom plates. As previously stated, the SAR logic's digital data modifies the bottom plate. After the initial comparison, we had to adjust the DAC coding to 10000000 by setting the MSB to 1.

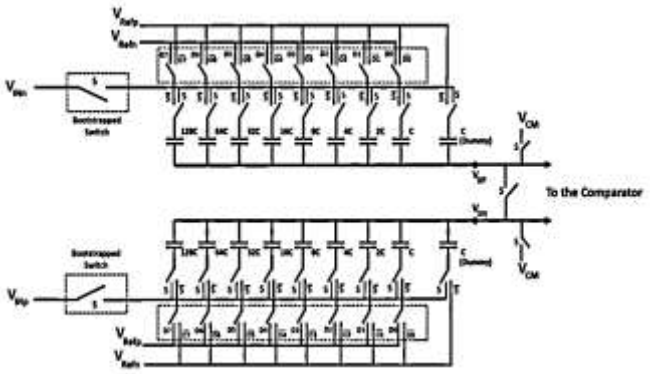

Figure 3: Topology of an 8-bit capacitance DAC.

Equation 1 shows that, unlike V_{CM}, the variation in V_X is caused by voltage division and charge distribution combined. That would be like matching the V_{IN} to half of the V_{REF}. When V_{IN} exceeds 50% of V_{REF} and V_X is less than zero, the comparison variable returns 1. If the comparator fails to meet this criterion, it provides a zero response.

$$\text{For DAC= 10000000, } \Delta v = \frac{4c}{4c+2c+c+c} \ldots\ldots\ldots 1$$

$$V_x = -V_{IN} + \Delta v = -V_{IN} + \frac{V_{ref}}{2} \ldots\ldots\ldots\ldots 2$$

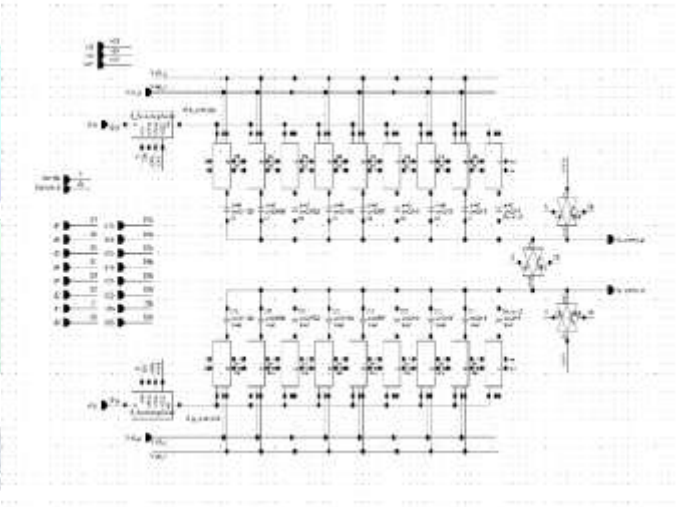

Figure 4: Realisation of the CMOS 8-bit DAC

In the above example, the MSB influences the comparator's final value, D2, while MSB-1 equals 1. V_{IN} comparison occurs separately from within the upper half of V_{REF} whenever D2 = 1, and inside the bottom half when D2 = 0. Throughout the assessment, the MSB-1 bit selects the current value for comparison D1, whereas the MSB-7 bit assigns 1. After eight comparisons, the binary code D7D6D5D4D3D2D1D0 indicates the voltage level of the VDAC. Figure 6 illustrates how node voltage fluctuations affect 8-bit DAC capacitor capacitance during conversion.

C. COMPARATOR

The single-tail comparator design originated from superior low-voltage performance. Numerous approaches to comparator development have been investigated.

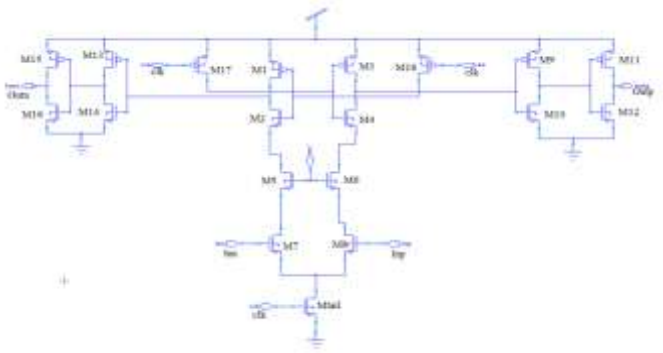

Figure 5: Proposed Comparator

The single-tail comparator design originated from better low-voltage performance. Researchers have investigated numerous approaches to comparator development. In terms of speed and optimization of power use, latch comparators outperform traditional comparators. The low-voltage medical implants may benefit from the circuit topology's improved input-output separation and reduced kickback noise. Figure 7 illustrates the idea architecture of the kickback noise reduction comparator. The comparator under study undergoes reset and analysis through clock control. We reset the transistor's tail zone by setting the clock (clk) to 0V. As such, VDD affects both output terminals. When the clock (clk) encounters VDD, the tail transistor discharges both of its terminals. A comparator's outputs change from zero to VDD and back again according to the inputs.

The parallel capacitors in this circuit serve the purpose of providing the sample and hold (S/H) function while simultaneously reducing thermal noise. By segregating comparator outputs, inverter buffers mitigate offset errors and minimize superfluous node capacitance. The comparison circuit reduces the number of transistors to conserve energy. When the voltage is below 0.6 V, the majority of MOS transistors in the structure operate within the weakest inversion region.

When the clock signal approaches VDD under stable operating conditions, kickback is evaluated. Kickback noise reduces the accuracy of ADC input waveforms. Figure 4 designs the switches M5-M6 to safeguard against potential voltage anomalies from the comparators at nodes Inp and Inn. When the comparator's reset clock signal is in a logic low state (clk=0), transistors M5 and M6 remain closed. Transistors M5 and M6 perform the function of segregating input data from outputs and inverter latches. Compared to Inp and Inn, the M5 and M6 significantly reduce kickback noise. During assessment, we keep transistors M5 and M6 open to isolate the inverted latch and outputs from incoming data. Comparators eliminate and balance the parasitical energy injection by selecting comparable logic values for the outputs Outp or Outn.

D. SAR DIGITAL CONTROL LOGIC

As claimed in [19] and [20], asynchronous control logic frequently achieves high speeds. However, PVT variations may have an impact on intrinsic logical signal transmission comparison cycles. Figure 5 depicts the synchronous system control methods used in this study. DAC switching signals are among the synchronous output codes that the control logic now generates. Creating control signals requires evaluating the system inputs (SAMPLE and CLK). According to comparator findings, SAR logic assigned digital codes to DACs. Digital circuits that use a binary search algorithm output an ADC result and an End of Conversion (EOC) message. Functioning together are unitary switches, shift registers, and other necessary parts. A latch saves comparator output; the shift register produces pulses; and the mixed switch signals the differentiating DAC. In this test, one conversion took 17 clock cycles. Figure 6 displays the SAR logic of the circuit.

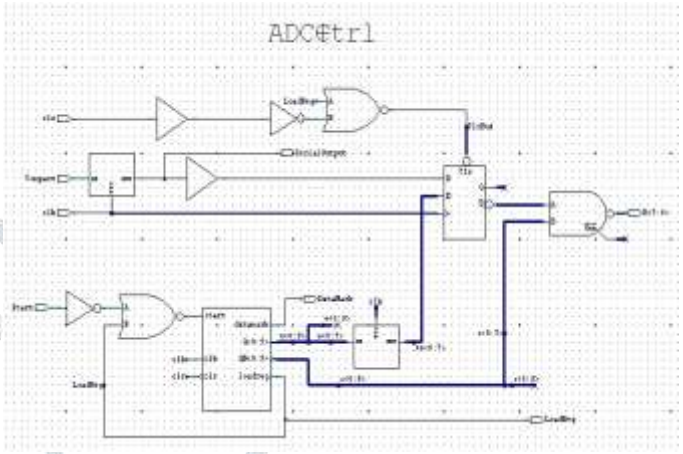

Figure 6: Circuit diagram of SAR Control Logic

4. SIMULATION RESULTS

We designed an 8-bit low-power SAR-ADC using 45nm CMOS semiconductor technology for use in biomedical implant devices. The design includes a revised comparator with the required SAR logic and a capacitance DAC.

Table 1: Results of DAC

Parameters	DAC_Out	DAC_DNL
Minimum	275.10m	-5.5
Average deviation	17.69m	1.9
Maximum	412.15m	4.29
Mean	357.10m	31.1m
Variance	433.80u	4.59
Standard deviation	33.69m	2.19

Table 1 displays DAC DNL measurements. Figure 7 shows schematic of SAR ADC.

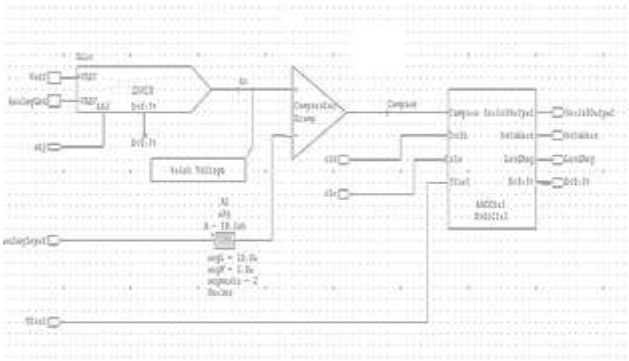

Figure 7: Implementation of 8-bit SAR-ADC

At 20.8 kS/s, the input's Nyquist rate, Figure 10, shows the 1024-point FFT spectrum. 59.16 dB is the SNDR, and 64.02 dB is the SFDR. ENOB is 9.53. Table 2 compares the features of SAR ADC performance to those from earlier studies. With the provided ADC, power consumption and other features are lower. The suggested ADC achieves good performance at 1.9 uW of power. The suggested approach results in an increase in SNDR. Figure 8 displays the SAR ADC's PSD.

The results suggest that the proposed ADC method could enhance the efficiency of the SAR ADC. Low-power and moderate-conversion-rate ADCs are useful in biology applications. The latest CMOS technology could improve performance. The suggested ADC finds numerous uses, as bio-implantable portable devices require the ability to detect analog signals. For these applications to extend battery life, low-power sensor connections are required.

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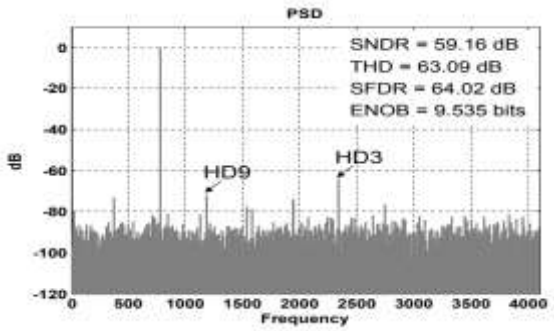

Figure 8: PSD function of SAR ADC

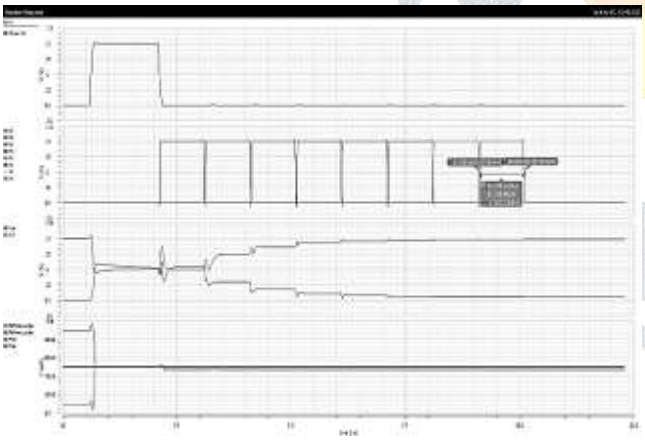

Figure 9: Transient simulation result of DAC

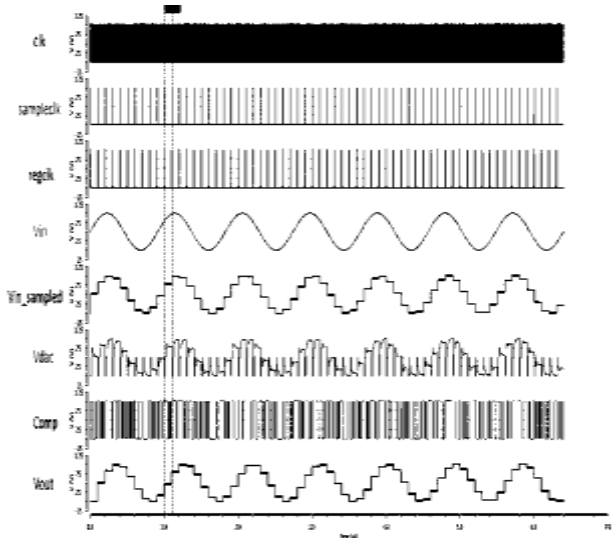

Figure 10: Transient simulation result of SAR-ADC

Figures 9 and 10 show transient outcomes of simulations for DAC and SAR ADC respectively.

Table 2: Comparison Performance of ADC

PARAMETERS	[18]	[19]	[20]	[21]	[22]	[23]	This Work
Technology (nm)	0.18	0.090	0.045	0.090	0.18	0.065	0.045
Resolution (bits)	10	13	14	14	18	14	8
Sampling rate (S/s)	110K	127K	6M	82M	10K	37M	1.1 MHz
Supply Voltage (v)	0.6	1.5	5	1.2	1	2.2	1
ENOB (bits)	12.6	11.6	12.1	13	-	11.8	9.53
SNDR(db)	56.9	69.1	74.4	79.1	-	71.3	59.16
SFDR(db)	82	84	90	87.1	-	80.3	64.02
Power(uw)	3.7	3.9	56.6	1.67	32.82	32.2	1.987

From the table 2, it is evident that proposed SAR provides lower power consumption when compared to current architectures of SAR –ADC. It also exhibits better performance characteristics when compared with existing architectures.

5. **CONCLUSION:**

In this study, the usage of a C-2C DAC results in a power-efficient switching mechanism, reducing switching energy significantly. SAR-ADC has the ability to provide outstanding linearity. Current study focuses on the offset property of a comparator operating in a weak-inversion scenario. We could have utilized Monte-Carlo simulation to verify the comparator's optimal configuration. The research shows that the comparator in this study was not created utilizing an offset-cancelling approach. This work describes a new switching technique and comparator for developing an 8-bit SAR-ADC with extremely low power consumption. We specifically designed the ADC for use in medically implantable devices. vices. We built the ADC in 45nm CMOS. The ADC runs at the input frequencies specified by the Nyquist criteria. It achieves an ENOB of 9.31

while consuming 1.9 uW of electricity. The ADC samples at a rate of 1.1 MS/s. The above-mentioned performance level indicates that the ADC has good energy efficiency.

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