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POWER OPTIMIZATION IN VLSI CIRCUITS USING MACHINE LEARN TECHNIQUES

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Abstract: Power optimization is a vital aspect of VLSI circuit design as it determines power consumption and directly influences device performance and battery life. Traditional methods such as clock gating, power gating and voltage scaling have been used to minimize power dissipation; however, they often lack accuracy and speed. In recent years, Machine Learning Techniques have emerged as a promising alternative to achieve efficient power optimization in VLSI circuits. This paper presents a detailed study of existing conventional and Machine Learning based approaches for power optimization, their methodologies, and comparative advantages.

Keywords: VLSI, power optimization, Machine learning techniques

I. INTRODUCTION

Power optimization is a critical requirement VLSI circuit design, as it directly influences power consumption and the battery life of devices. Effective power optimization significantly increases the life span of portable devices. In earlier stages, conventional methods
such as clock gating, power gating and voltage scaling were widely used to reduce power consumption. Although these methods improve power efficiency, they often lack accuracy and speed. Various abstraction levels such as system level, RTL level, gate level and transistor level are also employed to achieve desired results, but these approaches generally prioritize speed over accuracy.

To optimize the power consumption of VLSI circuits, several factors must be considered including the number of gates, logic levels, fan-out, number of flip-flops, switching activity and types of gates. In most VLSI circuits, power dissipation occurs primarily due to switching activity, glitches and leakage power.

Recent studies show that Machine Learning applications in power optimization yield superior results compared to traditional approaches. The adoption of Machine Learning techniques continues to grow due to their ability to improve both accuracy and efficiency.

This paper is organized into five sections.
In section I, we discuss the importance of power optimization in VLSI circuits.

In section II, we analyze fundamental techniques used for reducing power consumption.
In section III, we delve the details of general design automation.
In section IV we explore various ML methods applied for power optimization from the existing research papers.
In section V, we conclude the possible ML techniques for efficient power optimization and future prospects.

II.FUNDAMENTAL METHODS USED FOR POWER OPTIMIZATION

In an earlier research, several fundamental methods were employed to address power consumption issues. The major techniques are as follows;

i) Gate power control

VLSI circuits often contain large number of gates, which can lead to significant power consumption. To minimize power loss, , the substrate voltage in a gate region may be adjusted .However, this approach requires triple well fabrication, making it both costly and time- consuming.

i) Clock gating

Clock gating is one of the most common methods for power reduction. Since clock signals exhibit the highest switching activity, unnecessary clock propagation can be disabled in regions where it is not needed. This is achieved using Integrated Clock Gating. However, this technique may introduce timing delays in the circuit.

ii) Data latching

Glitches are another source of power consumption, caused by unnecessary circuit activity. To prevent this, unused latches can be used to hold the data. When the output is not required, input transitions should be avoided. However, this technique can introduce errors during the forbidden state of an SR flip-flop.

iii) Voltage scaling

Power consumption in CMOS gates is proportional to the square of the supply voltage. Reducing the supply voltage can decrease power dissipation but may degrade circuit performance. This limitation can be mitigated by introducing parallelism in the design.
Power improvement can be expressed as follows:

$P_n(n) = [1+C_i(n)\backslash nC_{ref} + C_x(n)/Cref](V/Vref)$,

Where, n is the number of parallel functional units,
V is the new supply voltage,
C_{ref} is the reference capacitance of the original functional unit,
C_i is the capacitance due to inter-processor communication, and
C_x is the capacitance due to the input\output multiplexing.

iv) Advanced Dynamic Voltage and Frequency Scaling(DVFS)

DVFS is used to control power consumption in microprocessors by dynamically adjusting the operating voltage and clock frequency. The power controller determines appropriate frequency and voltage settings to balance performance and power efficiency [1].

III. GENERAL DESIGN AUTOMATION IN POWER OPTIMISATION

In [2], Arun Tigathi discussed design automation tools and their benefits such as improved power optimization performance, reduced design cycle time, enhanced quality, and minimized human error. They also mentioned the tools used for simulation and synthesis includes Cadence Virtuoso, Synopsys, Mentor Graphics, Xilinx, Tanner and Alliance.
The author also highlighted the challenges in design automation including design complexity, quality assurance and reliability .
In [4], B. S. Vinay Kumar et al, reviewed bio-inspired optimization techniques for power optimization , focusing on various use cases of bio-inspired algorithm. However, this paper did not explore the potential of Machine Learning based approaches for improved power performance.

Linumon Thomas et al, focused on clock network optimization technique to reduce power consumption in digital circuits. They analyzed different clock network architectures and compared power consumption before and after optimization, reporting a 4.4515 mv power saving through clock network optimization method[7].
K. Abdul Munaf et al, surveyed various power optimization techniques other than clock network optimization and concluded that many discussed parameters are interrelated [8].

IV. MACHINE LEARNING APPROACHES FOR POWER OPTIMISATION IN VLSI CIRCUITS

Traditional approaches for power optimization in VLSI circuits are often time- consuming and complex, especially for large scale designs. Hence, Machine-Learning based methods, have gained attention due to their ability to learn complex relationships between design parameters and power metrics, achieving better prediction and optimization.

OVERVIEW OF MACHINE LEARNING

Machine Learning is one of the subsets of Artificial Intelligence and it can be classified into:

- Supervised learning,
- Unsupervised learning and
- Reinforcement learning.

Supervised learning method depends on output labels where unsupervised learning relies on an input variable. Reinforcement learning is based on trial and error.
In [3], Deepthi Amuru et al, explored AI and ML applications across VLSI design cycle from design specification to post silicon validation and highlighted positive potential of ML for power optimization.

Dharminder Kumar emphasized about the Mead-Conway approach, discussing both low power and high- performance VLSI design, Artificial Intelligence as the potential tool[10]

In [5], V. Govindharaj et al, presented an ML based power estimation in VLSI circuits, using supervised learning model such as Back Propagation Neural Network(BPNN) and Random Forests. Their comparative analysis demonstrated the effectiveness of ML in predicting and reducing power consumption.
Yassine Attaoui et al, explained the applications of Machine Learning in Electronic Design Automation and VLSI. They also discussed the challenges and limitations of applying ML in VLSI. Additionally, they suggested varying clock frequencies at different speeds to obtain the desired data [6].
Dr. Ayushi Arya highlighted the importance of power estimation prediction to achieve power optimization in VLSI circuits. The author compared traditional and advanced methods for predicting power estimation and explained the various parameters to collect datasets[10].
In [11], E. Poovannan et al, discussed different types of Machine Learning models such as Linear Least-Square Regression, Ridge Regression, K-NNR and Neural Network Regression. They used the Average Absolute Error (AAE) and Maximum Absolute Error analysis methods to evaluate accuracy of their proposed system. However, they restricted the testing methodologies due to time and resources restrictions in their research. Therefore, there remains scope for obtaining more accurate results if other methodologies are explored further.

V.CONCLUSION

Power optimization remains a fundamental challenge in VLSI design. Conventional methods such as clock gating, voltage scaling and power gating effectively reduce power but often compromise speed and accuracy. Machine Learning based techniques, however offer enhanced accuracy, scalability, cost-effective and adaptability. Supervised and ensemble learning models ensure reliable results in power optimization. Future research enable integrate Machine learning techniques into Electronic Design Automation workflows to achieve intelligent, automated and energy-efficient VLSI design

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