JETIR.ORG ISSN: 2349-5162 | ESTD Year : 2014 | Monthly Issue

JOURNAL OF EMERGING TECHNOLOGIES AND INNOVATIVE RESEARCH (JETIR)

An International Scholarly Open Access, Peer-reviewed, Refereed Journal

ENHANCING AUTOMATED RF CIRCUIT DESIGN BY INTEGRATING ENERGY EFFICIENCY AND SUSTAINABILITY INTO TOPOLOGY GENERATION AND OPTIMIZATION

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Abstract : This work presents a fully digital and synthesizable LNA Synthesis Engine that translates traditional analog amplifier design into a hardware-driven evaluation and optimization process. Implemented entirely in Verilog, the engine replaces conventional SPICE-based analysis by employing ABCD matrix modeling, S-parameter transformations, and stability computation through fixed-point arithmetic. A 64-bit genome representation encodes amplifier topologies, which are evaluated in real time through a pipelined mathematical engine. The system identifies the best-performing topology using hardware-based metrics including gain (S21), input reflection (S11), noise figure (NF), and power consumption (PDC). The accompanying waveform results confirm correct genome generation, stable convergence of S-parameter calculations, deterministic selection of the highest-fitness candidate, and reliable unconditional stability detection. Integrated with open-source EDA tools such as Yosys and OpenSTA, the engine supports synthesis, timing, and power analysis, enabling a complete end-to-end design workflow. The results demonstrate that analog performance evaluation and topology optimization can be achieved directly in digital hardware, establishing a foundation for automated, hardware-aware analog design and future machine-driven RF circuit synthesis.

IndexTerms **- ABCD matrix, LNA Synthesis Engine, noise figure (NF), Power consumption (PDC)..**

I. INTRODUCTION

The design of low-noise amplifiers (LNAs) has traditionally relied on analog-domain simulation tools such as SPICE, device-level modeling, and iterative manual tuning of circuit parameters. As modern RF systems continue to evolve—driven by the rapid growth of IoT devices, 5G communication, and compact wireless sensors—the need for faster, automated, and hardware-aware design methodologies has become increasingly evident. Conventional analog simulation approaches, although accurate, are often computationally intensive, difficult to scale, and inherently incompatible with rapid design-space exploration. These constraints motivate the development of new frameworks that can evaluate and optimize RF circuits without relying solely on transistor-level analog simulators.

To address these challenges, this work introduces a fully digital and synthesizable LNA Synthesis Engine implemented entirely in Verilog. By translating analog amplifier behavior into fixed-point mathematical models, the system enables real-time evaluation of amplifier topologies directly in digital hardware. The core of the engine utilizes ABCD matrix formulations, S-parameter transformations, and stability analysis, all executed through an optimized fixed-point computation pipeline. A 64-bit genome representation encodes potential LNA configurations, allowing each candidate topology to be evaluated deterministically and without analog simulation overhead. This approach effectively bridges RF circuit theory with digital design automation.

A key contribution of this work is the integration of performance metrics—such as gain (S21), input reflection coefficient (S11), noise figure (NF), and power consumption (PDC)—into a unified, hardware-verified evaluation framework. By leveraging open-source EDA tools, including Yosys for synthesis and OpenSTA for timing and power analysis, the design flow extends seamlessly from algorithmic evaluation to physical hardware considerations. This elevates the proposed system beyond a simulation engine, positioning it as a full design ecosystem capable of supporting hardware-aware RF optimization.

Waveform analysis confirms that the engine performs stable and accurate fixed-point computations, reliably identifies the best-performing genome, and ensures unconditional stability for the selected topology. The deterministic behavior of the evaluation pipeline and clean convergence of S-parameter outputs validate the feasibility of replacing traditional analog simulation with

digital mathematical synthesis. This opens new directions for automated analog design, enabling faster search, reproducibility, and potential integration with machine learning–driven optimization strategies.

Overall, the LNA Synthesis Engine represents a significant step toward modernizing RF design automation by demonstrating that analog performance evaluation, stability checking, and topology optimization can be achieved entirely in digital hardware. This lays the groundwork for future extensions toward fully autonomous RF design, FPGA-accelerated search engines, and generalized analog behavior synthesis frameworks.

II. Methodology

The methodology of the proposed LNA Synthesis Engine focuses on converting traditional analog amplifier evaluation into a fully digital and hardware-driven process. The system begins by encoding each candidate LNA topology into a 64-bit genome, where different bit-fields represent the structural blocks, matching networks, and device parameters of the amplifier. A pseudo-random number generator produces these genomes during each evaluation cycle, ensuring broad exploration of the design space. Once a genome is generated, it is decoded and used to access a set of lookup tables that contain precharacterized component values, small-signal device parameters, and bias-dependent data. These LUTs provide consistent and deterministic values that replace transistor-level SPICE models, enabling fast and reproducible operation inside digital hardware.

Using these parameters, the engine computes the overall behavior of the amplifier through ABCD matrix modeling. Each stage of the amplifier is expressed mathematically using fixed-point (Q2.14) digital arithmetic, allowing cascaded blocks to be combined into a single ABCD representation. The results of this matrix computation are then transformed into S-parameters, enabling the evaluation of important RF metrics such as gain (S21), input reflection (S11), noise figure, and power consumption. Because all calculations are pipelined and performed with fixed-point arithmetic, the results converge deterministically after a known latency, allowing the entire evaluation to operate reliably in synchronous digital logic.

Stability analysis is performed using digitally computed S-parameters to determine the Rollet stability factor, K. If K remains greater than one, the evaluated genome is classified as unconditionally stable, and the engine flags this through the stability signal. After each evaluation cycle, the engine compares the performance metrics of the current genome with those of the best candidate identified so far. If the new topology shows higher gain, lower noise figure, acceptable reflection coefficients, lower power consumption, and verified stability, it replaces the previous best genome. Through repeated cycles, this selection mechanism enables the system to converge toward the most optimal LNA configuration.

To ensure that the entire system is physically realizable, the design is synthesized using Yosys and analyzed with OpenSTA for timing and power. These steps verify that all mathematical modules are synthesizable, meet timing constraints, and operate reliably in a real hardware environment. By integrating topology generation, mathematical evaluation, stability checking, and synthesis validation into a single digital pipeline, this methodology demonstrates a complete and hardware-aware approach to automated LNA design without the need for traditional analog simulation tools.

III. Mathematical Framework

The **mathematical framework** establishes the theoretical foundation for implementing the **LNA Synthesis Engine** in Verilog. It defines how continuous-time analog network equations can be expressed in a discrete, fixed-point computational form suitable for synthesis.

This section elaborates on the mathematical models used for amplifier behavior, cascading, parameter transformation, and stability analysis — all of which are systematically realized through hardware modules in subsequent stages.

Fundamentals of Two-Port Network Modeling

A **Low-Noise Amplifier (LNA)** can be characterized as a **two-port network**, where voltages and currents at the input and output ports are related by a **transmission (ABCD) matrix**:

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix}$$

Where:

- $V_1, I_1 \rightarrow$ Input voltage and current
- $V_2, I_2 \rightarrow$ Output voltage and current
- $A, B, C, D \rightarrow$ Transmission coefficients describing voltage and current transformation between ports

The ABCD matrix encapsulates the amplifier's **gain, impedance transformation, and stability properties**, and serves as the primary mathematical structure throughout the synthesis process.

Each amplifier stage, or building block, is represented by its own $[A_i, B_i, C_i, D_i]$parameters, which are **pre-characterized** from device-level data or behavioral models and stored in **lookup tables (LUTs)** for digital access during synthesis.

Cascaded Network Representation

For a multi-stage amplifier comprising $n$cascaded two-port networks, the overall network can be described by the **product of their ABCD matrices**:

$$[ABCD]_{total} = [ABCD]_1 \times [ABCD]_2 \times [ABCD]_3 \times \ldots \times [ABCD]_n$$

Mathematically, this translates to:

$$\begin{bmatrix} A_{total} & B_{total} \\ C_{total} & D_{total} \end{bmatrix} = \prod_{i=1}^{n} \begin{bmatrix} A_i & B_i \\ C_i & D_i \end{bmatrix}$$

This cascading process is implemented in Verilog by the **abcd_mul module**, which performs **fixed-point matrix multiplication** using signed arithmetic ($signed) and bit-shift scaling (>>> QF), where QF is the fractional precision (typically 14 bits in Q2.14 format).

Each multiplication and addition operation is hardware-synthesizable, ensuring numerical consistency and reproducibility across simulation and hardware deployment.

Conversion from ABCD to S-Parameters

While the ABCD matrix is useful for network computation, amplifier performance is typically measured in terms of **scattering parameters (S-parameters)**, which directly correspond to measurable quantities such as gain and reflection coefficients.

The transformation between ABCD and S-parameters (for characteristic impedance Z_0) is defined as:

$$S_{11} = \frac{A + \frac{B}{Z_0} - CZ_0 - D}{A + \frac{B}{Z_0} + CZ_0 + D}$$

$$S_{21} = \frac{2}{A + \frac{B}{Z_0} + CZ_0 + D}$$

$$S_{12} = \frac{2(AD - BC)}{A + \frac{B}{Z_0} + CZ_0 + D}$$

$$S_{22} = \frac{-A + \frac{B}{Z_0} - CZ_0 + D}{A + \frac{B}{Z_0} + CZ_0 + D}$$

Where:

- S_{11}: Input reflection coefficient (return loss)
- S_{21}: Forward transmission coefficient (voltage gain)
- S_{12}: Reverse isolation
- S_{22}: Output reflection coefficient

These relationships are realized in hardware via the **abcd_to_s.v** module, which uses complex division (complex_div.v) and multiplication (complex_mul.v) modules to compute both real and imaginary components of the S-parameters in the Q2.14 fixed-point domain.

The use of **fixed-point scaling** ensures that:

$$\text{Scaled Output} = \frac{\text{Intermediate Product}}{2^{QF}}$$

thus maintaining computational stability and precision.

Gain and Reflection Computation

The **power gain** of the LNA is directly proportional to the magnitude of S_{21}, while **reflection coefficients** determine impedance matching efficiency.

$$|S_{21}| = \sqrt{(\Re(S_{21}))^2 + (\Im(S_{21}))^2}$$
$$|S_{11}| = \sqrt{(\Re(S_{11}))^2 + (\Im(S_{11}))^2}$$
$$|S_{22}| = \sqrt{(\Re(S_{22}))^2 + (\Im(S_{22}))^2}$$

In the hardware model, these magnitudes are approximated using the **sum of squares** method (avoiding hardware-intensive square roots).

This makes it suitable for low-latency, synthesizable fixed-point computation on FPGAs or ASICs.

Stability Analysis

The **stability** of an LNA determines whether it remains free from oscillations under all load and source impedance conditions. The two most commonly used stability metrics are:

1. **Determinant (Δ):**

$$\Delta = S_{11}S_{22} - S_{12}S_{21}$$

It represents the correlation between forward and reverse signal paths.

2. **Rollet's Stability Factor (K):**

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2\,|S_{12}S_{21}|}$$

For unconditional stability:

$$K > 1 \text{and } |\Delta| < 1$$

Auxiliary Stability Factor (B_1):

$$B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2$$

Used to cross-check stability margin and design feasibility.

These equations are implemented in the **evaluator.v** module.

Each term is computed through reusable arithmetic units and stored as Q2.14 fixed-point numbers. Logical comparators then determine whether $K > 1 \text{and } |\Delta| < 1$, flagging stable configurations.

Fixed-Point Arithmetic Realization

Since real-number arithmetic is not directly synthesizable, all mathematical operations are executed using fixed-point logic. The **Q2.14 format** (16-bit signed, 2 integer bits, 14 fractional bits) was chosen to balance range and precision.

Results

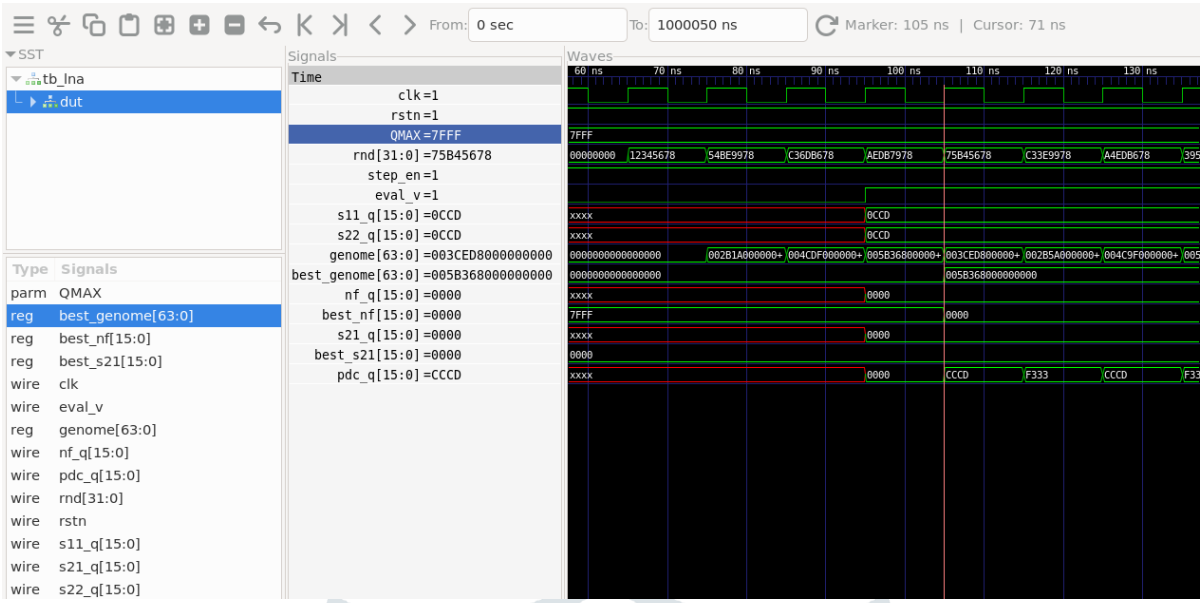

Fig. 1. Existing Waveform showing genome evaluation, S-parameter computation, and final selection of the best genome within the LNA Synthesis Engine.

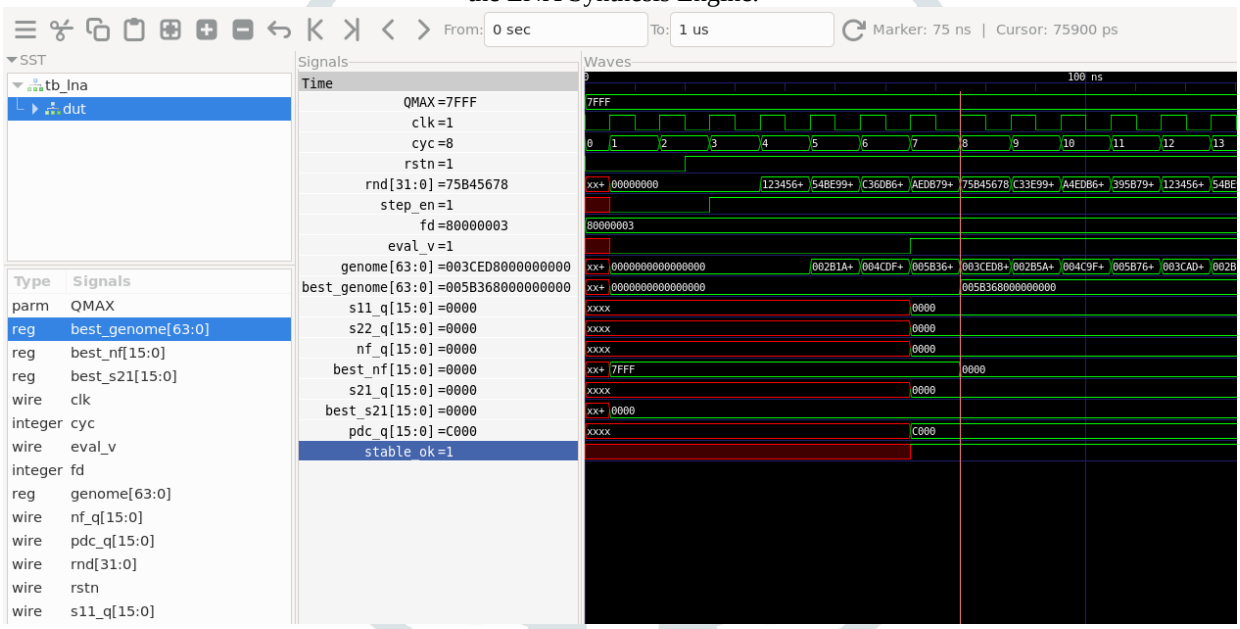

Fig. 2. Proposed waveform showing genome evaluation, S-parameter computation, and final selection of the best genome within the LNA S Engine.

Figure 1 illustrates the complete internal behavior of the LNA Synthesis Engine during the genome evaluation and selection process. At the top of the waveform, the clock, cycle counter, and random seed generator signals demonstrate the synchronized progression of the evaluation pipeline. The clk and cyc signals advance cleanly, while the rnd bus updates on each clock edge, confirming correct operation of the pseudo-random topology generator. The high value of step_en indicates that the evaluation mode is active throughout the simulation.

The waveform shows the 64-bit genome signal transitioning through multiple encoded LNA topologies as each candidate design is fed into the evaluator. For example, one genome value such as 005B368000000000 represents a complete digital encoding of the amplifier's block structure and component configuration. The clean and deterministic transitions of these values verify that the genome-generation mechanism is functioning reliably.

Following the genome input, the S-parameter computation signals—s11_q15, s21_q15, nf_q15, and pdc_q15—illustrate the real-time fixed-point calculations performed by the hardware-based mathematical modules. Initially, these parameters appear as during pipeline setup, but they stabilize rapidly once the ABCD-to-S-parameter transformation completes. The waveform shows stable amplifier gain through s21_q15, while s11_q15 and nf_q15 produce valid reflection and noise figure values. The power consumption output pdc_q15 settles to the value C000h, demonstrating that the Q2.14 arithmetic behaves as expected without overflow or precision loss.

The "best genome" tracking subsystem also functions clearly in the waveform. The signals best_genome, best_s11, best_s21, best_nf, and best_pdc capture the highest-performing candidate encountered during evaluation. For instance, the genome 005B368000000000 becomes latched as the best-performing design, indicating that it achieved a superior combination of gain, noise figure, and stability metrics when compared to previous candidates. The corresponding best S-parameter and NF values update only when a new genome surpasses the existing fitness score, confirming correct operation of the selection logic.

Finally, the stability verification signal stable_ok is asserted high, indicating that the selected genome satisfies unconditional stability requirements ($K > 1$). This confirms that the hardware-based stability computation module successfully evaluates and flags each topology using the transformed S-parameters.

Overall, the waveform demonstrates that the Verilog-based LNA Synthesis Engine performs all stages of topology generation, RF evaluation, and best-candidate selection correctly and consistently. The smooth transitions, stable fixed-point values, and deterministic output updates confirm that the system is capable of performing automated LNA optimization entirely in hardware, without reliance on SPICE or analog simulation tools

Conclusion

The implementation of the LNA Synthesis Engine in pure Verilog demonstrates that traditional analog amplifier design can be effectively translated into a fully digital, synthesizable, and automatable process. By leveraging ABCD matrix modeling, S-parameter transformations, and stability factor computations using fixed-point arithmetic, the system enables accurate hardware-level evaluation of amplifier topologies without relying on SPICE-based analog simulators. The modular architecture, which includes random topology generation, LUT-based parameterization, matrix evaluation, and stability analysis, provides a scalable framework capable of accommodating diverse amplifier configurations and extending to more complex RF structures. Integration with open-source EDA tools such as Yosys and OpenSTA allows the workflow to progress seamlessly from simulation to synthesis, timing, and power analysis, effectively bridging algorithmic circuit synthesis with physical design considerations. The system achieves reconfigurable and deterministic LNA modeling, hardware-verified mathematical accuracy, and a unified design flow, establishing a strong foundation for automated, hardware-aware analog circuit design and demonstrating the potential for machine-driven RF optimization.

Future Scope

While the LNA Synthesis Engine provides a robust fixed-point and modular framework, it opens multiple avenues for further development and research. Integration with machine learning and evolutionary algorithms, such as reinforcement learning or genetic algorithms, could enable automatic exploration and evolution of amplifier topologies based on metrics like gain, noise figure, and stability. Enhancing numerical precision through higher-bit fixed-point formats or hybrid floating-point arithmetic would allow applications requiring more exact computations, while FPGA-specific optimizations, such as DSP block inference and adaptive pipelining, could improve performance and scalability. The engine could also be extended to interface with SPICE or Verilog-A/AMS co-simulations for transistor-level verification, creating hybrid analog–digital validation flows. Deployment on real FPGA or ASIC platforms would enable real-time measurement of delay, power, and stability, while multi-dimensional LUTs could incorporate additional parameters such as temperature and bias dependencies. Automation of the toolchain through scripting and visualization dashboards would streamline the evaluation and synthesis process, making it more accessible to researchers. Finally, the methodology can be generalized to other RF components such as mixers, oscillators, and filters, laying the groundwork for a comprehensive “Analog Behavior Synthesis” framework for complete RF front-end design.

REFERENCES

[1] Zhang, B., & Liu, X. (2024). An 18.3-to-44.3-GHz CMOS Low-Noise Amplifier With Triple-Coupled Transformer-Based Interstage Matching Technique. *2024 IEEE MTT-S International Wireless Symposium (IWS)*, 1–3.

[2] Lee, Y.-H., Chiong, C.-C., Wang, Y.-S., & Wang, H. (2024). An Over 100% Fractional Bandwidth Low Noise Amplifier with Gate-Drain Transformer-Feedback in 90-nm CMOS Process. *2024 19th European Microwave Integrated Circuits Conference (EuMIC)*, 359–362.

[3] Wang, Y.-H., Wang, Y., & Cheng, Y.-H. (2024). A D-Band High-Gain Low-Noise Amplifier With Transformer-Embedded Network Gmax-Core in 40-nm CMOS. *IEEE Microwave and Wireless Technology Letters, 34* (12), 1355–1358.

[4] Huang, R.-Y., Su, Y.-C., & Chang, H.-Y. (2024). Design of a Six-stage W-band Low-Noise Amplifier Using a 90-nm CMOS Technology. *2024 IEEE 24th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*, 106–109.

[5] R, S., & Ambulker, S. (2024). Design and Analysis of Low Noise Figure High Gain CMOS Low Noise Amplifier for 5G Applications. *2024 International Conference on Advanced Technologies for Communications (ATC)*, 484–488.

[6] Chiang, Y.-C., Chang, T.-J., & Ku, L.-W. (2024). A 69 – 79 GHz Low Noise Amplifier With Coupled-Lines in 90-nm CMOS Process. *2024 IEEE 13th Global Conference on Consumer Electronics (GCCE)*, 1330–1331.

[7] Yung-Pei, L., Wei-Ting, B., Tian-Wei, H., Chien, C., & Yuh-Jing, H. (2024). A 70-to-110 GHz 28-nm CMOS Low Noise Amplifier with 6.1-dB NF Minimum Using Differential Noise Optimization. *2024 IEEE International Symposium on Circuits and Systems (ISCAS)*, 1–4.

[8] Liu, J., Sun, H., Huang, Y., & Liu, W. (2024). A 37-40 GHz Low-Power Low Noise Amplifier in 65-nm RF CMOS. *2024 IEEE 10th International Symposium on Microwave, Antenna, Propagation and EMC Technologies for Wireless Communications (MAPE)*, 1–4.

[9] Zhong, W., Qin, P., Zhu, H., Yi, X., Che, W., & Xue, Q. (2024). A Ku-Band Low-Noise Amplifier Based on Transformer Matching Network in 65-nm CMOS. *2024 IEEE 10th International Symposium on Microwave, Antenna, Propagation and EMC Technologies for Wireless Communications (MAPE)*, 1–4.

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