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AREA EFFICIENT AND HIGH SPEED FULL ADDER ARCHITECTURE USING X-NOR AND XOR BASED LOGIC IN 45NM CMOS TECHNOLOGY

KELLA SUDHA [1], ***N.CHANDRASEKHAR*** [2]

[1]*M.Tech Student, Department of Electronics & Communication Engineering, Avanthi St.Theressa Institute of Engineering and Technology, JNTU-GV University, Vizianagaram, India*
[2]*Assosciate Professor, Department of Electronics & Communication Engineering, Avanthi St.Theressa Institute of Engineering and Technology, JNTU-GV University, Vizianagaram, India*

ABSTRACT

A Binary Full Adder is a critical component in microprocessor and digital signal processor data pipelines since it is used in almost all arithmetic operations. It serves as the foundation for critical activities like as multiplication, division, and addresses computation for cache or memory accesses, and is typically integrated into arithmetic logic units and floating-point units. As a result, improving their speed has significant implications for high-performance applications. This paper emphasizes the fundamental function of addition in digital computer systems and presents three new gate-level complete adder architectures. These designs are created using components from a typical cell library: the first uses XNOR and multiplexer gates (XNM), the second combines XNOR, AND, Inverter, multiplexer, and complex gates (XNAIMC), and the third uses XOR, AND, and complex gates. These designs are compared to several existing gate-level complete adder implementations. The XNM-based full adder was recognized as area-efficient, whilst the XNAIMC-based full adder demonstrated a moderate mix of speed and area efficiency when compared to the other two designs. The circuit was successfully developed and constructed utilizing the Tanner EDA tool and 45nm technology.

Keywords: Combinational Logic, Full Adders, XNOR, X0R, XNAIMC, Tanner EDA tool 45nm Technology

I. INTRODUCTION

Current trends in innovation and creativity in designing equipment or devices require an emphasis on certain qualitative recognition by designing processors such as high-end computers and portable design applications (PDAs), which play an important role in the development of modern electronic technology. The use of these electronic gadgets is rising on a daily basis, and they have become a vital part of every human life. Research in the sector is ongoing, and designers are working hard to produce new gadgets that have low power consumption, are tiny in size, high in speed, and energy efficient. Most electrical systems are made up of arithmetic circuits, and an adder is the essential building block for any ALU operation such as addition, subtraction, and multiplication. Thus, power and delay are the two most important performance characteristics in any electronic circuit. Nonetheless, upgrading the speed adder design and increasing the adders' performance would considerably improve the overall system operation. The primary goal of creating an area-efficient and high-speed full adder is to create an efficient arithmetic unit that executes binary addition with little latency and maximum power usage. The circuit's implementation of the adder at the gate level utilizing synchronous design principles enables precise timing control and speedier operation, which is critical for high-performance digital systems such as processors, signal processors, and communication devices. This design seeks to increase speed, decrease propagation latency, and improve overall computing efficiency. The impetus for building an area

efficient and high speed full adder originates from the requirement for quicker and more efficient arithmetic operations in modern digital systems. Full adders are the essential building blocks of processors, ALUs, and other computational devices. As technology improves, there is an increased desire for high-performance computing with low latency and power consumption. The complete adder, which focuses on gate-level implementation and synchronous design, can improve speed, timing accuracy, and overall system performance, making it suited for real-time processing, embedded systems, and advanced computing architectures.

II LITERATURE SURVEY

C. Senthilpari al in [1], have introduced a fresh and inventive method to multiplier design that strives to achieve minimal power consumption while maintaining excellent performance. This study makes a substantial contribution to the field of digital multiplier design by introducing a new full-adder cell that combines MCIT and Shannon-based approaches, as well as applying it to various multiplier kinds and conducting comprehensive performance evaluations.

S. Goel al in [2], have introduce a hybrid CMOS logic approach for full adder design that can create both XOR and XNOR full-swing outputs at the same time. This revolutionary design technique is based on a novel XOR-XNOR circuit, which considerably improves the energy efficiency and reliability of the complete adder. The suggested design beats various conventional full adders in terms of power consumption and drive capabilities without sacrificing performance.

Y. Jiang al in [3], have constitutes an important addition to the realm of digital circuit design, particularly for low-power VLSI systems. The MBA-12T adder, with its novel design and verified performance benefits, establishes a new benchmark for full adder designs that prioritize energy conservation and high speed operation.

A.M. Shams al in [4], have a detailed investigation of numerous low-power 1-bit CMOS full adder cells was conducted, with a focus on power consumption, speed, and area. The work is organized to provide a thorough comparison of various adder cell designs, emphasizing their respective strengths and drawbacks. This involves an assessment of both traditional and new adder cell designs, with the goal of determining the most efficient and effective digital circuit solutions.

Chandran Venkatesan al in [5], have analyzed a 1-bit full adder utilizing various ways in Cadence 45nm Technology. The goal of this study is to reduce the power, latency, and stability factor of a full adder by utilizing various 1bit full adder designs and methodologies. Here, 10T complete adder circuits using CMOS technology show the lowest power usage compared to others.

III PROPOSED METHOD

This paper proposes three distinct full adder designs. The initial design only used XNOR gates and 2:1 multiplexers, with one of the two non-inverting 2:1 Multiplexers having an inverted input. Figure 1 illustrates this setup, which is known as the XNM-based full adder. The second adder design is an improvement on the previous full adder design, characterized by the replacement of the AND gate in the second half adder module and the OR gate related to the carry output with a single complex gate, the AO12 cell, as depicted in Figure 2, and is known as the XAC-based full adder. Figure 3 depicts the final adder design, which features XNOR, AND, NOT, an inverted input 2:1 MUX, and complicated gates. The AO12 cell is used as a complex gate to execute the function f = xy + z, where 'x' and 'y' are the AND logic inputs and 'z' is a separate OR logic input.

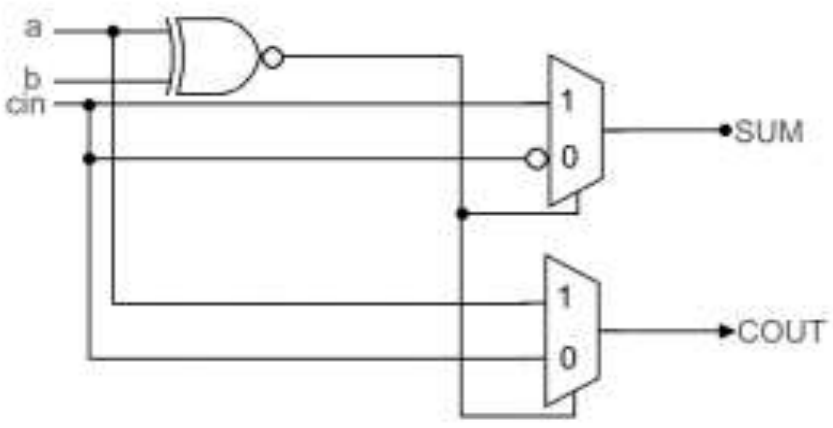

Figure 1: Proposed XNM based full adder

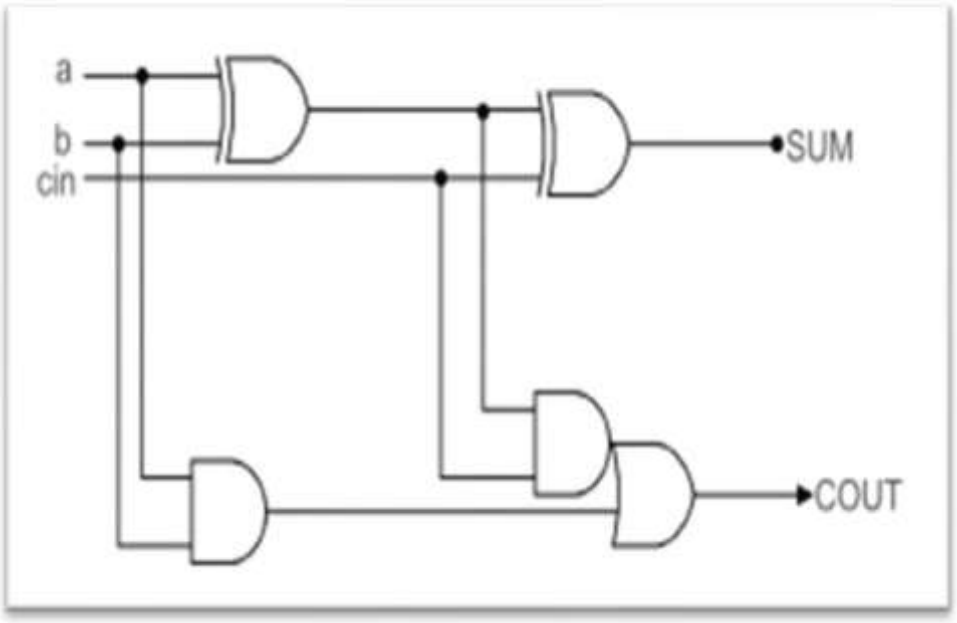

Figure 2: Proposed XAC based full adder

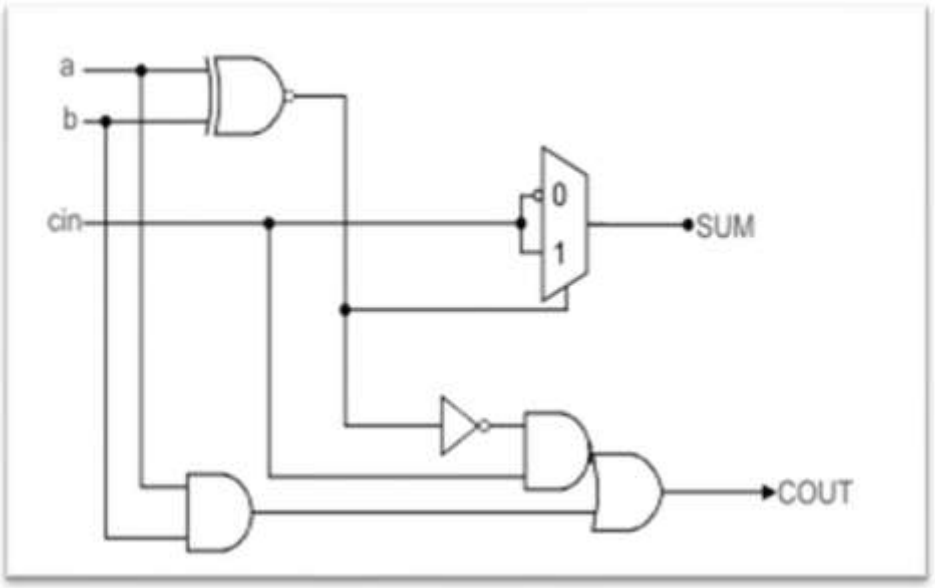

Figure 3: Proposed XNAIMC based full adder

The paper emphasizes the importance of addition in computer architecture and proposes three novel designs for gate-level fully additive circuits (full adders) based on a standard cell library. The first of these systems, called XNM, is based on XNOR and multiplexer gates. The second, XNAIMC, ensures balance by utilizing a range of gate types, including XNOR, AND, inverter, multiplexer, and other sophisticated logic gates. Finally, the third design, XAC, relies on XOR, AND, and sophisticated logic gates to boost performance while focusing on speed. Each of the proposed adders has been comprehensively benchmarked against a large number of gate-level complete adders. Benchmarking entails embedding each of the full adders into a 32-bit carry ripple adder, testing performance at three different PVT (process, voltage, and temperature) corners with high-speed (low-Vt) 65 nm STMicroelectronics CMOS technology, and evaluating performance using propagation delay. Benchmarking findings show that the full adder based on the XAC architecture has the smallest propagation delay of all the studied designs, including those based on current standard library full adder cells. The XNM design has the smallest area footprint, while the XNAIMC is a very good performance-to-area tradeoff among the other designs.

IV SOFTWARE RECQUIRED

Tanner Electronic Design Automation (EDA) Tool is widely used in custom analog/mixed-signal (AMS) IC design. This tool has been successfully applied to new technology nodes such as 45nm by adding specific process technology files (BSIM models), allowing for the assessment of circuit performance, low power consumption (Adders), and functional verification prior to the fabrication process. Tanner Designer is a complete analogue verification management environment that records all the simulations employed in a given project. The Tanner suite of products contains tools used for schematic capture, circuit simulators, and waveform development, along with the full-custom layout editor. Electronic Design Automation (EDA) falls under the hardware, software, service, and process category of computer-aided design and assists in building up complex electronic systems, for example, Printed Circuit Boards, Integrated Circuits, and Microprocessors. According to EDA, the main application of these tools allow you to analyze data prior to drawing conclusions, such as identifying errors, trends, outliers/oddities, and potentially interesting relationships between variables before revealing some level of confidence in the findings.

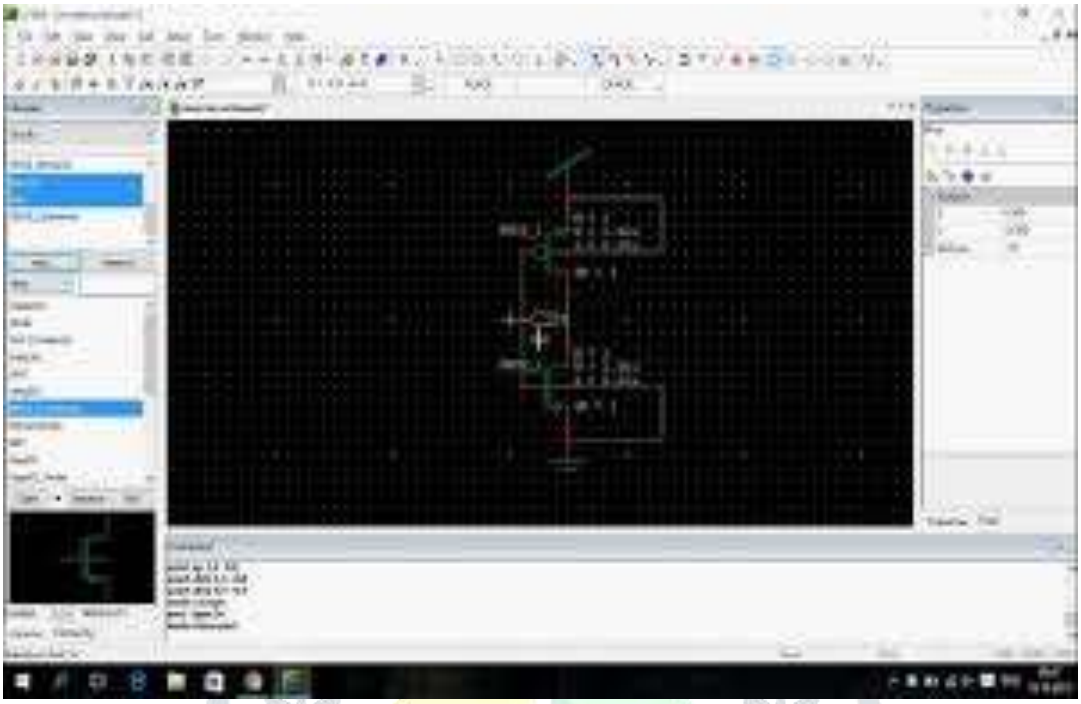

Figure 4: Tanner EDA Tool

V RESULTS

Figure 6 depicts the Proposed Schematic XAC full adder, which was constructed using a novel structure of integrated XOR, AND, and Carry Logic Functions to minimize overall complexity and boost efficiency by sharing classified intermediate values on the sum and carry routes. Optimized logic results in lower power consumption and increased speed. The design shown here is scalable and can meet the performance requirements associated with higher-end VLSI application designs.

Proposed Schematic XNM Full Adder is illustrated in Figure 7 and is built on a new framework, XOR-NOT-Multiplexing Logic. The adder architecture generates sum and carry outputs with less logic modification than traditional adders, providing a more efficient method of generating these outputs. Improved routing of the signals reduces both total power consumption and propagation delay significantly. This design provides a small and fast adder topology for use in low power very large scale integrated (VLSI) applications.

Figure 8 depicts the Proposed Schematic XNMAIC Full Adder, which uses an Advanced XOR/NOT/MUX Structure and an Optimized AND/INVERTER Complex (XNMAIC) method to enable for efficient sum and carry operations. By reducing the amount of Logical Transition events, the XNMAIC creates a Small, High-Performance, Low-Power VLSI (Very Large Scale Integration) solution with an Optimized Routing Design that decreases power consumption and propagation times.

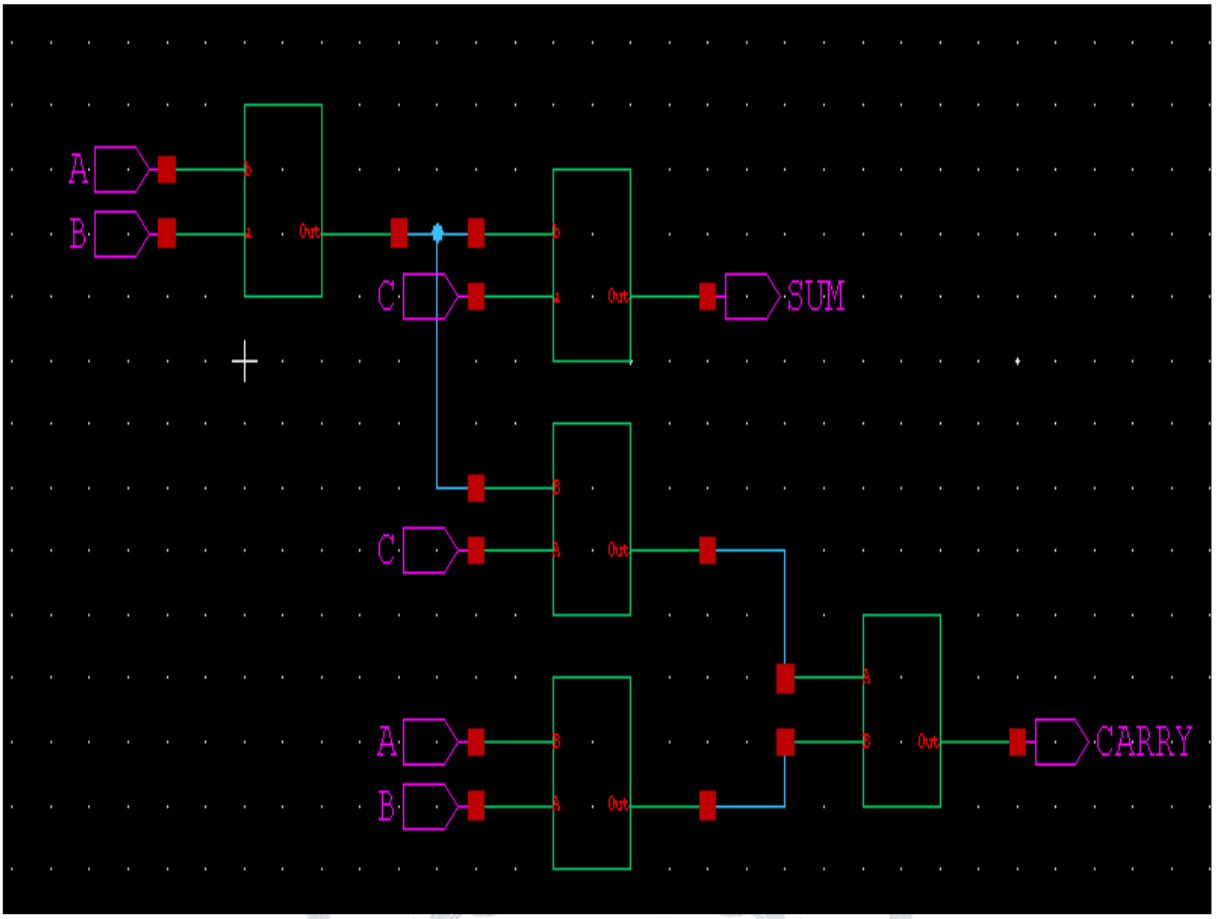

Figure 6: Schematic of Proposed XAC Based Full Adder

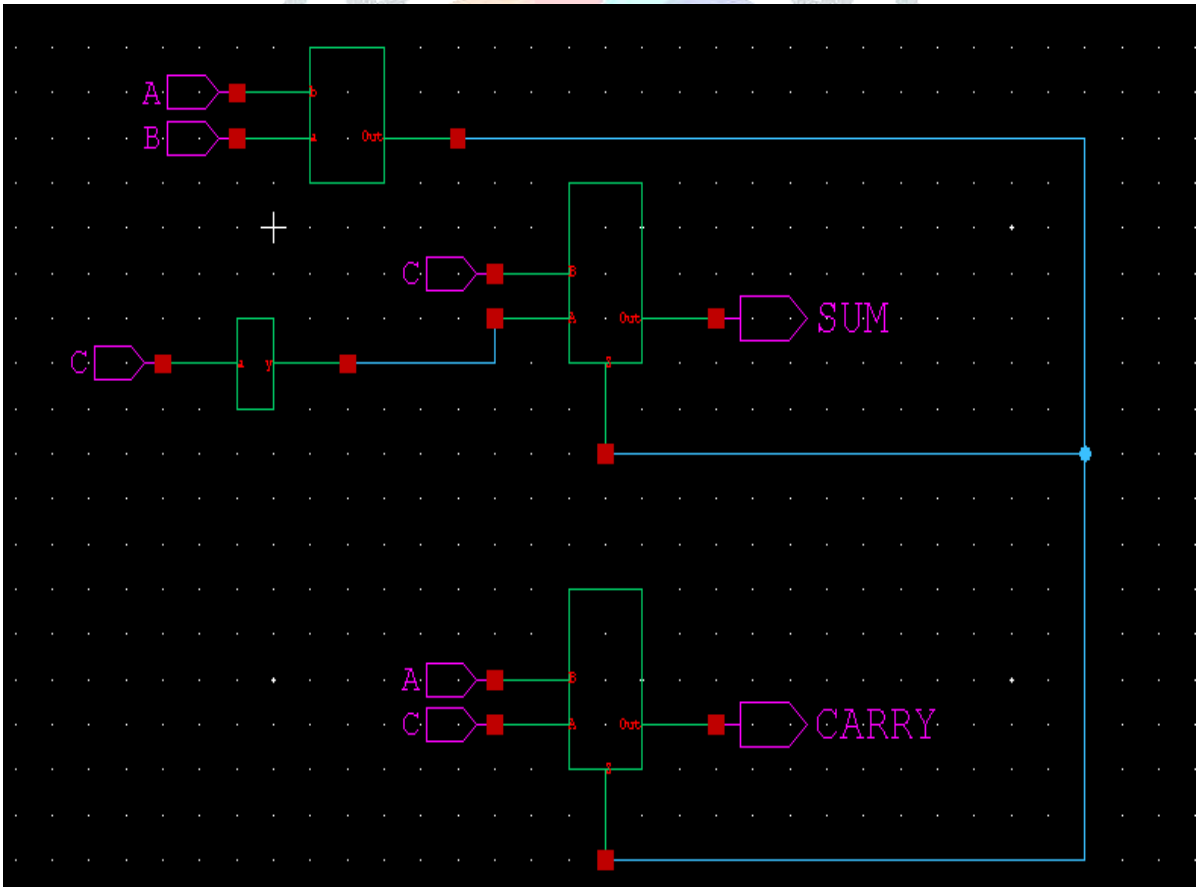

Figure 7: Schematic of Proposed XNM Based Full Adder

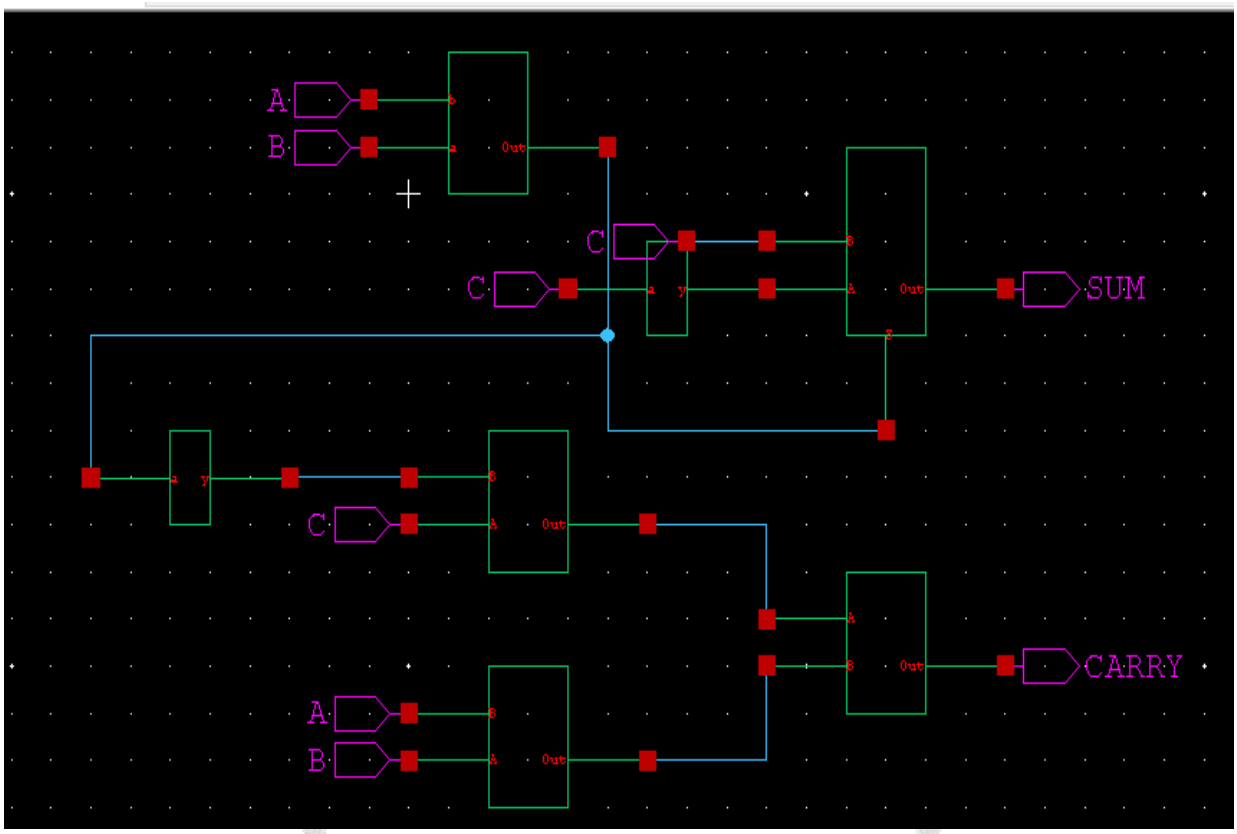

Figure 6: Schematic of Proposed XNAIMC Based Full Adder

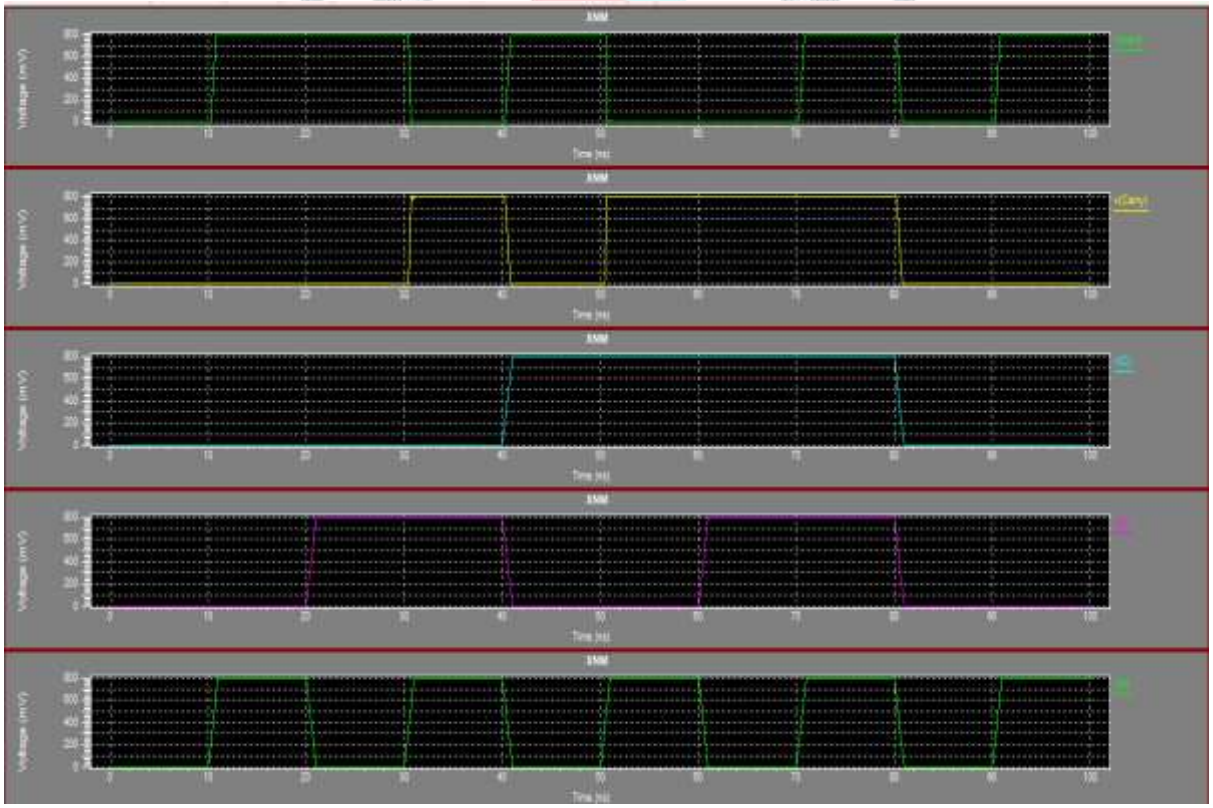

Figure 9: Waveforms of Proposed Full Adder Designs

VI RESULT ANALYSIS

The Proposed full adder designs are contrasted in Table 1 according to area, latency, and power consumption. The efficiency of the XNM design is demonstrated by its lowest transistor count (38), fastest latency (0.032 ns), and lowest power consumption (3.907 µW). Compared to XAC and XNAIMC, which need more transistors (46) and have higher latency (0.159 ns) and power consumption (5.62 µW), XNM is a more energy-efficient and compact solution for low-power VLSI applications.

Parameter	Area (Transistor Count)	Delay (ns)	Power (uw)
XNM	38	0.032	3.907
XAC	46	0.159	5.616
XNAIMC	46	0.159	5.62

Table 1: Comparison of Proposed Full Adder designs in terms of transistor count, propagation delay, and power consumption.

VI CONCLUSION

This paper presents three novel gate-level full adder designs: XNM, XNAIMC, and XAC. The XAC-based full adder has the fastest speed, while the XNM-based full adder is the most space-efficient. In terms of latency, the XNAIMC-based adder and the XAC-based adder are nearly identical. Notably, the XAC-based full adder surpasses the full adder cell in a commercial standard cell library, demonstrating its higher performance. The hybrid adder can be altered in the future to serve as a multiplier, subtractor, compressor, and sequential circuit. Since the proposed designs have demonstrated effectiveness in a number of performance metrics, it is anticipated that more successful outcomes will be attained when integrating these circuits to implement other intricate systems in the field of low power VLSI design.

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