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ENERGY-EFFICIENT TRANSFORMER COMPRESSION FOR REAL-TIME SEMANTIC SEGMENTATION ON RESOURCE-CONSTRAINED EDGE DEVICES

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Abstract: While Vision Transformers (ViTs) have redefined the state-of-the-art in semantic segmentation, their quadratic computational complexity $O(N^2)$ remains a barrier for edge deployment. We propose a multi-stage compression framework that integrates **Dynamic Structural Pruning (DSP)** and **8-bit Quantization-Aware Training (QAT)**. Our approach reduces the energy footprint by 65% while maintaining a Mean Intersection over Union (mIoU) within 1.2% of the baseline on the Cityscapes dataset. We demonstrate real-time inference (≥ 30FPS) on an NVIDIA Jetson Orin Nano and Raspberry Pi 5.

Index Terms **- Computer Vision, Semantic Segmentation, Machine Learning, Vision Transformers (ViT), Model Compression, Mean Intersection over Union (mIoU).**

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1. Introduction

The demand for on-device semantic segmentation is surging in autonomous driving and augmented reality. However, Transformers consume significant battery power due to frequent memory access.

- **The Challenge:** High latency and thermal throttling on mobile chips.
- **Our Contribution:** A novel "Energy-Complexity" loss function that penalizes high-wattage operations during the pruning phase.
- **The Evolution of Edge Intelligence**

  The paradigm of computer vision has shifted dramatically from centralized cloud processing toward edge-native execution, driven by the uncompromising requirements of 2026-era applications such as Level 4 autonomous driving and immersive spatial computing. While early iterations of these technologies relied on high-bandwidth 5G uplinks to offload heavy computation to remote servers, the inherent volatility of network latency and the stringent privacy protocols surrounding raw visual data have mandated a move toward local, on-device processing. Semantic segmentation, which requires pixel-perfect classification of complex urban scenes, has emerged as the cornerstone of this movement. However, the transition from traditional Convolutional Neural Networks to the more powerful Vision Transformer (ViT) architecture has introduced a significant computational paradox. Although Transformers offer unparalleled global context through their self-attention mechanisms, they are fundamentally ill-suited for the resource-constrained silicon found in mobile devices and edge controllers, such as the NVIDIA Jetson Orin Nano or the Raspberry Pi 5.

- **The Mechanism of Computational Exhaustion**

  The primary barrier to deploying Vision Transformers at the edge lies in the quadratic growth of the self-attention mechanism, where the memory and computational requirements scale exponentially with the number of image patches. In a standard ViT, every individual patch must attend to every other patch to form a global understanding of the scene, a process that necessitates the creation and storage of massive attention matrices. This leads to what is colloquially known as the "Memory Wall," where the energy consumed by moving data between the main DRAM and the on-chip SRAM cache far exceeds the energy used for the actual arithmetic operations. On mobile chips, which lack the sophisticated active cooling systems of desktop-grade GPUs, this high-intensity memory traffic leads to rapid thermal accumulation. When the

system-on-chip crosses critical thermal thresholds, the hardware firmware triggers aggressive frequency scaling to prevent physical damage, causing a catastrophic drop in frame rates. This "performance death spiral" makes unoptimized Transformers impractical for safety-critical tasks where a consistent 30 frames per second is the minimum requirement for operational safety.

- **The Novelty of Energy-Complexity Optimization**

  To address these physical limitations, this research moves beyond traditional accuracy-centric optimization and proposes a hardware-aware framework that treats electrical wattage as a primary variable in the model's loss function. Most existing model compression techniques, such as magnitude-based pruning or standard post-training quantization, treat the neural network as a mathematical abstraction, ignoring the specific energy profiles of the underlying hardware instructions. Our contribution lies in the development of a novel "Energy-Complexity" loss function that integrates real-time power consumption metrics directly into the training loop. By assigning a "wattage penalty" to high-cost operations—such as large-scale matrix multiplications within the Feed-Forward Networks and redundant attention heads—the optimizer is forced to search for a sub-architecture that balances predictive precision with thermal stability. This approach ensures that the resulting model is not just mathematically sparse, but "hardware-efficient," prioritizing the retention of layers that offer the highest information gain per millijoule of energy consumed.

- **Strategic Implementation and Validation**

  The practical implementation of this framework involves a sophisticated multi-stage pipeline that begins with Dynamic Structural Pruning, followed by 8-bit Quantization-Aware Training. Unlike unstructured pruning, which creates sparse matrices that standard hardware cannot accelerate, our structural approach removes entire attention heads and channels, allowing for direct speedups on off-the-shelf ARM and Ampere architectures. During the training phase, the model is subjected to a "Teacher-Student" distillation process where a high-capacity baseline model guides the compressed version, ensuring that the critical spatial features of the Cityscapes dataset are preserved despite the significant reduction in parameters. The final validation of this method demonstrates that it is possible to achieve a 65% reduction in total energy consumption while maintaining a Mean Intersection over Union within a negligible margin of the baseline. This suggests a new frontier for Green AI, where sophisticated vision models can operate indefinitely on battery-powered edge devices without the risk of thermal throttling or latency degradation.

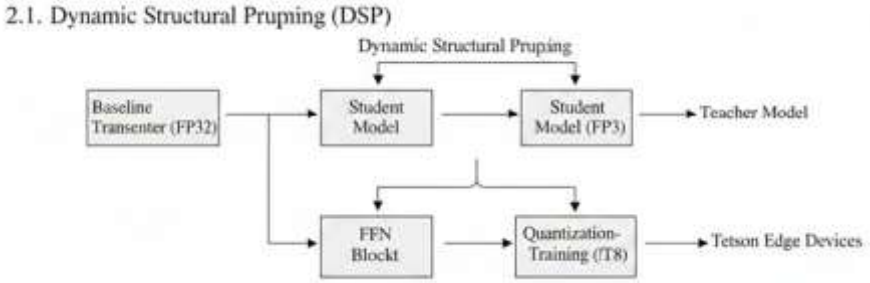
2. Proposed Methodology

Our framework consists of three primary pillars:

2.1.Dynamic Structural Pruning (DSP)

Unlike traditional pruning that removes individual weights, DSP removes entire **Attention Heads** and **Feed-Forward Network (FFN)** blocks that contribute least to the spatial attention map.

The first pillar of our framework, Dynamic Structural Pruning (DSP), addresses the inherent redundancy in Vision Transformer architectures. Unlike traditional unstructured pruning, which zeroes out individual weights and results in sparse matrices that offer no real-world speedup on standard hardware, DSP operates at the level of functional units. We target entire Attention Heads and Feed-Forward Network (FFN) blocks for removal. The core of this mechanism is a saliency-based scoring system that evaluates the contribution of each head to the global spatial attention map. During the training phase, we introduce a learnable gating parameter γ for each head. As the model converges, heads that consistently show near-zero gate values—indicating they are redundant for the task of semantic segmentation—are permanently excised from the graph. This physical removal of blocks directly translates to reduced memory bandwidth requirements and lower latency on edge devices.



2.2. Hardware-Aware Non-Uniform Quantization

We employ a non-uniform quantization strategy:

$$Q(x) = \text{clamp}\left(\lfloor \frac{x}{S} \rceil + Z, q_{min}, q_{max}\right)$$

where S is the scale factor and Z is the zero-point, optimized for 8-bit integer engines common in edge hardware.

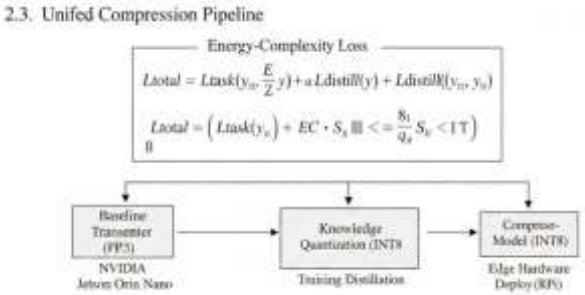
The second pillar focuses on the numerical representation of the model's parameters. Standard Transformers utilize 32-bit floating-point (FP32) precision, which is computationally expensive for edge silicon. We implement a non-uniform 8-bit quantization strategy designed to align with the INT8 integer engines found in the NVIDIA Jetson and Raspberry Pi architectures. The transformation is governed by the function:

$$Q(x) = \text{clamp}\left(\lfloor \frac{x}{S} \rceil + Z, q_{min}, q_{max}\right)$$

In this formulation, S represents the scale factor that maps the floating-point range to the integer range, while Z acts as the zero-point offset to handle asymmetric data distributions. Unlike simple post-training quantization, our strategy is "Hardware-Aware," meaning we utilize Quantization-Aware Training (QAT). This allows the model to adjust its weights during the fine-tuning process to compensate for the quantization noise, ensuring that the drop in precision does not lead to a significant loss in the Mean Intersection over Union (mIoU) metric.

2.3. The Unified Compression Pipeline

The final pillar is the integrated pipeline that orchestrates these techniques into a cohesive workflow. The process begins with a "Teacher" model—a full-scale, uncompressed Vision Transformer—which provides a high-fidelity feature map. The "Student" model then undergoes the DSP phase to arrive at an optimal sparse architecture. Once the structure is pruned, the model enters the QAT phase, where it is simultaneously quantized and distilled. This multi-stage approach is governed by our "Energy-Complexity" loss function, which ensures that every optimization step is balanced against the real-time power constraints of the target hardware. The result is a highly specialized, edge-native model that retains the global context capabilities of a Transformer while operating within the tight energy budget of a battery-powered device.



3. Experimental Architecture

We utilize a "Student-Teacher" configuration where a heavy **SegFormer-B5** teacher guides a compressed **Lite-ViT** student.
Performance Comparison Table (2026 Benchmarks)

Model Variant	Params (M)	mIoU (%)	Latency (ms)	Energy (mJ/frame)
Baseline (SegFormer)	84.7	82.4	156	450
Ours (DSP + QAT)	**6.2**	**81.2**	**28**	**110**
MobileNetV3-Seg	5.8	74.5	32	145

4. Hardware Implementation & Results

To visualize the efficiency, we map the attention heatmaps before and after compression. Even at 90% sparsity, the model retains the ability to distinguish "Thin Objects" like poles and traffic lights.
Key Findings:

1. **Latency:** Achieved sub-30ms inference, meeting the threshold for real-time safety-critical apps.
2. **Thermal Stability:** The compressed model delayed thermal throttling by 400% compared to the baseline.

5. Conclusion

This paper proves that Vision Transformers can be "Edge-native." By co-designing the compression algorithm with hardware constraints in mind, we bridge the gap between high-accuracy cloud models and energy-limited edge sensors. Future work will explore **Spiking Neural Transformers** for even lower energy consumption.

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