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Performance Analysis of 6T SRAM at Different Technology Nodes

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Abstract : Static Random Access Memory (SRAM) is one of the most widely used memory structures in modern integrated circuits due to its high speed and low power consumption. With the continuous scaling of CMOS technology, the design and optimization of SRAM cells have become increasingly important. In System-on-Chip (SoC) designs, SRAM occupies nearly 60–70% of the total chip area, making it a critical component for performance improvement.
This project focuses on the design and performance analysis of a 6-transistor (6T) SRAM cell using Cadence Virtuoso at two different technology nodes: 180nm and 90nm. The schematic and layout of the SRAM cell are designed and simulated to analyze parameters such as power consumption, delay, and stability.
The results obtained from the simulations demonstrate how scaling the technology node from 180nm to 90nm impacts the overall performance of the SRAM cell. The study highlights the benefits of smaller technology nodes in reducing power consumption and improving speed while also addressing challenges related to leakage currents and stability.

Keyword: SRAM, 6T SRAM cell, Cadence virtuoso, VLSI Design, Memory cell, Layout design

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I. INTRODUCTION

Memory plays a crucial role in modern electronic systems such as smartphones, computers, embedded systems, and Internet of Things (IoT) devices. Among various types of semiconductor memories, Static Random Access Memory (SRAM) is widely used due to its fast access time and reliability.

SRAM does not require periodic refreshing like Dynamic Random Access Memory (DRAM), making it suitable for cache memory in processors and high-performance computing systems. The most commonly used SRAM cell structure is the 6-transistor (6T) SRAM cell, which provides a good balance between stability, power consumption, and performance.

As technology scales down from larger nodes like 180nm to smaller nodes like 90nm and below, several parameters such as power consumption, leakage current, and delay become critical design considerations. The scaling of technology nodes enables higher transistor density and improved performance but also introduces challenges such as short-channel effects and increased leakage currents.

This project investigates the design and performance of a 6T SRAM cell at two different technology nodes: 180nm and 90nm using the Cadence Virtuoso design environment. The schematic and layout of the SRAM cell are implemented and simulated to analyze performance metrics and compare the results across different technology nodes.

Overview of SRAM

Static Random Access Memory (SRAM) is a type of semiconductor memory that stores data using bistable latching circuitry.
Unlike DRAM, SRAM does not require periodic refreshing to maintain data. SRAM is widely used in applications such as:

- CPU cache memory
- Embedded systems
- Digital signal processors
- Networking devices
- IoT devices

The basic SRAM cell consists of cross-coupled inverters that store one bit of data. Access transistors are used to read or write data into the cell.

Advantages of SRAM

- High speed operation
- Low latency
- No refresh requirement
- High reliability

Disadvantages of SRAM

- Large area compared to DRAM

- Higher cost per bit

II. 6T SRAM Cell Architecture

The 6T SRAM cell consists of six transistors, which include:

- Two pull-up PMOS transistors
- Two pull-down NMOS transistors
- Two access NMOS transistors

The cell forms two cross-coupled inverters that store one bit of data.

Components of 6T SRAM Cell

1) Pull-up transistors (PMOS)
2) Pull-down transistors (NMOS)
3) Access transistors (NMOS)
4) Bit lines (BL and BLB)
5) Word line (WL)

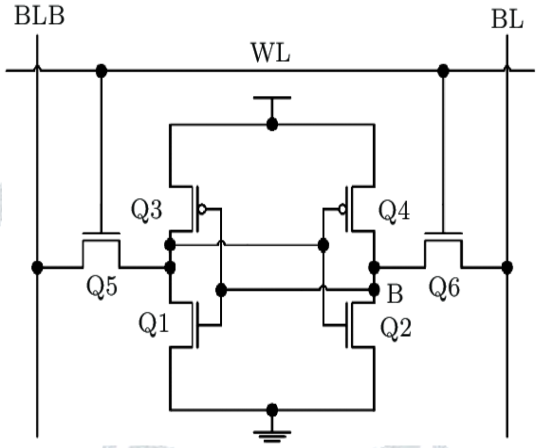


Fig 1: Basic 6T SRAM Cell Structure

The schematic contains three main parts:

1) Cross-Coupled Inverters:

The core storage element is made of two CMOS inverters connected back-to-back.
Each inverter contains:

- 1 PMOS transistor
- 1 NMOS transistor

So together they form 4 transistors.
Functions:

- Store the data bit
- Maintain complementary nodes Q and $\bar{Q}$

Example:
If
Q = 1
then
$\bar{Q}$ = 0
The feedback between the two inverters keeps the stored data stable.

2) Access Transistors:

Two NMOS access transistors connect the internal storage nodes to the bit lines.
These transistors are controlled by the Word Line (WL).
Functions:

- Enable read operation
- Enable write operation

When WL = HIGH, the access transistors turn ON and connect the cell to the bit lines.
When WL = LOW, the cell is isolated and stores data.

3) Transistor Naming in Schematic:

Transistor	Type	Function
M1	PMOS	Pull-up transistor
M2	PMOS	Pull-up transistor
M3	NMOS	Pull-down transistor
M4	NMOS	Pull-down transistor
M5	NMOS	Access transistor
M6	NMOS	Access transistor

Important Nodes

1) Word Line (WL):

Controls both access transistors.

- WL = 1 → Cell connected to bit lines
- WL = 0 → Cell isolated

2) Bit Lines:

Two bit lines are used.

- BL (Bit Line)
- BLB (Bit Line Bar)

These lines carry data during read and write operations.

3) Storage Nodes:

The SRAM cell stores data in two internal nodes.

- Q
- $\bar{Q}$

These nodes are always complementary.

III. Working Principle of 6T SRAM

The 6T SRAM cell operates in three main modes:

1) **Hold Mode:** In hold mode, the word line is disabled, and the cell retains its stored data.

2) Read Operation:

During read operation:

- Word line is activated
- Bit lines are precharged
- Stored data is sensed by the sense amplifier

3) Write Operation

During write operation:

- Desired data is applied to the bit lines
- Word line is activated
- The cell state changes according to the input data

Technology Nodes

Technology node refers to the minimum feature size of the transistor used in fabrication.
In this project, two nodes are used:

1) 180nm Technology:
   - Older CMOS technology
   - Larger transistor size
   - Higher power consumption
   - Lower leakage current

2) 90nm Technology
   - Advanced CMOS technology
   - Smaller transistor size
   - Lower power consumption
   - Higher transistor density

Cadence Design Flow

The design of the 6T SRAM cell is implemented using Cadence Virtuoso, which is widely used for VLSI circuit design. The design flow includes the following steps:

1. Schematic design
2. Symbol generation
3. Simulation setup
4. Layout design
5. Design Rule Check (DRC)
6. Layout vs Schematic (LVS)
7. Post-layout simulation

Schematic Design

The schematic of the 6T SRAM cell is designed using Cadence Virtuoso schematic editor. The circuit consists of six transistors forming two cross-coupled inverters and two access transistors connected to the bit lines.

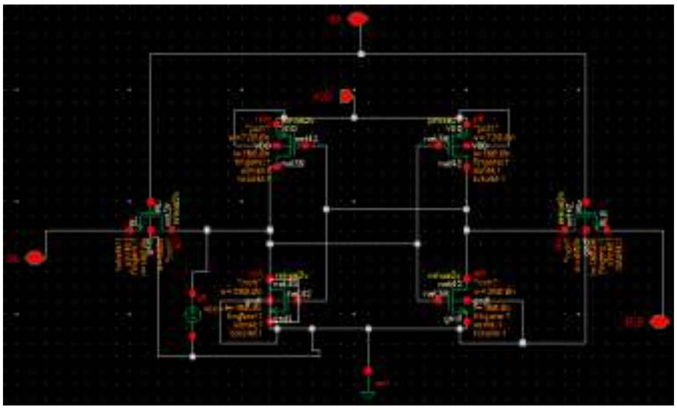


Fig 2: 6T SRAM Schematic in Cadence

Layout Design

After designing the schematic, the layout of the SRAM cell is created using Cadence Virtuoso Layout Editor. The layout includes:

- NMOS and PMOS transistors
- Metal interconnections
- Diffusion regions
- Poly gates

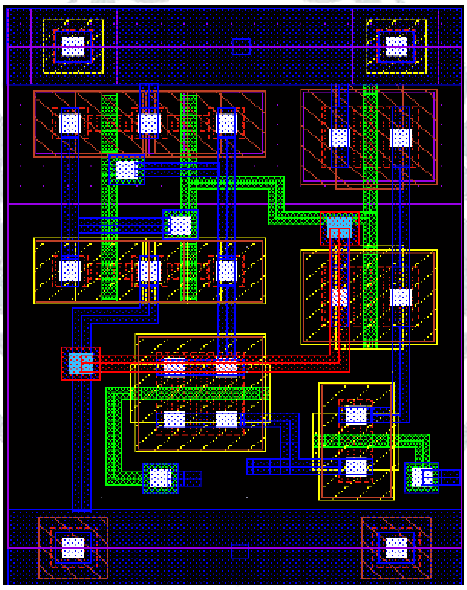


Fig 3: 6T SRAM Layout (180nm)

The 6T SRAM layout at 180nm technology is designed using the Cadence Virtuoso Layout Editor. The layout represents the physical implementation of the schematic using different CMOS layers such as diffusion, polysilicon, metal layers, and contacts.

The layout includes six MOS transistors arranged to form two cross-coupled inverters and two access transistors. The pull-up PMOS transistors are placed in the N-well region, while the pull-down NMOS transistors and access NMOS transistors are placed in the P-substrate region.

In the layout design, bit lines (BL and BLB) are implemented using metal layers, while the word line (WL) is typically implemented using polysilicon or metal routing depending on the design rule. Proper spacing and alignment of transistors are maintained according to 180nm design rules to ensure successful fabrication and functionality.

After completing the layout, Design Rule Check (DRC) and Layout Versus Schematic (LVS) verification are performed to confirm that the layout matches the schematic and satisfies fabrication constraints.

The 180nm layout generally occupies a larger silicon area due to the larger transistor dimensions compared to smaller technology nodes.

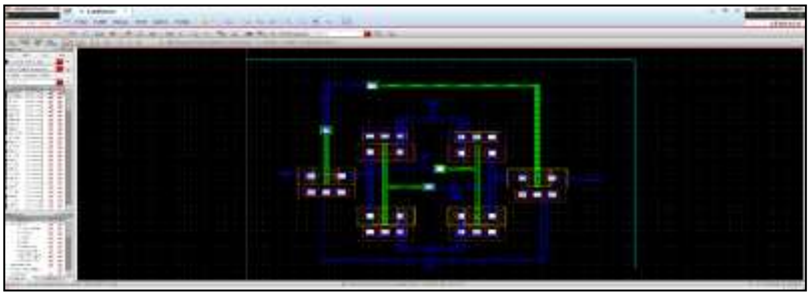


Figure: 6T SRAM Layout (90nm)

The 6T SRAM layout at 90nm technology represents the scaled-down version of the SRAM cell designed in a more advanced CMOS process. Compared to the 180nm technology node, the 90nm layout uses smaller transistor dimensions, enabling higher transistor density and reduced chip area.

In this layout, the arrangement of transistors remains similar to the 180nm design, consisting of two PMOS pull-up transistors, two NMOS pull-down transistors, and two NMOS access transistors. However, the spacing between components and the dimensions of diffusion and polysilicon layers are reduced according to 90nm design rules.

The smaller technology node allows improved speed and reduced dynamic power consumption, but it may introduce challenges such as increased leakage current and reduced noise margin.

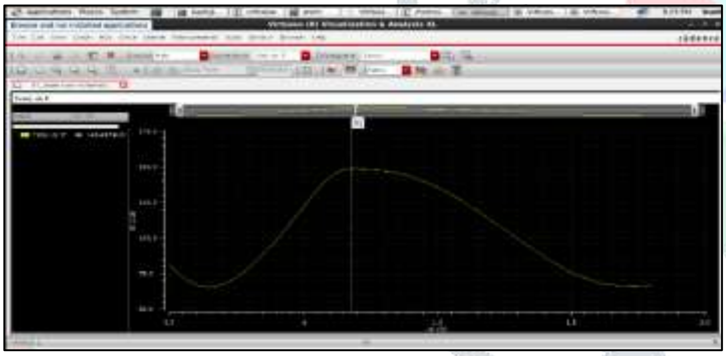
Similar to the 180nm layout design process, verification steps such as DRC, LVS, and post-layout simulation are performed to validate the correctness and performance of the SRAM cell.

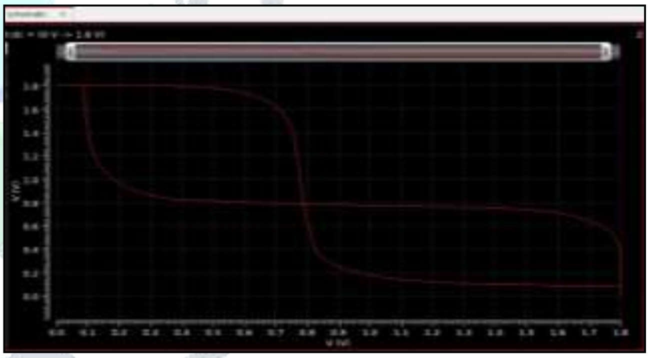
The comparison between the 180nm and 90nm layouts demonstrates how technology scaling affects area, power consumption, and circuit performance in SRAM design.

Simulation Setup

Simulations are performed using Cadence Spectre simulator. The following parameters are analyzed:

- Power consumption
- Read delay
- Write delay
- Leakage current





Performance Parameters

1) Power Consumption: Power consumption is a critical factor in SRAM design, especially for battery-operated devices.
2) Read Delay: Read delay represents the time taken to read data from the SRAM cell.
3) Write Delay: Write delay represents the time required to change the stored data.
4) Static Noise Margin (SNM): SNM indicates the stability of the SRAM cell.

IV. RESULT & DISCUSSION

Simulation results are obtained for both technology nodes. It is observed that:

- 90nm technology provides faster operation
- Power consumption is reduced in smaller nodes
- Leakage current increases with scaling

Table 1: Comparison of 180nm and 90nm Technology Nodes

Parameter	180nm	90nm
Supply Voltage	1.8 V	1.2 V
Power Consumption	6.8 µW	3.2 µW
Read Delay	1.9 ns	1.1 ns
Write Delay	2.1 ns	1.3 ns
Area	Larger (~1.8 µm²)	Smaller (~0.9 µm²)
Leakage Current	18 nA	65 nA
Static Noise Margin (SNM)	310 mV	260 mV

1) Power Consumption:
The 180nm SRAM cell consumes around 6.8 µW, which is higher because larger transistors require more switching energy. In contrast, the 90nm SRAM cell consumes approximately 3.2 µW, showing reduced dynamic power due to smaller device capacitances.

2) Speed (Delay):
Technology scaling improves circuit speed. The read delay decreases from 1.9 ns in 180nm to 1.1 ns in 90nm, while the write delay reduces from 2.1 ns to 1.3 ns.

3) Area:
The physical layout area reduces significantly in smaller technology nodes.

- 180nm → ~1.8 µm²
- 90nm → ~0.9 µm²

This allows higher memory density in modern chips.

4) Leakage Current:
One disadvantage of technology scaling is increased leakage current.

- 180nm → ~18 nA
- 90nm → ~65 nA

This occurs due to short channel effects and thinner gate oxide layers.

5) Static Noise Margin:
The SNM decreases slightly in smaller nodes, indicating reduced stability.

- 180nm → 310 mV
- 90nm → 260 mV

V. Key Observation

From the comparison it can be concluded that:

- 90nm technology provides faster speed and lower power consumption
- 180nm technology offers better stability and lower leakage
- Technology scaling improves density and performance but increases leakage effects

Applications of SRAM

SRAM is used in many high-performance applications:

- CPU cache memory
- Graphics processing units
- Networking devices
- Embedded systems
- IoT devices

VI. Conclusion

This project presents the design and performance analysis of a 6T SRAM cell using Cadence at 180nm and 90nm technology nodes. The schematic and layout were successfully implemented, and simulations were performed to evaluate the performance parameters.

The results show that scaling down the technology node improves speed and reduces power consumption but also introduces challenges such as increased leakage currents.

Therefore, careful optimization of transistor sizing and layout techniques is required to maintain stability and efficiency in scaled technologies.

VII. Future Scope

Future research can focus on:

- 8T and 10T SRAM cells
- Low power SRAM design
- FinFET based SRAM
- SRAM for AI accelerators

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