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POWER AWARE FSPA-VLSA ARCHITECTURE WITH ADAPTIVE BODY BIASING FOR ADVANCED DRAM SYSTEMS

V.PAVANI [1], SIMANTINI ROY CHOWDHURY [2], P.ROHIT [3], T.JYOTHI KUMARI [4]

[1]Assistant Professor, Department of Electronics & Communication Engineering, Ballari Institute of Technology and Management, Ballari, Karnataka, India
[2]Assistant Professor, Department of Electronics & Communication Engineering, Ballari Institute of Technology and Management, Ballari, Karnataka, India
[3]Assistant Professor, Department of Electronics & Communication Engineering, Chaitanya College of Engineering, JNTU-GV University, Vishakhapatnam, India
[4]Assistant Professor, Department of Electronics & Communication Engineering, Chaitanya College of Engineering, JNTU-GV University, Vishakhapatnam, India

ABSTRACT

High-density memory architecture is still dominated by DRAM technology, yet power dissipation in sense amplifiers continues to be a significant congestion in sophisticated VLSI systems. Leakage and dynamic switching losses have a major effect on total energy efficiency as scaling moves into deep submicron regimes. An energy-conscious Foot Switch PMOS Access Voltage Latch Sense Amplifier (FSPA-VLSA) designed for open bit-line DRAM architecture is proposed in this study. A PMOS foot-switch mechanism is purposefully incorporated into the suggested architecture to suppress superfluous current paths during read operations. The architecture reduces dynamic and standby power consumption by enhancing the latch stabilization and charge sensing phases. At 45 nm technology, the circuit construction improves voltage sensing accuracy while preserving operational reliability. Cadence Virtuoso design tools were used for both implementation and validation. The suggested method is quite appropriate for next-generation low-power VLSI and ULSI memory systems since simulation findings show an approximate 81% reduction in total power usage. Additionally, threshold voltage is dynamically controlled using an Adaptive Body Biasing (ABB) optimization technique, allowing for further leakage reduction without sacrificing sensing speed.

Keywords: DRAM Technology, Sense amplifier, FSPA-VLSA, Adaptive Body Biasing (ABB) Optimization

I. INTRODUCTION

Dynamic Random-Access Memory (DRAM) is an essential part of contemporary computing systems, allowing for high-speed and high-density data storage in applications ranging from high-performance CPUs to embedded systems. Power consumption has become a major design constraint in VLSI and ULSI circuits as technology continues to scale into deep submicron regimes. The sense amplifier, one of the several DRAM sub-blocks, is essential for deciding overall power efficiency, speed, and reliability because it is in charge of identifying and magnifying minute voltage variations on bit-lines during read operations. However, considerable dynamic switching power and leakage currents plague typical sense amplifier topologies, particularly at 45 nm technology and below. Innovative circuit-level optimization strategies that may concurrently lower power dissipation, preserve sensing precision, and guarantee stable operation under process fluctuations are required to address these issues. Therefore, for next-generation DRAM systems, sophisticated low-power design approaches including adaptive biasing techniques and foot-switch based designs have drawn more attention. A DRAM memory system with several banks arranged into sub-arrays and supported by peripheral circuits such the row decoder, column decoder, row buffer, and I/O buffers for data access control is depicted in Figure 1. It shows how the memory cells are connected via local and master word lines and data lines, and how sense amplifiers placed in between bit lines pick up and magnify tiny voltage variations during read operations. Additionally, it illustrates the fundamental 1T-1C DRAM cell construction, which consists of a single transistor and a single capacitor linked to a bit line and word line for data storage. The architecture shows how charge sharing between the bit line and cell capacitor to start the sensing process is made possible by row activation. Refresh operations are then used to return the boosted signal to the cell in order to preserve data integrity. This hierarchical structure ensures scalability and effective signal routing while increasing memory density. Overall, the structure demonstrates how modern DRAM technology strikes a balance between dependable operation, compact layout design, and fast data access.

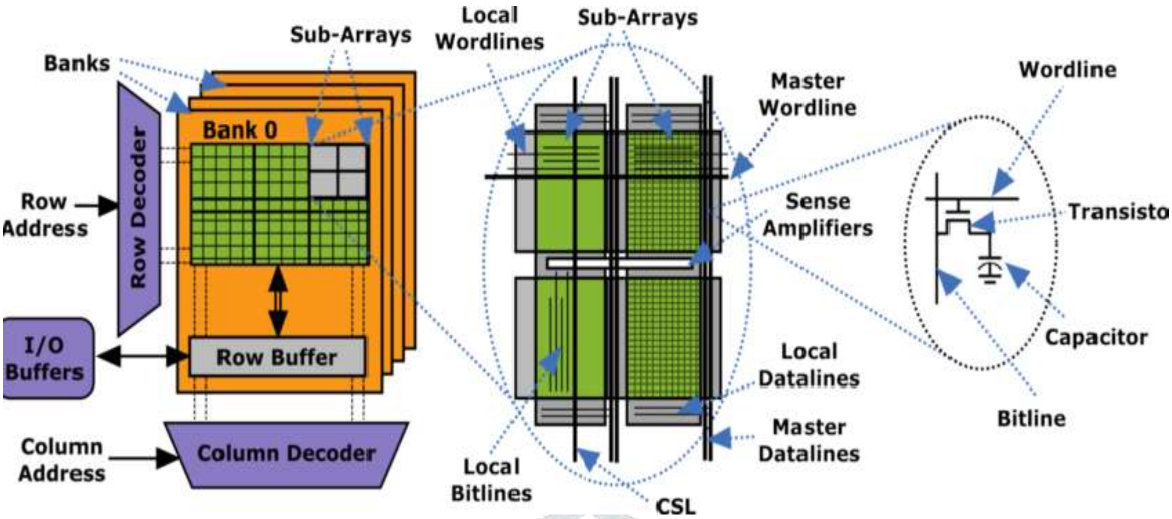

Figure 1: Basic DRAM Organization

II. LITERATURE REVIEW

T. Singh et.al [1], has talked about employing a 45nm technology node to simulate a unique sense amplifier component of the memory. Three different types of sense amplifiers are current mode, voltage mode, and charge transfer type sense amplifier is introduced to address the issues of latency and power consumption.

A.L.Elgreatly et.al [2], has talked about a resonant tunneling diode-based high speed low power reading technique for DRAMs. It is a specifically engineered logic buffer that may be made in silicon nano electronics utilizing a Resonant Tunneling Diode (RTD). Higher read operation speed, complete noise margin, reduced power consumption, and increased chip density are all features of the suggested design.

N.B Singh et.al [3], has talked about the complete bespoke 1KB CMOS PSRAM design. A PSRAM is a one-transistor dynamic RAM with non-multiplexed addresses on the chip in the refresh circuit and an external refresh pin that regulates the cell's refresh to preserve data in the memory.

S. Bae et.al [4], has talked about a New Low Area Overhead Body Bias FPGA Design for Low Power Uses. In 45 nm technology low power architectures, body biasing is a popular and effective method of reducing leakage current. While increasing the granularity to the finest level significantly raises the area overhead over 100%, FPGAs with coarse-grained body bias control only incurred roughly 10% of the overhead.

III. ADAPTIVE BODY BIASING (ABB) OPTIMIZATION

In semiconductor circuits, Adaptive Body Biasing (ABB) is a dynamic approach that modifies the body bias voltage of transistors during operation to maximize power consumption and performance. Variations in manufacturing procedures and operating conditions can cause threshold voltage changes in contemporary CMOS technologies, which impact the circuit's speed and leakage power. By delivering either forward body bias (FBB) or reverse body bias (RBB) to the transistor substrate, ABB corrects for these fluctuations. While reverse body bias raises the threshold voltage to lower leakage current and power consumption, forward body bias lowers the threshold voltage to boost switching speed. DRAM (Dynamic Random Access Memory) technology uses Adaptive Body Biasing (ABB) to boost reliability, decrease leakage power, and improve performance under various operating situations. The threshold voltage of transistors used in memory cells and peripheral circuits in DRAM circuits can be impacted by changes in supply voltage, temperature, and manufacturing technology. To account for these fluctuations, ABB dynamically modifies the body bias voltage of these transistors. The threshold voltage is lowered by using Forward Body Bias (FBB), which speeds up transistor switching and enhances read/write performance. Conversely, Reverse Body Bias (RBB) lowers standby power consumption and leakage current by raising the threshold voltage. Adaptive Body Biasing (ABB) is very helpful in DRAM arrays in sense amplifiers, word line drivers, and peripheral control circuits where power efficiency and timing precision are crucial. Forward body bias can be used to accelerate the sensing and amplification of stored charge in DRAM cells during high-performance tasks like memory access. Reverse body bias is used to reduce leakage current and increase battery life in portable devices during idle or standby modes. DRAM can continue to operate at peak efficiency while consuming less energy thanks to this adaptive regulation.

IV PROPOSED ARCHITECTURE OF DRAM SENSE AMPLIFIER

The DRAM sense amplifier and the FSPA-VLSA (Foot Switch PMOS Access Voltage Latch Type Sense Amplifier) are both used in proposed method. FSPA-VLSA is positioned in the center of the circuit after the DRAM memory array is split into two halves. Fig. 2, which shows two cross-coupled inverters, provides a clear illustration of this. The PM2, PM3, and NM2 all receive the same input, "SENSE." The output of the FSPAVLSA is connected to bit lines BLL (bit line left) and BLR (bit line right). A column of dummy cells is added to each side of the circuits for the express purpose of acting as references. Here, NM5 and NM8, along with their storage capacitances "Cs," are utilized as dummy cells, which are displayed in the circuits' shadowed regions. At the left and right of the FSPA VLSA, which is used to store data in the open bit architecture of the dram sensing amplifier, are two DRAM cells, each made up of one NMOS and one capacitor.

To ensure that the fake cells are charged with the voltage of VDD/2, we first turn on the L and LB lines simultaneously. Then, During the Read cycle one of the word line is enables from L0, L1, R0 and R1. As a result, we elevate the Word line L0, which is present in the BLL and causes the BLL's voltage to change. Raising L to choose the other dummy cell in the other memory halves concurrently generates the appropriate voltage. The latch toggles when the BLR voltages fall between "0" and "1," assuming that the BLL and BLR are perfectly matched.

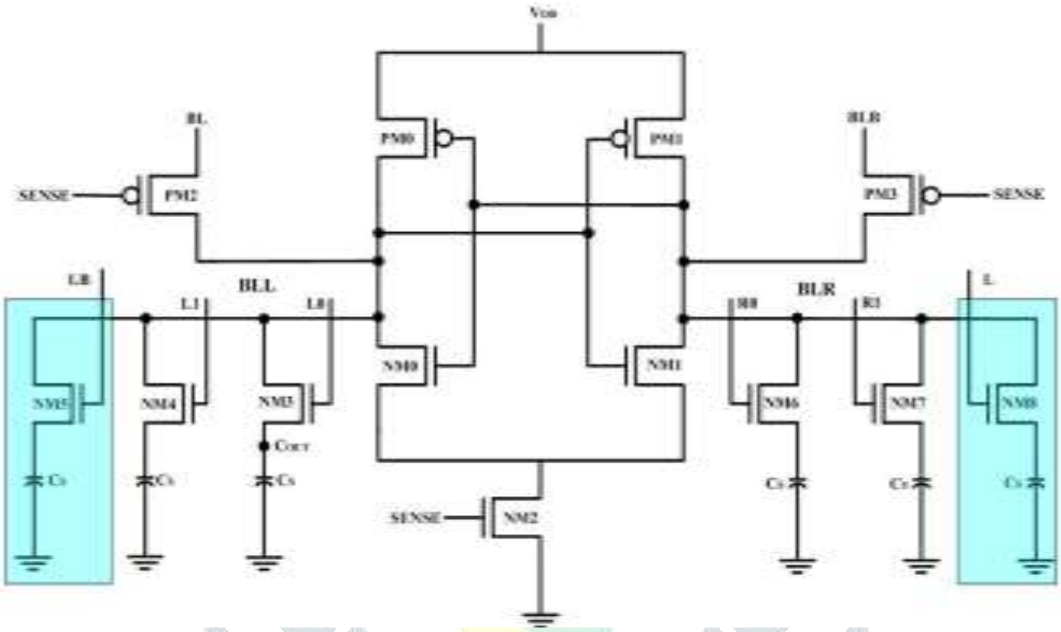

Figure 2: Proposed technique for Open bit architecture of DRAM Sense Amplifier

Advantages of Proposed DRAM Sense Amplifier

- **Power Savings:** The overall power consumption reduction is one of the major benefits of designing DRAM sensing amplifiers utilizing 45nm technology. Significant power savings are achieved by using a Foot Switch PMOS Access Voltage Latch Type Sense Amplifier (FSPA-VLSA) in the open bit architecture of DRAM cells during read operations. This method makes it possible to use power more effectively, which is essential for the creation of memory systems that consume less energy.
- **Advanced CMOS Technology:** The sense amplifier design can incorporate more intricate and effective circuits thanks to the utilization of 45nm technology. Advanced features like latch type sense amplifiers, which have been demonstrated to lower sensing delay and enhance DRAM system performance overall, can be implemented thanks to this technology.
- **Improved Performance:** Performance metrics are enhanced when 45nm technology is used into DRAM sense amplifiers. Reduced sensing latency is essential for the quick data access needed by contemporary computing systems. These parameters can be optimized thanks to the use of sophisticated CMOS technology in sense amplifier design, which guarantees that the DRAM system runs at high speeds while consuming little power.
- **Reduced Soft Error Rate (SER):** Additionally, the 45nm technology used in the construction of DRAM sensing amplifiers helps to lower the soft error rate (SER). The SER of DRAMs can be greatly decreased by using sophisticated structures and ideas, such as novel dummy cell approaches. This is essential to guaranteeing the dependability and accuracy of data kept in DRAM systems.

Applications of DRAM Sense Amplifier

- **High-Performance Computing (HPC):** High-speed computer systems can benefit from DRAM sensing amplifiers made with 45nm technology because of their enhanced performance and lower power consumption.
- **Embedded Systems:** The design of DRAM sensing amplifiers employing 45nm technology can greatly lower the overall power consumption in embedded systems, where memory efficiency and power savings are crucial. Energy efficiency is a major challenge for battery-powered devices and systems, therefore this is essential.
- **Mobile Devices:** DRAM sensing amplifiers employing 45nm technology are perfect for mobile devices because of their small size and high efficiency. The sensing amplifiers' lower power consumption can assist prolong battery life and enhance the device's overall performance because these devices frequently run on limited power.
- **Data Centers:** The efficiency and performance gains provided by the design of DRAM sense amplifiers utilizing 45nm technology can drastically lower operating costs in data centers, where massive volumes of data are processed and stored.

V RESULTS AND DISCUSSION

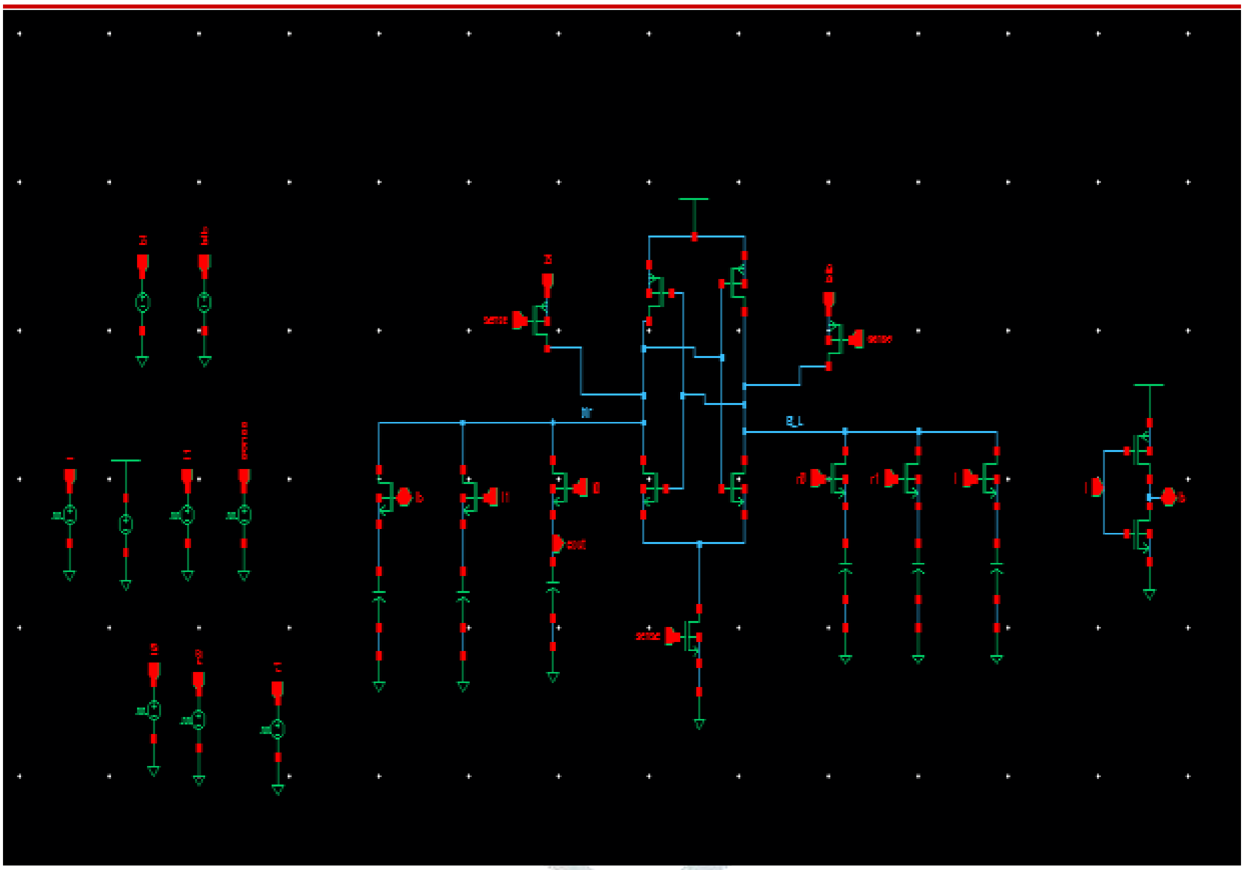

Figure 3: Schematic of Proposed DRAM Sense Amplifier

Proposed DRAM sense amplifier, which is intended to identify and magnify minute voltage variations from the memory bit lines, is schematically shown in Figure 3. Cross-coupled transistors make up the circuit, which quickly amplifies the received signal by creating a positive feedback structure. In order to stabilize the sensing operation and increase speed, more biasing and control transistors are needed. The read performance and dependability of DRAM memory operations are improved by this approach.

The transient analysis waveform of the proposed DRAM sensing amplifier is displayed in Figure 4 during a period of 0–10 ns. The control signal (pwr) switches to initiate the sensing process, while the input signal (I/0) displays a triangle waveform. The sensed bit-line signals determine how the output voltage (cout) changes. The amplifier's differential sensing behavior during memory read operation is shown by the bit-line voltages (bl and blr).

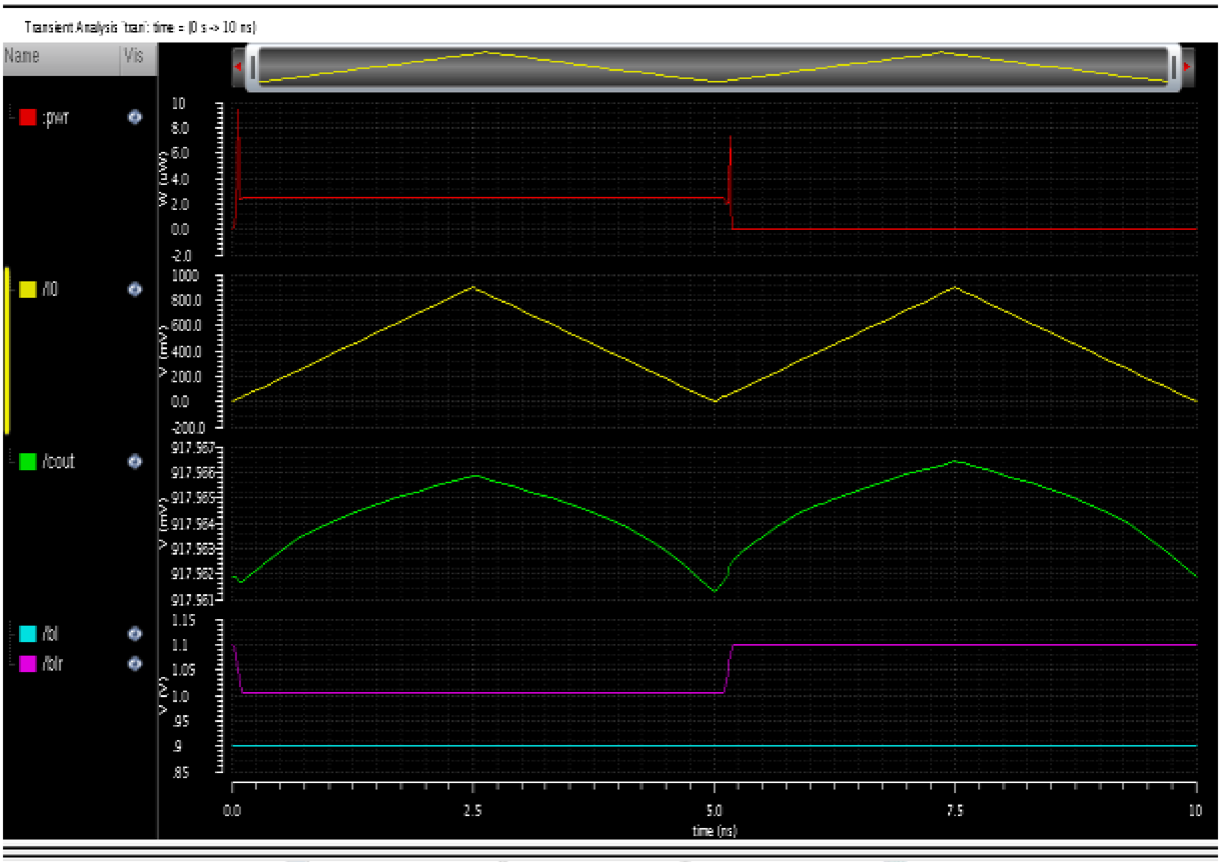

Figure 4: Waveforms of Proposed DRAM Sense Amplifier

VI RESULT ANALYSIS

Method	AREA(Transistors count)	Power (w)
DRAM voltage latch sense amplifier	17	6.195 uw
Foot Switch PMOS Access Voltage Latch Sense Amplifier	15	1.328 uw

Table 1: Comparison of Transistor Count and Power Consumption of the Proposed DRAM Sense Amplifier

Based on the number of transistors utilized in the design, the table.1 compares the DRAM sensing amplifier's area and power. The first setup requires 6.195 µW of power and 17 transistors. The circuit area and power consumption are decreased by the optimized design's 15 transistors. At 1.328 µW, it exhibits far lower power dissipation. According to this comparison, proposed design increases efficiency by reducing the number of transistors. As a result, the DRAM sensing amplifier achieves lower power consumption and improved area utilization.

VII CONCLUSION

The proposed work assesses the power consumption of DRAM sensing amplifiers using the open bit architecture technique during read operations. It shows that the open bit architecture of DRAM sense amplifier utilizing a simple latch type sense amplifier consumes about 81% more power than the suggested method of DRAM sense amplifier using FSPA-VLSA. The application of the same pulse to every circuit input is responsible for this decrease. For half of the simulation period, the PMOS transistor is active and the NMOS transistor is dormant. After that, the NMOS transistor is active and the PMOS transistor is inactive for the remaining simulation time. Because of the NMOS or PMOS, the circuit spends the majority of its time in a cut-off state, which lowers overall power consumption.

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