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Design and Implementation of an Ultra-Low-Power RISC-V CPU Using RRAM-CMOS Hybrid Standard Cells with PMOS Power Gating

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ABSTRACT :

The increasing demand for energy-efficient and high-performance digital systems has driven the exploration of alternatives beyond conventional CMOS scaling. Resistive Random Access Memory (RRAM) has emerged as a promising technology due to its non-volatile nature, fast switching capability, and potential for compact integration. However, effectively utilizing RRAM in practical digital circuit design remains a challenge. In this work, a low-power design approach using RRAM-CMOS hybrid standard cells combined with PMOS power-gating technique is presented for RISC-V based processor applications. The integration of RRAM with CMOS logic helps in reducing transistor count and static power consumption while maintaining reliable operation. In addition, PMOS power gating minimizes leakage current during idle conditions, further improving energy efficiency. The proposed NAND gate and half-adder designs are implemented and verified through simulation. The results demonstrate correct functionality along with reduced delay and power consumption compared to conventional CMOS designs. These improvements indicate that the proposed approach can be effectively used as building blocks for future low-power processor architectures.

Keywords : RRAM-CMOS hybrid logic, Resistive random access memory (RRAM), PMOS power gating, Half-adder, NAND-based logic, Energy-efficient circuits, RISC-V applications

I. INTRODUCTION :

The demand for energy-efficient and high-performance processors has increased significantly due to the rapid growth of portable devices, IoT systems, and battery-operated applications. Conventional CMOS-based designs, although widely used, face limitations such as higher leakage power, increased area, and reduced efficiency when scaled for ultra-low-power applications.

To address these challenges, emerging memory technologies like Resistive Random-Access Memory (RRAM) have gained attention. RRAM is a non-volatile memory that can retain data without power and offers advantages such as fast switching speed and low leakage current. By combining RRAM with CMOS technology, it is possible to design hybrid circuits that are more compact and energy-efficient compared to traditional designs.

In this work, a RISC-V CPU is designed using RRAM-CMOS hybrid standard cells along with PMOS-based power gating techniques. The use of RRAM helps in reducing transistor count and enables logic-in-memory capability, while power gating further minimizes leakage during inactive states. This combined approach improves overall energy efficiency without affecting performance.

Basic digital building blocks such as logic gates and arithmetic units form the foundation of the proposed design. The efficiency of these components directly impacts the overall performance of the CPU. RISC-V, being an open-source and flexible instruction set architecture, is used in this work due to its simplicity and adaptability for low-power designs.

Overall, this study highlights the potential of integrating RRAM with CMOS logic and power gating techniques for developing next-generation low-power processor architectures.

II. LITERATURE REVIEW:

Recent advancements in beyond-CMOS technologies have led to significant interest in emerging memory devices such as Resistive Random Access Memory (RRAM) and memristors for energy-efficient computing applications. These technologies enable novel computing paradigms such as logic-in-memory and neuromorphic systems, addressing the limitations of conventional CMOS-based architectures.

[1]M. Fritscher et al., (2024) present an area-efficient digital design approach using RRAM-CMOS hybrid standard cells. The proposed methodology integrates RRAM devices within standard cell structures to reduce transistor count and silicon area. By leveraging the non-volatile nature of RRAM, the design achieves improved energy efficiency while maintaining functional correctness. The work demonstrates that hybrid RRAM-CMOS logic can be effectively used for compact and low-power digital system design.

[2]L. Brackmann et al., (2024) experimentally verify non-stateful logic gates implemented using resistive RAM (RRAM). The study evaluates key parameters such as speed, power consumption, and reliability. Unlike conventional logic gates, these RRAM-based implementations do not require intermediate storage, resulting in reduced energy consumption. The results validate the feasibility of logic-in-memory concepts for ultra-low-power applications. [3]A. Bende et al., (2024**)** present an experimental validation of memristor-aided logic using a 1T1R TaOx RRAM crossbar array. The proposed design enables computation directly within memory arrays, thereby reducing data transfer overhead. The work highlights the efficiency of memory-centric computing and demonstrates improved performance in terms of energy and area when compared to traditional architectures.

[4]M. Ulbricht et al., (2023) introduce the TETRISC System-on-Chip (SoC), a resilient quad-core processor based on the ResiliCell approach. The design emphasizes fault tolerance and reliability, which are critical for modern computing systems. The study demonstrates how emerging technologies can be integrated into processor architectures while maintaining robustness and performance. [5]V. Milo et al., (2019) investigate multilevel HfO_2-based RRAM devices for low-power neuromorphic applications. The study shows that RRAM devices can store multiple resistance states, enabling efficient data representation and reduced power consumption. This work highlights the potential of RRAM in advanced computing paradigms such as artificial intelligence and neuromorphic systems.

[6]S. Kvatinsky et al., (2014) propose the MAGIC (Memristor-Aided Logic) approach, which enables logic operations directly within memory devices. This reduces the need for frequent data transfer between memory and processing units, thereby improving energy efficiency. The work highlights the potential of memristor-based logic for low-power digital systems.[7]D. Bhattacharjee et al., (2018) present a technology-aware logic synthesis approach for ReRAM-based in-memory computing. The proposed method optimizes logic mapping based on device characteristics, resulting in improved performance and reduced power consumption.

[8]X.-Y. Wang et al., (2021) introduce a memristor-CMOS ternary logic family that supports multi-valued logic operations. The design achieves higher integration density and reduced area compared to conventional binary logic implementations.[9]H. Li, Q. Xia, and J. J. Yang, (2020) explore memristive crossbar array architectures for brain-inspired computing. Their work demonstrates high parallelism and energy efficiency, making such architectures suitable for next-generation computing systems.[10]S. Yu, (2020) provides a detailed overview of emerging non-volatile memory technologies for neuromorphic and energy-efficient computing. The study emphasizes the scalability and low-power advantages of RRAM-based systems.[11] J. Rajendran, H. Zhang, and Y. Liu, (2020) analyze key challenges in memristor-based computing systems, including device variability, reliability, and security concerns. The study highlights the importance of robust design methodologies for practical implementation.[12]P. Yao et al., (2020) demonstrate a hardware implementation of a memristor-based convolutional neural network. The results show improved computational efficiency and reduced energy consumption, indicating the potential of memristor technology in advanced computing applications.

III. PROPOSED METHOD :

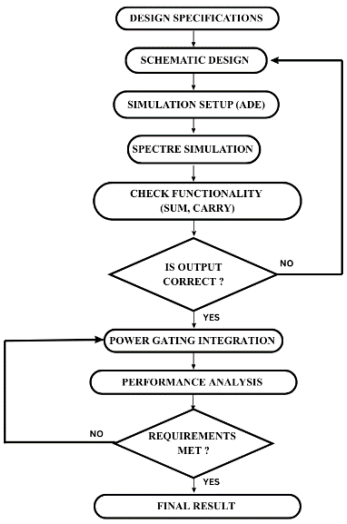

Figure 1 : The design flow of the proposed Method

The design of low-power digital circuits has become increasingly important with the demand for energy-efficient computing systems. To address this, a hybrid approach using RRAM-CMOS logic combined with power-gating techniques is considered. The overall design flow followed in this work is illustrated in Figure 1.

The design process begins with the schematic development of basic logic gates using RRAM-CMOS hybrid structures. NAND gates are implemented by integrating RRAM devices with CMOS inverters, which helps in reducing transistor count and improving compactness. These gates are then used to construct a half-adder circuit for performing basic arithmetic operations.

The circuit is simulated using Analog Design Environment (ADE) and Spectre simulator to verify its functionality. The outputs (Sum and Carry) are analyzed to ensure correct logical operation. If the output does not meet the expected behavior, the design is modified and re-evaluated, as shown in the design flow.

To further enhance energy efficiency, PMOS-based power gating is incorporated, as illustrated in Figure 2. In this technique, a PMOS transistor is placed between the supply voltage and the logic block to control power delivery. During idle conditions, the supply is disconnected, reducing leakage power, while during active operation, normal functionality is maintained.

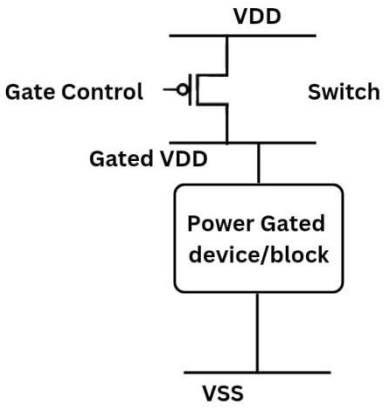

Figure 2 : The design flow of the proposed Method

After integrating power gating, the circuit is analyzed in terms of performance parameters such as delay and power consumption. If the required performance is not achieved, the design is refined either at the schematic level or during power-gating integration. Once the desired performance is obtained, the final design is achieved.

Overall, this approach provides a structured VLSI design methodology for developing low-power and area-efficient digital circuits using RRAM-CMOS hybrid logic.

IV. RESULTS AND DISCUSSION :

The performance of the proposed RRAM-CMOS based design is analyzed through schematic implementation and simulation results. The half-adder circuit designed using NAND gates is shown in **Figure 3**, where RRAM-CMOS hybrid logic is used to achieve compact and efficient circuit realization.

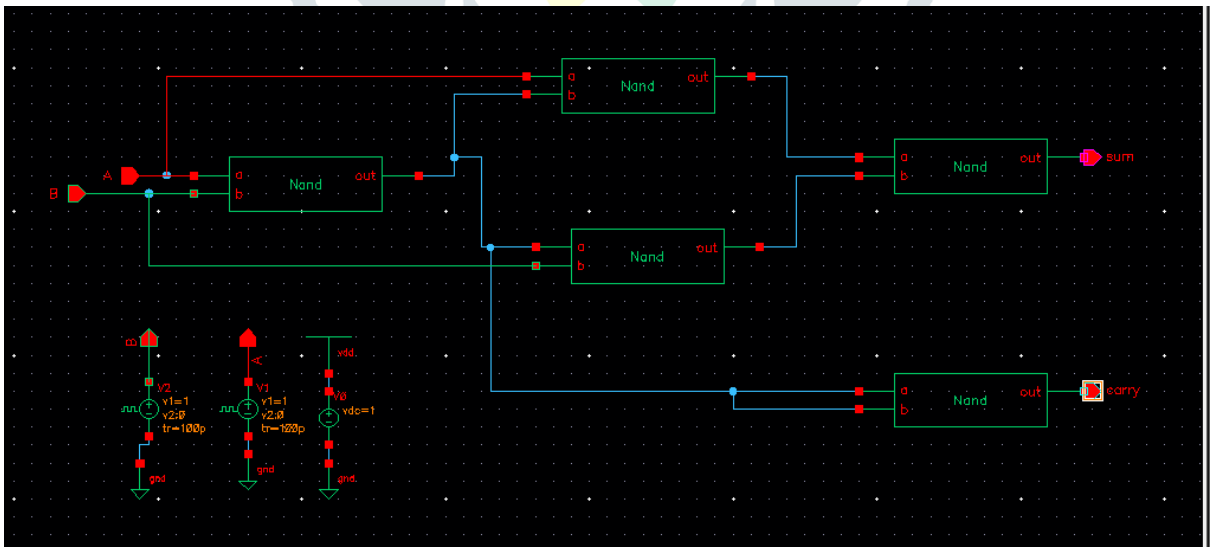

Figure 3 : Half adder schematic designed using NAND gates based on RRAM-CMOS hybrid logic

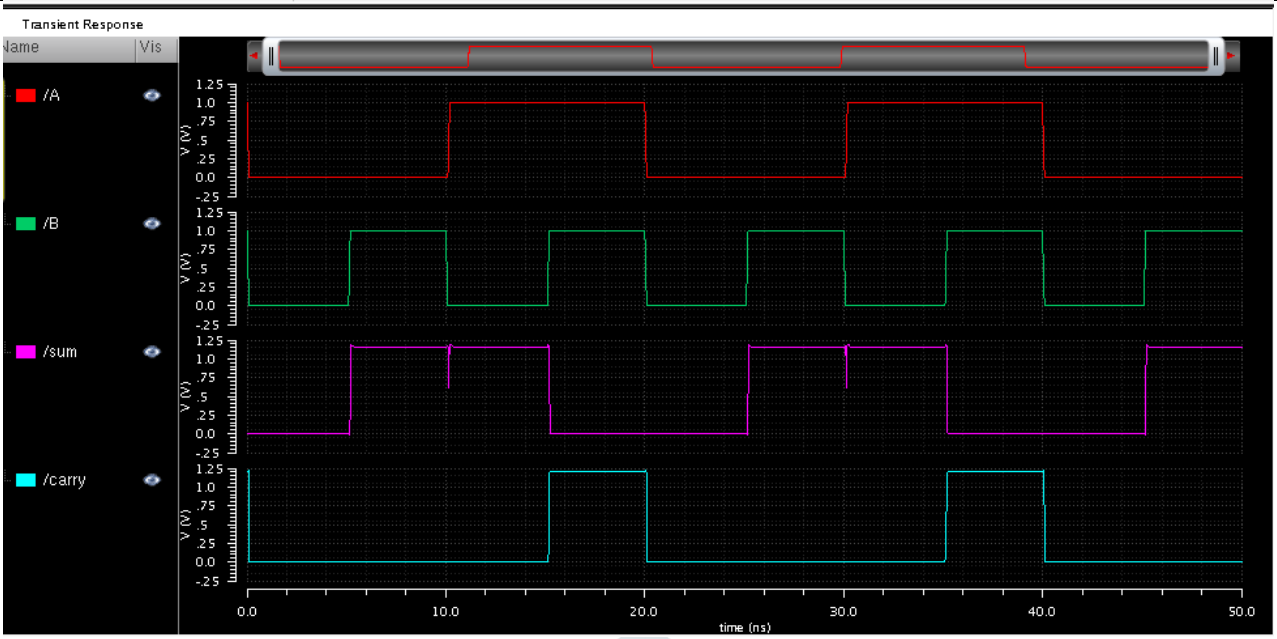

Figure 4 : Simulation waveform of proposed RRAM-CMOS based Half Adder showing input signals (A, B) and outputs (Sum, Carry)

The functional verification of the proposed design is carried out using transient analysis. The simulation waveforms shown in Figure 4., illustrates the input signals (A, B) along with the corresponding outputs (Sum and Carry). It can be observed that the Sum output follows the XOR operation, while the Carry output follows the AND operation. The waveform confirms correct logical functionality and stable switching behavior of the half-adder circuit.

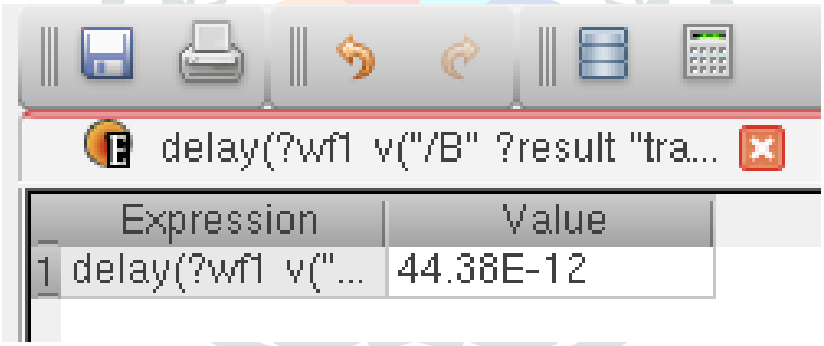

Figure 5 : Measured propagation delay of the proposed RRAM-CMOS based half adder

Further performance evaluation is carried out in terms of propagation delay and power consumption. The measured propagation delay of the circuit is presented in Figure 5, which is found to be **44.38 picoseconds**, indicating fast switching performance of the proposed design.

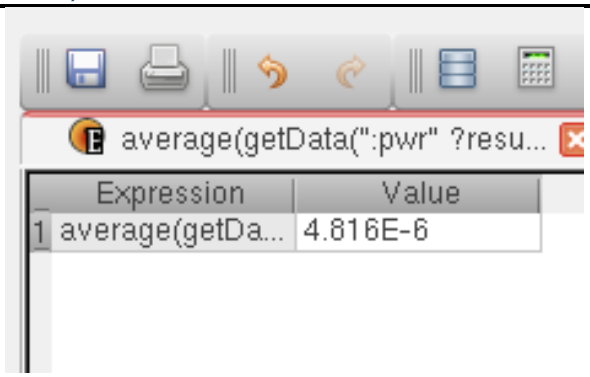

Figure 6 : Average power consumption of the proposed RRAM-CMOS based half adder

The average power consumption of the circuit is shown in **Figure 6**, with a value of **4.186 µW**. The reduction in power consumption is mainly due to the use of RRAM-based logic combined with PMOS power-gating techniques, which effectively reduce leakage power during idle conditions.

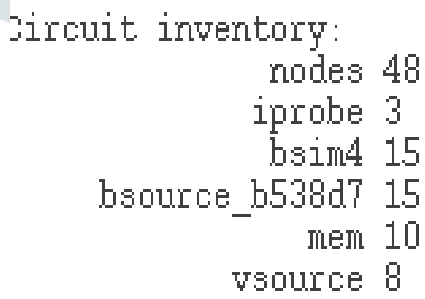

Figure 7 : Device count summary of the proposed circuit

In addition to power and delay analysis, the device count of the proposed circuit is shown in **Fig. 7**. The circuit inventory indicates a reduced number of components, including nodes, resistive elements, and voltage sources. This reduction is achieved due to the use of RRAM-CMOS hybrid logic, which minimizes transistor usage compared to conventional CMOS designs. The lower device count contributes to improved area efficiency and compact circuit implementation.

V. CONCLUSION :

In this work, a low-power design approach using RRAM-CMOS hybrid logic along with PMOS power-gating technique has been presented. The integration of RRAM with CMOS helps in reducing the number of transistors and provides non-volatile behavior, which is useful for minimizing standby power. In addition, the use of PMOS power gating effectively reduces leakage power by disconnecting inactive parts of the circuit during idle conditions.

The proposed half-adder design was successfully implemented and verified through simulation. The results show correct logical operation along with improved performance in terms of delay and power consumption. The measured delay is in the picosecond range, indicating fast switching capability, while the reduced power consumption highlights the efficiency of the proposed approach. The lower device count further contributes to compact circuit design and better area utilization.

Overall, the combination of RRAM-based logic and power-gating technique offers a practical and energy-efficient solution for modern digital circuit design. This approach can be extended to more complex systems such as low-power applications, making it suitable for future energy-constrained computing environments.

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