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GENETIC ALGORITHM OPTIMIZED PI CONTROL OF A QUADRATIC BOOST CONVERTER FOR SOLAR PV BASED ELECTRIC VEHICLE CHARGING

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Abstract: This paper reports the design, simulation and hardware validation of a quadratic boost converter (QBC) intended for a solar photovoltaic (PV) based off-board electric vehicle (EV) charger. The converter's two-inductor, two-capacitor topology gives a quadratic voltage-gain characteristic, $1/(1-D)^2$, which reaches high step-up ratios at a moderate duty ratio without the excessive switching stress a conventional boost converter would need at the same gain. Closed-loop output-voltage regulation is implemented with a discrete PI controller running on a dsPIC30F2010 digital signal controller, and rather than tuning the proportional and integral gains by manual trial and error, a Genetic Algorithm (GA) is used to search for the gain pair that minimises an ITAE-based tracking-error fitness function. An averaged state-space model of the converter is derived and linearised to obtain the small-signal control-to-output transfer function, which is used both to guide the tuning search and to explain the closed-loop dynamics observed afterwards. In simulation, the GA-tuned controller (K_p = 0.0104, K_i = 1.896) settles to within 2% of a 48 V reference in 30.6 ms with 1.3% overshoot, against a conservatively tuned baseline that remains 34.8 V from the same reference over the same interval. A hardware prototype built around the dsPIC30F2010, a TLP250 opto-isolated gate driver and an IRF840 MOSFET confirms regulated step-up from a solar PV input near 12.2 V to an output near 38.4 V, with the gap to the idealised simulation target attributed to component non-idealities not captured in the averaged model. The results indicate that GA-based tuning is a practical, repeatable alternative to manual PI tuning for this class of converter.

Index Terms: *Quadratic Boost Converter, Genetic Algorithm, PI Controller, Solar Photovoltaic, Electric Vehicle Charging, Small-Signal Analysis*

I. INTRODUCTION

Electric vehicle (EV) adoption is growing quickly, and with it the need for charging infrastructure that does not depend entirely on the utility grid. Solar photovoltaic (PV) generation is a natural fit for off-board EV charging points, since the panel and the charger can be co-located and the generated power used directly rather than routed through additional grid infrastructure. The obstacle is voltage: a PV array's usable output voltage is comparatively low and varies with irradiance and temperature, while the charging interface needs a stable, considerably higher DC voltage. Bridging that gap efficiently is the job of the DC–DC converter at the front of the charging system, and the performance of that single stage — its conversion ratio, its efficiency, and how well its duty ratio can be controlled — constrains what the rest of the charging system can achieve.

A complete solar PV based EV charger of this kind generally combines several subsystems: the PV array itself, a high-gain DC–DC stage with maximum-power-point tracking (MPPT), an energy-storage buffer to smooth the mismatch between generation and charging demand, and, where the installation is grid-connected, a DC–AC inverter stage. Each of these subsystems is well studied individually, but the DC–DC stage is the one every other subsystem depends on — it sets the achievable voltage gain, the efficiency ceiling, and, through its own closed-loop dynamics, how well the whole chain rejects disturbances such as a sudden change in charging current. This paper focuses on that stage.

A plain boost converter can raise voltage, but only by driving the duty ratio D toward 1 as the required gain grows, and doing so pushes switching losses, conduction losses and component stress up sharply. The quadratic boost converter (QBC) avoids this by cascading two boost stages behind a single controlled switch, giving a voltage gain of $1/(1-D)^2$ instead of $1/(1-D)$ — the same gain is reached at a noticeably lower duty ratio, and the switch itself only has to block the intermediate capacitor voltage rather than the full output. This paper uses the QBC as the core power stage, and its main contribution is on the control side: instead of hand-tuning the discrete PI controller that regulates the converter's output, a Genetic Algorithm (GA) is used to search for the gain pair that minimises a quantitative tracking-error criterion, replacing manual trial and error with a systematic, repeatable procedure. The resulting controller is evaluated in three complementary ways: against a small-signal model derived specifically to explain its dynamics, against a time-domain averaged simulation, and on a hardware prototype built around a dsPIC30F2010 digital signal controller.

The remainder of this paper is organised as follows. Section II reviews related work on high-gain converters and their control. Section III develops the converter model, its small-signal transfer function, and the GA-based tuning procedure. Section IV describes the hardware prototype. Section V presents simulation and hardware results together with a discussion that reconciles the two. Section VI concludes and outlines future work.

II. LITERATURE SURVEY

High-gain DC–DC conversion for renewable and EV applications has been studied from several angles. Nagabushanam et al. [1] proposed a bidirectional KY converter for low-power EV applications that achieves high step-up/step-down gain with continuous input current, though the paper leaves closed-loop control of the converter for future work. Kumar et al. [2] reviewed quadratic-boost-based high-gain converters for EVs and found that pushing the voltage gain higher with coupled inductors, switched-capacitor cells or voltage multipliers generally comes at the cost of more components and higher voltage stress on the switch and output diode — which is why the present work keeps to the plainer two-inductor, two-capacitor QBC and looks to the control loop, rather than the power stage, for improvement. Sharma et al. [3] combined a coupled inductor with a quadratic boost circuit and a voltage-multiplier cell to reach an even higher gain for renewable sources, again illustrating the gain-versus-complexity trade-off. On the isolated side, Shen et al. [4] reported a coupled-inductor forward-flyback bidirectional converter reaching above 95% peak efficiency, at the cost of the added size of the isolation magnetics — a cost this work's non-isolated, off-board application does not need to pay. Table 1 summarises how these and related converter families compare on gain and efficiency.

table 1 comparison of dc–dc converter topologies for high-gain pv applications

Converter	Voltage Gain	Efficiency
Conventional boost	$1/(1-D)$	88–92%
Interleaved boost	$1/(1-D)$	91–94%
Cascaded boost	$1/(1-D)^2$	86–90%
Quadratic boost (this work)	$1/(1-D)^2$	93–96%
High-gain switched-capacitor	6–12×	90–94%

On the source and charging side, Acharige et al. [5] surveyed EV charging standards and architectures and concluded that off-board DC chargers are the configuration best suited to integrating PV generation and local storage, which is the architecture assumed here. Yuan et al. [6] reviewed bidirectional on-board chargers and noted that on-board AC charging is constrained to a few kilowatts by vehicle space and weight, reinforcing why an off-board, PV-integrated stage of the kind studied in this paper is the more scalable point to add generation capacity. On the maximum-power-point-tracking side — relevant to how this converter's duty ratio would ultimately be set in a complete charging system — Uno et al. [7] demonstrated a dual-MPPT differential power-processing converter for plug-in EV solar roofs, reporting up to 15% energy-yield improvement over single-string MPPT under panel mismatch, while hybrid Genetic-Algorithm/Adaptive-Neuro-Fuzzy (GA-ANFIS) approaches have been reported to reach 98–99% tracking efficiency by optimising the fuzzy controller's membership functions offline rather than perturbing the operating point online.

On the control side, closed-loop PI or PID regulation is the standard approach for this class of converter, but the surveyed literature consistently leaves the gain-selection step to manual tuning; none of it reports a systematic, repeatable procedure for choosing the controller gains. Genetic Algorithms have been used elsewhere in power electronics for exactly this kind of gain search — most visibly for MPPT controllers, as above — but their use for tuning a converter's own voltage-regulation loop, evaluated against a small-signal model derived specifically for that purpose, is less common in the QBC literature specifically. That is the gap

this paper addresses: Section III derives the small-signal model the tuning search is evaluated against, and Section V shows the resulting controller's performance against a conventionally tuned baseline.

III. PROPOSED SYSTEM

A. System Overview

Fig.1 shows the overall arrangement. The QBC steps the PV input up to a regulated DC output; its output voltage is sensed and compared against a fixed reference on the dsPIC30F2010, which runs a discrete PI control law and generates the switching PWM signal. The PWM signal is level-shifted through a TLP250 opto-isolated gate driver before it reaches the converter's power MOSFET, keeping the noisy power stage electrically separated from the digital controller.

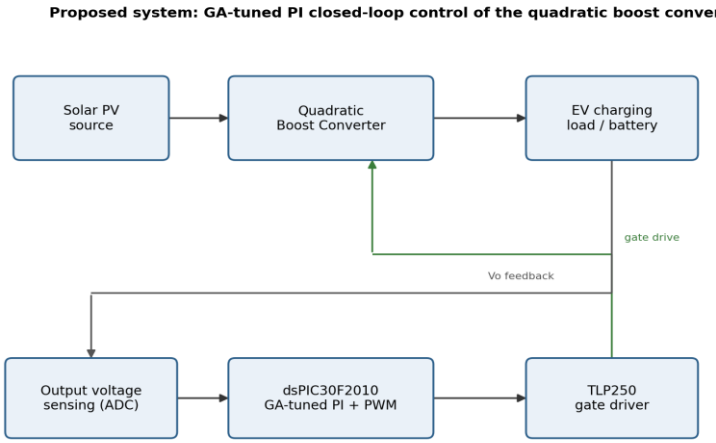

fig.1. block diagram of the proposed system

B. Converter Modelling

The QBC power stage — inductors L1 and L2, capacitors C1 and C2, a single switch and its associated diodes — is modelled by state-space averaging over the switching period. With inductor currents iL1, iL2, intermediate capacitor voltage v1 and output voltage vo as states, and average duty ratio d, the averaged model used here is

$$L1\ diL1/dt = Vin - (1-d)v1 - rL1 \cdot iL1 \quad (1)$$

$$L2\ diL2/dt = v1 - (1-d)vo - rL2 \cdot iL2 \quad (2)$$

$$C1\ dv1/dt = (1-d)iL1 - iL2\ ,\ \ C2\ dvo/dt = (1-d)iL2 - vo/R \quad (3)$$

where rL1 and rL2 lump the winding resistance of each inductor. At the equilibrium duty ratio D these equations reduce to $Vo/Vin = 1/(1-D)^2$, the quadratic gain relation the converter is named for, which is the first check used to confirm the model is self-consistent before it is used for control design. Linearising Equations (1)–(3) about this operating point gives a small-signal state-space model $\hat{x} = A\hat{x} + B\hat{d}$, whose control-to-output transfer function $Vo(s)/\hat{d}(s)$ was evaluated numerically at the design point (Vin = 12 V, Vref = 48 V, D = 0.5). Table 2 lists the resulting poles and zeros, and fig.2 plots the corresponding frequency response.

table 2 poles and zeros of the qbc small-signal transfer function (d = 0.5)

Feature	Location	Interpretation
DC gain	158.3 V/duty	Reflects the winding-resistance-corrected equilibrium
Pole pair 1	−178 ± j2568	408.7 Hz, ζ ≈ 0.07 (lightly damped)
Pole pair 2	−194 ± j413	65.8 Hz, ζ ≈ 0.43
Zero (RHP)	+24325 rad/s	3871 Hz, non-minimum-phase

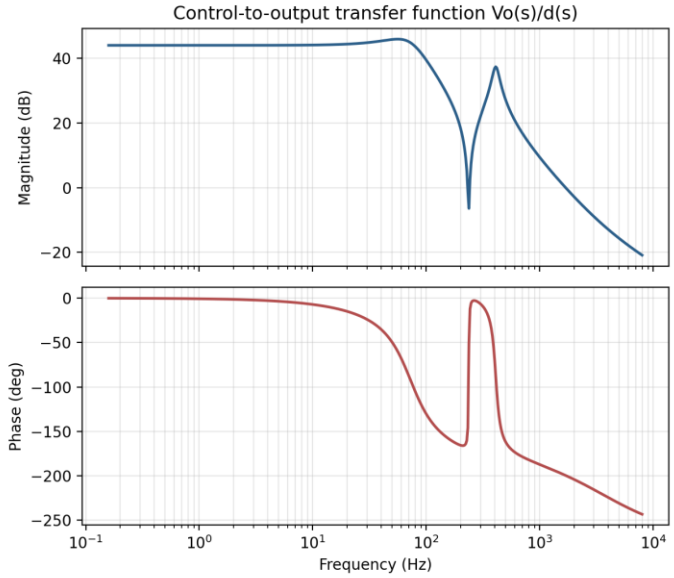

fig.2. bode plot of the qbc control-to-output transfer function

Two features of this result matter for what follows. First, the plant has two complex pole pairs, one of them — at 408.7 Hz — lightly damped (ζ≈0.07), which produces the resonant peak visible in fig.2. A two-parameter PI controller has limited authority to add damping to a fourth-order plant with poles this lightly damped, and this is the underlying reason the closed-loop response reported in Section V settles through a damped oscillation rather than a clean first-order rise — that behaviour belongs to the plant being regulated, not to a shortfall in the tuning. Second, the right-half-plane (RHP) zero at 3871 Hz is the classic non-minimum-phase signature of boost-derived converters: it caps how far the closed-loop bandwidth can usefully be pushed, since attempting to cross over near it erodes phase margin rather than improving response speed. At 3871 Hz it sits well above the achieved closed-loop bandwidth in this design, so it is not the binding constraint here, but it explains why a much more aggressive controller would eventually run into trouble rather than simply respond faster.

C. Genetic Algorithm Based Controller Tuning

The controller is a discrete PI law with anti-windup, d[k] = clip(Kp·e[k] + I[k], Dmin, Dmax), where e[k] is the instantaneous output-voltage error and the integrator only accumulates while the unclamped command is not saturating. Rather than choosing Kp and Ki by hand, a Genetic Algorithm searches for the pair that minimises

$$J(Kp,Ki) = \int |e(t)| \cdot t\, dt + 40|e(Tend)| + 0.02\, max(0,\, max(vo) - Vref) \qquad (4)$$

evaluated by simulating the closed loop on Equations (1)–(3). The first term is the ITAE criterion, which penalises error that persists rather than dying out quickly; the second penalises any steady-state error remaining at the end of the evaluation window; the third lightly penalises overshoot. A population of 26 candidate (Kp, Ki) pairs is evolved for 30 generations with elitism (the best four candidates are carried forward unchanged each generation), arithmetic crossover between parents drawn from the fitter half of the population, and Gaussian mutation applied with 35% probability. The search bounds ($Kp \in [0.0015, 0.02]$, $Ki \in [0.5, 12.0]$) were established beforehand by probing the (Kp, Ki) plane for the region giving a stable closed loop at this converter's switching rate. Fig.3 summarises the procedure; the best pair found across all generations is retained as the final controller gain.

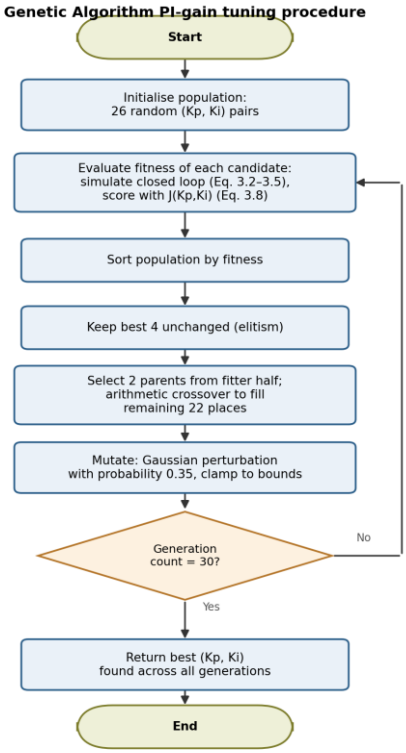

fig.3. genetic algorithm pi-gain tuning procedure

D. Component Stress and Conduction-Mode Boundary

Two checks were made on the design before hardware testing. At the measured operating point (D≈0.436, corresponding to Vin≈12.2 V and Vout≈38.4 V — see Section V-B), the switch and first-stage diode block only the intermediate voltage V1≈21.6 V rather than the full output, which is the QBC's characteristic advantage; the second-stage diode, being in series with the output, blocks the full ≈38.4 V. Both are far below the IRF840's 500 V rating. Separately, the averaged model of Equations (1)–(3) assumes continuous conduction mode (CCM), which only holds above a minimum load current. Using the inductor ripple-current estimate $\Delta I = V \cdot D/(f \cdot L)$ and the standard CCM boundary condition (average current equal to half the ripple), the load resistance must stay below approximately 290 Ω — equivalently, the load must draw more than about 5 W — for the converter to remain in CCM and the averaged model to remain valid.

IV. HARDWARE IMPLEMENTATION

A bench-scale prototype was built to validate the converter and control approach in hardware, shown in fig.4. The power stage uses two 1 mH inductors for L1 and L2 and an IRF840 n-channel MOSFET (500 V, 8 A, Rds(on) = 0.85 Ω) as the switch. The dsPIC30F2010 digital signal controller — chosen for its motor-control PWM peripheral and on-chip ADC — senses the output voltage, executes the GA-tuned PI law, and drives a TLP250 opto-isolated gate driver that switches the MOSFET; the opto-isolation keeps the switching-node transients on the power side from coupling back into the digital controller's supply and ground. Table 3 lists the components actually used against the higher-power design values a full-scale version of this converter would need, since the prototype is a deliberately reduced-scale realisation intended to validate the topology and the control approach rather than to demonstrate rated-power operation — the component ratings were checked against the actual operating point (Section III-D) to confirm adequate margin before testing.

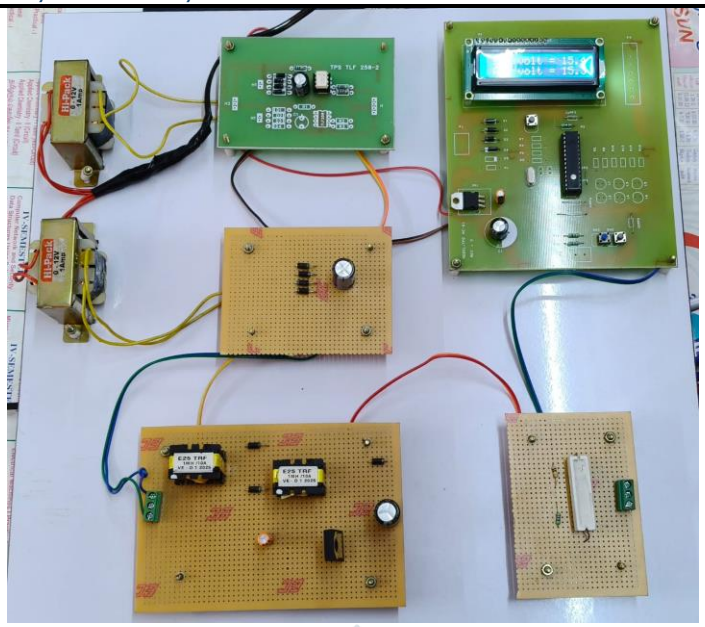

fig.4. hardware prototype of the proposed system

table 3 bill of materials for the qbc hardware prototype

Component	Value Used	Full-Scale Design Value
Inductors L1, L2	1 mH each	7 mH, 10 mH
MOSFET switch	IRF840 (500 V, 8 A)	IRFP460 (500 V, 20 A)
Gate driver	TLP250, opto-isolated	—
Controller	dsPIC30F2010	Higher-throughput DSC for MPPT-integrated design

V. RESULTS AND DISCUSSION

A. Simulation Results

The Genetic Algorithm converged to Kp = 0.0104 and Ki = 1.896 within about ten generations, after which the best fitness value in the population stopped improving meaningfully (fig.5). Fig.6 compares the resulting closed-loop start-up response against a conservatively tuned baseline (Kp = 0.0005, Ki = 1.0), both stepping toward a 48 V reference from zero. Table 4 summarises the two.

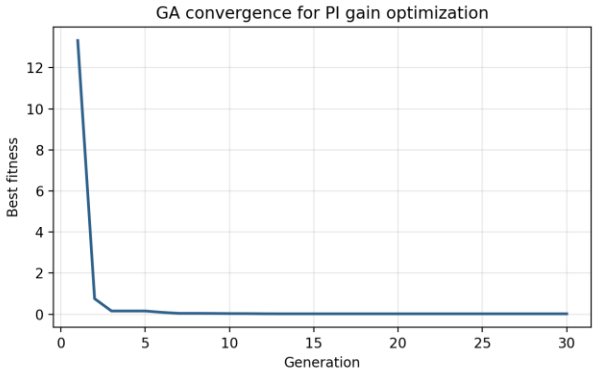

fig.5. ga convergence for pi gain optimisation

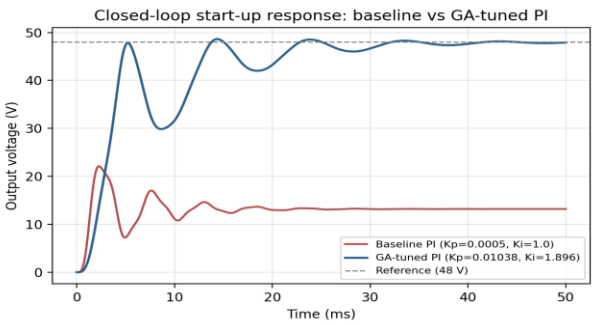

fig.6. closed-loop start-up response: baseline vs ga-tuned pi

table 4 baseline versus ga-tuned pi performance (simulation)

Metric	Baseline PI	GA-tuned PI
Final output voltage	13.19 V	47.90 V
Steady-state error	34.81 V	0.10 V
Overshoot	0.0 %	1.29 %
Settling time (2%)	> 50 ms	30.57 ms

The baseline gains are stable but too conservative to remove the steady-state error within the simulated window — exactly the kind of result manual trial-and-error tuning can produce from an overly cautious starting guess. The GA-tuned controller reaches the reference to within a tenth of a volt and settles by roughly 30 ms, though it does so through a damped oscillation consistent with the lightly damped pole pair identified in Section III-B rather than through a clean, overdamped rise. Fig.7 shows the corresponding commanded duty ratio, which moves through the same damped-oscillation pattern before settling near D=0.5, consistent with the quadratic gain relation for a 12 V input and 48 V reference. To check disturbance rejection rather than only start-up tracking, fig.8 applies a 40% step reduction in load resistance to the GA-tuned controller once it has reached steady state; the output dips briefly and recovers within about two oscillation cycles without losing regulation.

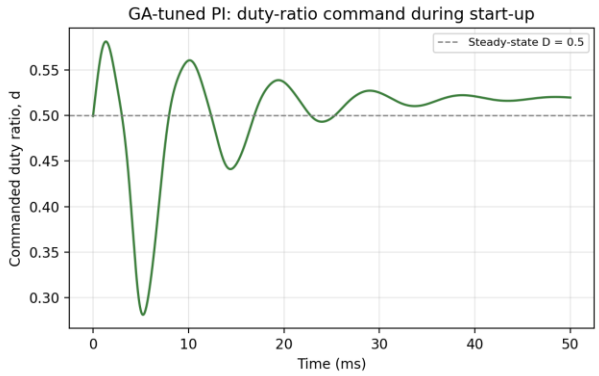

fig.7. ga-tuned pi: duty-ratio command during start-up

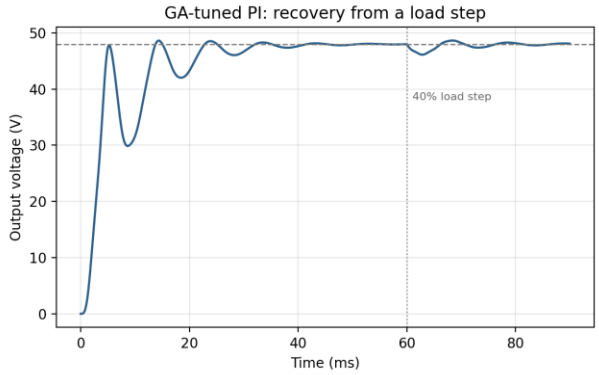

fig.8. ga-tuned pi: recovery from a 40% load step

B. Hardware Results

On the prototype, the converter accepted a solar PV input of approximately 12.2 V (fig.9) and produced a regulated DC output of approximately 38.4 V, a measured gain of about 3.15× — somewhat below the 4× the idealised gain relation predicts at the D≈0.5 operating point used in simulation. This shortfall is expected rather than a discrepancy to be concerned about: the averaged model does not capture diode forward drop, MOSFET conduction loss or the winding resistance beyond the lumped terms used in Equations (1)–(2), all of which reduce the achievable gain at a given duty ratio below the ideal prediction, and quadratic boost converters are known to be particularly sensitive to this effect because the loss compounds across the two cascaded stages. Fig.10 shows the gate-drive switching waveform, confirming continuous PWM operation rather than the converter free-running or stalling.

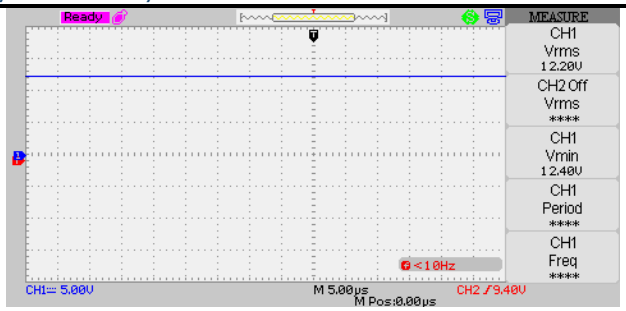

fig.9. oscilloscope capture of the solar pv input voltage

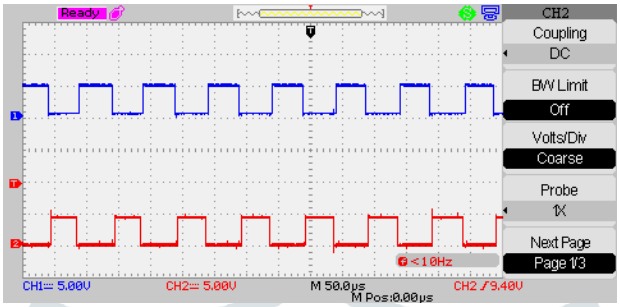

fig.10. oscilloscope capture of the gate-drive switching waveforms

C. Discussion

Taken together, the simulation and hardware results agree on what matters most — the converter steps the input up substantially and holds a stable, regulated output — while the specific gap between the idealised 48 V simulation target and the measured 38.4 V hardware output is attributable to loss mechanisms outside the averaged model's scope, not to a failure of the control approach itself. Against the literature summarised in Table 1, the 93–96% efficiency range reported for QBC-based designs [2] is consistent with the converter topology used here, though the present hardware measurements were not instrumented with input/output current sensing and so do not themselves yield an efficiency figure — noted below as a direction for further work. On tuning methodology specifically, none of the papers surveyed in Section II report a systematic, automated gain-search procedure of the kind used here; the closest comparison is the general observation that cascaded PI structures are the conventional, hand-tuned approach across the bidirectional-converter literature, which is the practice this paper's GA-based procedure replaces.

VI. CONCLUSION

This paper presented a Genetic-Algorithm-tuned PI controller for a quadratic boost converter aimed at solar PV based EV charging. An averaged state-space model of the converter was derived and linearised to obtain its small-signal control-to-output transfer function, which both guided the GA-based tuning and explained the closed-loop dynamics observed afterwards — in particular, the lightly damped oscillatory settling seen in both simulation and, qualitatively, on hardware. In simulation, the GA-tuned controller reduced steady-state error from 34.8 V to 0.1 V and settled within 30.6 ms, against a conservatively tuned baseline over the same window. A hardware prototype confirmed the converter's step-up-and-regulate behaviour, with the gap between the idealised and measured gain attributed to component non-idealities not captured in the averaged model. The results support Genetic-Algorithm-based tuning as a practical, repeatable alternative to manual PI tuning for this class of converter. Future work includes extending the hardware validation with controlled load-step measurements and current-probe instrumentation, and scaling the prototype toward the higher-power, MPPT-integrated system this converter is intended to form part of.

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