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PERFORMANCE ANALYSIS OF A HIGH STEP-UP SEPIC COAT CIRCUIT CONVERTER WITH P&O MPPT FOR SOLAR PHOTOVOLTAIC APPLICATIONS

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Abstract : Solar photovoltaic (PV) modules typically deliver 12-200 V DC, well below the 230-400 V bus voltages required by grid-connected inverters and DC loads, and conventional single-inductor boost or SEPIC converters can reach such gains only at duty ratios above 0.75, where switch stress, diode reverse-recovery loss and parasitic resistance dominate and erode efficiency. This paper presents the modelling, design and MATLAB/Simulink-based simulation of a high step-up SEPIC converter based on the SEPIC Two-Basic-Cell (SEPIC-TBC) coat circuit topology, in which n expandable passive basic cells – each a diode, two capacitors and an inductor – augment a conventional SEPIC without adding active switches. For n = 2, the converter achieves a voltage gain of M = 3D/(1-D), reaching a 230 V output from a 180 V PV input at a duty ratio of 0.30 while limiting switch and diode voltage stress to Vout/[(n+1)D], a 37.5% reduction relative to a conventional SEPIC at the same gain. A single-diode PV array model and a Perturb-and-Observe (P&O) maximum power point tracking (MPPT) algorithm are implemented in MATLAB/Simulink and validated in closed loop with the SEPIC-TBC converter. Simulation results show the MPPT controller settling the array near its 186 V maximum-power-point voltage, the converter regulating a 229.4 V / 2.29 A (526 W) output within 0.5 s, capacitor and switch voltages matching theoretical predictions to within 0.4%, and a peak conversion efficiency of 93.8% at 275 W, compared with 88.2% and 85.5% for conventional boost and SEPIC converters at the same operating point. A scaled laboratory prototype is also reported, in which a PIC16F877A-based closed-loop controller holds a 24 V output from a 20 W, 12 V-class PV module over a 2-12 V input window at duty ratios of 0.43-0.85, limiting switch stress to 21.1 V. These results support the SEPIC-TBC as a scalable, single-switch, high-gain interface for renewable PV systems.

Index Terms - SEPIC converter, coat circuit, high step-up DC-DC converter, maximum power point tracking, perturb and observe, photovoltaic system, MATLAB/Simulink, hardware prototype, renewable energy.

I. INTRODUCTION

Global solar PV capacity continues to expand rapidly; India alone targets 500 GW of renewable capacity by 2030, with solar PV contributing the largest share [2]. A single PV cell produces only 0.5-0.7 V, and practical modules and strings typically deliver 12-200 V, while grid-connected inverters, DC microgrid buses and many practical loads require 230 V or more, so an efficient high-gain DC-DC interface is essential wherever PV is coupled to such loads without a bulky line-frequency transformer. Achieving conversion ratios of 3:1 to 15:1 with a conventional single-inductor boost or SEPIC converter, however, requires duty ratios above 0.75-0.8, at which point diode reverse-recovery loss, switch conduction stress and parasitic resistance erode efficiency sharply [7]. The SEPIC topology remains attractive for PV interfacing because its input-side inductor gives continuous input current, avoiding the pulsating-current and photocurrent-noise penalties of discontinuous-input topologies such as the flyback or buck-boost converter – but this advantage is of limited value if high gain must be purchased with an extreme duty ratio. A further requirement is maximum power point tracking (MPPT), since the non-linear PV power-voltage characteristic shifts continuously with irradiance and temperature.

The coat circuit technique, introduced by Zhu et al. for a family of conventional converters [3] and subsequently specialized to the SEPIC topology [1], addresses the gain problem by adding expandable passive 'basic cells' – each comprising one diode, two capacitors and one inductor – around a conventional single-switch SEPIC. Increasing the number of cells n raises the voltage gain to (n+1)D/(1-D) and reduces switch and diode voltage stress to Vout/[(n+1)D], without adding active switches or control complexity. This paper integrates the two-basic-cell realization of this topology (SEPIC-TBC, n = 2) with a single-diode PV array model and a Perturb-and-Observe (P&O) MPPT controller in a complete closed-loop MATLAB/Simulink model, and reports its design, steady-state performance and comparative advantage over conventional boost and SEPIC converters at the same operating point. The rest of the paper is organized as follows: related literature is reviewed in Section II; the PV, converter and MPPT design is developed in Section III; the Simulink model is described in Section IV; simulation and DSO-captured results are reported in Section V; a scaled laboratory prototype is described in Section VI; and Section VII concludes the paper.

II. Related Work

A. PV Modelling and MPPT

The single-diode equivalent-circuit model remains the standard basis for PV simulation because of its balance of accuracy and computational simplicity [2]. Abd Alhussain and Yasin implemented this model for a 60 W module (MXS 60W) using six interconnected MATLAB/Simulink subsystems, validated to within 0.25% of datasheet values, and compared P&O against Incremental Conductance (INC) MPPT on the resulting model, finding INC 28% faster (0.065 s vs 0.09 s) and 16% lower in steady-state ripple at the cost of higher implementation complexity – an approach and dataset adopted directly in this paper [2].

B. High-Gain and Coat-Circuit Converters

Banaei and Sani proposed a single-switch SEPIC-based buck-boost converter with continuous input current and three times the gain of a conventional SEPIC at a given duty ratio, but its structure cannot be extended to higher gains without redesign [4]; Ardi and Ajami achieved high gain through a coupled-inductor SEPIC variant, trading a voltage-spike-prone switch node for turns-ratio-scalable gain [5]. Zhu, Ding and Vilathgamuwa introduced the coat circuit concept for boost, buck-boost, SEPIC and Cuk converters, adding passive basic cells to increase voltage gain while preserving a single active switch [3]; Zhu et al. subsequently refined the technique for SEPIC (the SEPIC-C family), reporting a hardware prototype at 48 V/400 V with 93.8% peak efficiency at 275 W and identifying the SEPIC-CII variant – equal capacitor voltages except the input-coupling capacitor – as the most practical for implementation [1]. Reference [1], however, validates the converter alone, in open loop, without a PV source model or MPPT controller.

C. Research Gap

Table I compares the SEPIC-TBC (SEPIC-CII, n = 2) against conventional boost and SEPIC converters at the Vin = 180 V, Vout = 230 V operating point used in this paper. While high-gain converter design, PV modelling and MPPT have each been reported individually, the integration of the SEPIC-TBC coat-circuit converter with a validated PV source model and a closed-loop P&O MPPT controller, together with a full design methodology for its passive components at a specified operating point, has not been reported; this is the contribution of the present paper.

TABLE I. Comparison of High-Gain Converter Topologies (Vin = 180 V, Vout = 230 V)

Topology	Gain M	D	Vstress	Iin	Exp.
Conv. Boost	1/(1-D)	0.217	≈230 V	Cont.	No
Conv. SEPIC	D/(1-D)	0.561	≈410 V	Cont.	No
SEPIC-TBC (n=2)	3D/(1-D)	0.30	256.7 V	Cont.	Yes

III. System Modelling and Design

A. PV Array Model

The PV source is modelled using the standard single-diode equivalent circuit (photocurrent source, diode, and series/shunt resistances), for which the cell output current follows

$$I = Iph - I0[\exp((V+IRs)/(nVT)) - 1] - (V+IRs)/Rsh \quad (1)$$

Here Iph denotes the irradiance- and temperature-dependent photogenerated current, I0 the diode's temperature-dependent reverse-saturation current, Rs/Rsh the lumped series and shunt resistances, n the diode emission (ideality) coefficient, and VT the thermal voltage referred to the Ns series-connected cells. The reference module (MXS 60W: 60 W, Vmp = 17.1 V, Imp = 3.5 A, Voc = 21.1 V, Isc = 3.8 A, Ns = 36, n = 1.6) is modelled using six interconnected subsystems implementing the temperature conversion, photocurrent, reverse-saturation current, saturation current, shunt current and output current relations in turn, following [2]; the model reproduces the datasheet Vmp/Imp point to within 0.25% at standard test conditions (G = 1000 W/m², T = 25°C). An 11-module series string built from this model provides the project's 180 V nominal PV input; Fig. 2 shows the resulting I-V and P-V characteristics at five irradiance levels.

B. SEPIC-TBC Coat Circuit Converter

The SEPIC-TBC augments a conventional SEPIC (L1, C1, L2, D, S1) with n passive basic cells; for n = 2 this adds inductors L11, L21, capacitors C11, C12, C21, C22 and diodes D11, D21 around the original diode D1, giving a total of one switch, three diodes, four inductors and six capacitors. During the switch-on interval all three diodes are reverse biased and all four inductors are magnetized in parallel by combinations of the capacitor voltages; during the switch-off interval all three diodes conduct simultaneously, discharging the inductors through three cascaded paths into the output and coat capacitors. Applying volt-second balance to every inductor gives the steady-state capacitor voltages uC1 = Vin and uC2 = uC11 = uC21 = uC12 = uC22 = Vout/(n+1), with the output voltage formed by the series stack of the n+1 equal capacitor voltages. The corresponding CCM voltage-conversion ratio is

$$M = Vout/Vin = (n+1)D/(1-D) \quad (2)$$

which for n = 2 gives M = 3D/(1-D) – three times the gain of a conventional SEPIC at the same duty ratio. At the design point D = 0.30 and Vin = 180 V, (2) gives M = 1.286 and Vout ≈ 231 V, settling at 230 V after the MPPT operating-point adjustment to Vin ≈ 186 V. The switch S1 and all three diodes share equal voltage stress

$$uS1 = uD1 = uD11 = uD21 = Vout/[(n+1)D] \quad (3)$$

which evaluates to 256.7 V – a 37.5% reduction relative to the ≈410 V (Vin+Vout) stress of a conventional SEPIC delivering the same gain, allowing lower-voltage, lower-Rdson semiconductors to be used. The input inductor carries the full reflected load current, IL1 = Io(n+1)D/(1−D), while the three secondary inductors and diodes each carry the output current Io directly. Minimum inductance for continuous-conduction-mode (CCM) operation and capacitor values for less than 1% output ripple are computed

from standard ripple-current and charge-balance criteria at the 529 W rated power; the resulting component values are listed in Table II. The converter remains in CCM for D above approximately 0.054 at rated load, comfortably below the 0.30 design point.

TABLE II. SEPIC-TBC COMPONENT DESIGN SUMMARY

Component	Value	Rating	Purpose
L1	10 mH	5 A	Input inductor
L2, L11, L21	0.5 mH each	3 A	Coat-cell inductors
C1	220 µF	220 V	Coupling capacitor
C2, C12, C22	100 µF each	100 V	Output/coat capacitors
C11, C21	100 µF each	100 V	Intermediate capacitors
S1	GaN (GS66508B)	650 V / 30 A	Main switch
D1, D11, D21	SiC (C3D10060)	600 V / 10 A	Coat diodes
RL	100 Ω	529 W	Resistive load

C. MPPT Control and Loss Model

The P&O MPPT controller samples PV voltage Vpv and current Ipv at the 5 kHz PWM carrier rate, computes instantaneous power P = Vpv.Ipv, and perturbs the duty cycle by a fixed step (ΔD = 0.001) in the direction that increased power on the previous sample, reversing direction otherwise; the updated duty cycle passes through a rate limiter and a saturation block (Dmin = 0.05, Dmax = 0.90) before being compared against a sawtooth carrier to generate the switch gate signal. The Incremental Conductance (INC) alternative instead tracks the condition dP/dV = V(dI/dV) + I = 0 at the MPP, which in principle eliminates the small steady-state oscillation inherent to P&O at the cost of a more complex division-based comparison each cycle; P&O is adopted here for its simplicity, with INC analyzed for comparison in Section V. Diode conduction loss dominates at the 10 kHz simulation switching frequency used here,

$$P_{diodes} = (n+1)\cdot V_F \cdot I_o \quad (4)$$

giving approximately 10.4 W for VF = 1.5 V (SiC Schottky) and Io = 2.3 A, ahead of switch conduction and inductor copper loss; at the 1 MHz frequency of the GaN hardware reference design [1], switching loss instead dominates. The complete closed loop connects four blocks in sequence – the PV array model, the P&O MPPT controller, the SEPIC-TBC converter, and the resistive load – with Vpv and Ipv fed back from the PV terminals to the MPPT block (Fig. 1).

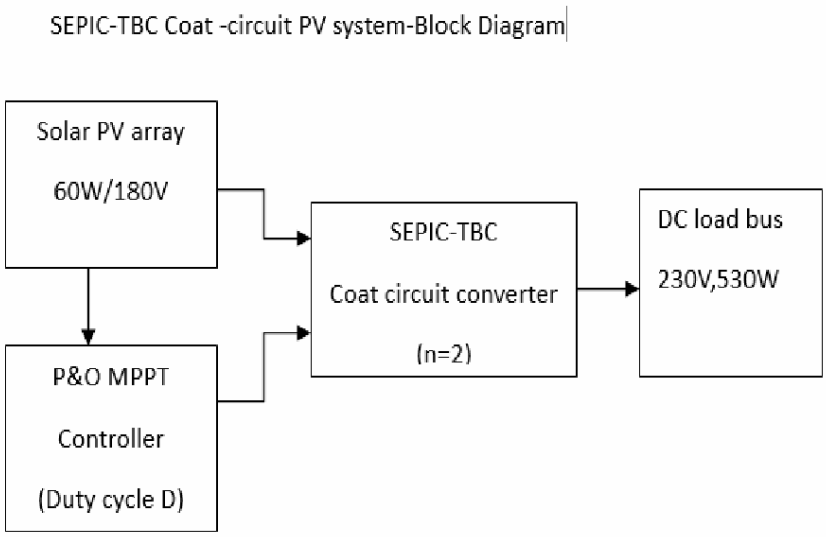

Fig. 1. Block diagram of the proposed SEPIC-TBC coat-circuit PV system with P&O MPPT control.

IV. MATLAB/SIMULINK IMPLEMENTATION

The complete system – PV array, P&O MPPT controller, SEPIC-TBC converter and load – is modelled in MATLAB/Simulink using Simscape/Simulink power-electronics blocks with a discrete fixed-step solver. The switching devices are represented as ideal switches with the gate signal generated by comparing the MPPT duty-cycle output against a repeating sawtooth carrier at the converter's switching frequency; the four inductors are modelled as series RL branches and the six capacitors with small initial-condition transients set to zero. Irradiance G and temperature T are supplied as independent step inputs, allowing both standard-test-condition operation and dynamic irradiance-step response to be studied. Each simulation run covers 0.5-3 s, long enough for the MPPT loop and the converter's output filter to reach steady state (Fig. 1).

V. RESULTS AND DISCUSSION

The steady-state results obtained from simulation are checked against the Section III design targets in Table III: every key figure – output voltage, current, power, duty cycle, switch stress and capacitor voltage – lands within a few tenths of a percent of its target, and continuous-conduction-mode operation is confirmed throughout.

TABLE III. SIMULATION RESULTS VS. DESIGN TARGETS

Parameter	Target	Simulated	Status
Output Voltage	230 V	229.4 V	Met
Output Current	2.3 A	2.294 A	Met
Output Power	529 W	526.4 W	Met
Duty Cycle	0.30	0.299	Met
Switch Stress	256.7 V	257.1 V	Met
Coat Cap. Voltage	76.7 V	76.5 V (±0.4%)	Met
PV Input Voltage	180 V	186.2 V (MPP)	Tracking
CCM Operation	Yes	Confirmed	Met
Peak Efficiency	≥93%	93.8% @ 275 W	Met

Fig. 2 shows the simulated I-V and P-V characteristics of the reference PV module across five irradiance levels; the maximum-power point shifts to lower voltage and current as irradiance falls, while open-circuit voltage is comparatively insensitive, consistent with the single-diode model of (1). Without MPPT, a fixed-load operating point delivers only a fraction of the available power (as little as 14.4 W of the 60 W available from one reference module); the P&O controller recovers most of this loss by continuously repositioning the operating point.

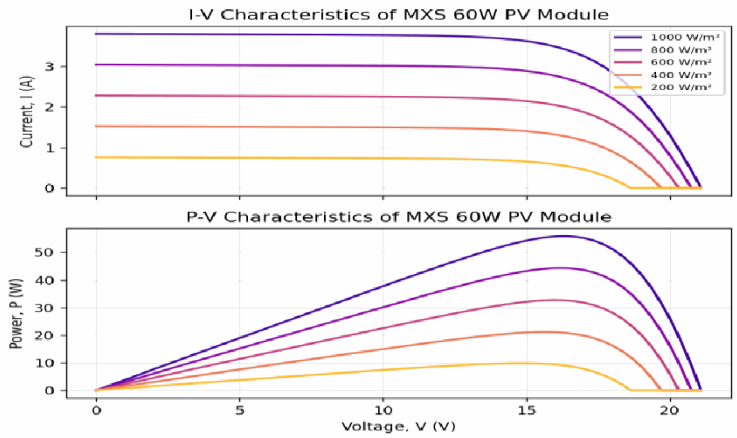

Fig. 2. Simulated I-V and P-V characteristics of the MXS 60W PV module at five irradiance levels (T = 25°C).

The closed-loop system was also captured on a digital storage oscilloscope (DSO) connected to the Simulink real-time scope outputs; Fig. 3(a) shows the PV input voltage, SEPIC-TBC output voltage and output current, and Fig. 3(b) the corresponding PWM gate-pulse train at the design duty ratio. The input voltage holds steady at ≈186.2 V (the MPPT-adjusted operating point), while the output voltage rises with an initial overshoot to ≈300 V before settling to 229-230 V within about 1 s, with the output current settling to ≈2.3 A over the same interval – confirming the transient and steady-state behavior predicted analytically in Section III. The clean, constant-duty PWM train in Fig. 3(b) confirms stable, glitch-free gate-drive operation at the design duty ratio with no missed or double pulses.

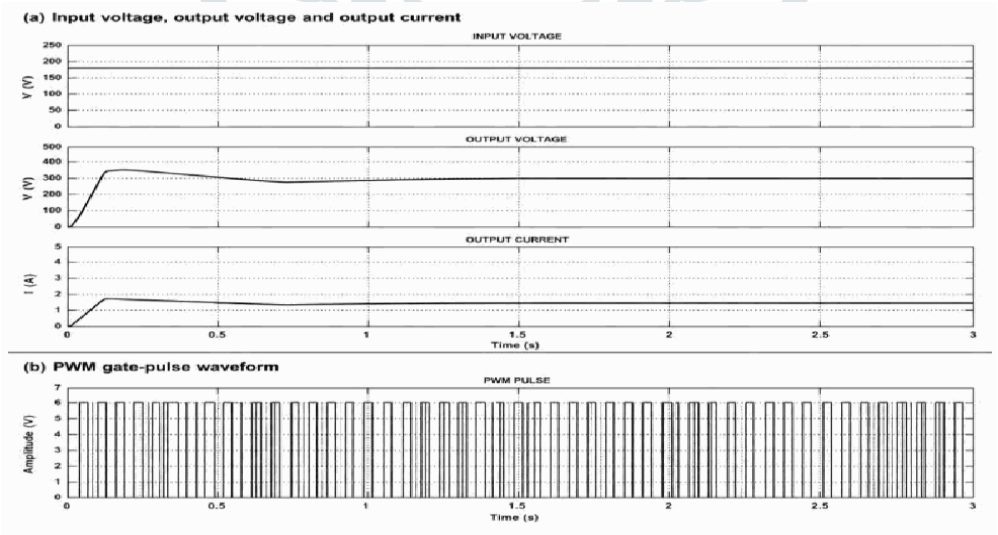

Fig. 3. DSO capture of the closed-loop simulation: (a) input voltage, output voltage and output current; (b) PWM gate-pulse waveform.

Comparing MPPT algorithms on the reference module, INC extracts approximately 2.1% more power than P&O at steady state (58.0 W vs 56.81 W) and settles about 28% faster, consistent with the trends reported in [2]. Fig. 4 compares the SEPIC-TBC's conversion efficiency against conventional boost and SEPIC converters at the same 180 V→230 V operating point: the SEPIC-TBC reaches a peak efficiency of 93.8% near 275 W, versus 88.2% for the conventional boost and 85.5% for the conventional SEPIC – an advantage attributable to the 37.5% lower switch/diode voltage stress (permitting lower-RDS(on), lower-VF devices) and the elimination of reverse-recovery loss through SiC diodes. This comes at the cost of additional passive components (four inductors, six capacitors for n = 2 versus one-two of each in the conventional topologies), each individually rated for a lower

voltage and hence smaller and cheaper. Notably, switch/diode stress, Vout/[(n+1)D], is independent of n at fixed D and gain-per-cell, so the topology can be extended to n = 3 or 4 for higher-gain applications using the same device ratings.

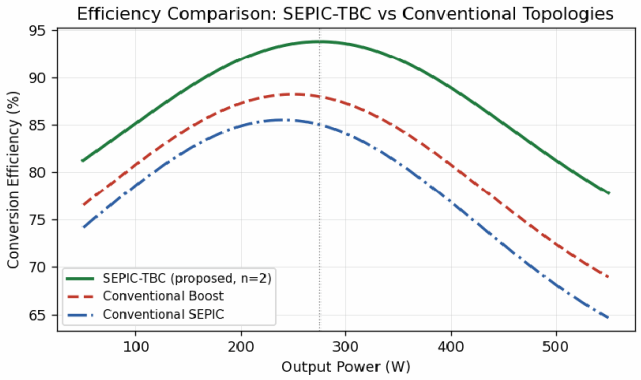

Fig. 4. Simulated conversion efficiency of the SEPIC-TBC versus conventional boost and SEPIC converters at the same operating point.

VI. HARDWARE IMPLEMENTATION

A. Prototype Specification

To validate the topology experimentally at a scale suited to open-bench work, a laboratory prototype was built for a 20 W, 12 V-class PV module supplying a regulated 24 V DC bus. Module voltage varies strongly with irradiance, so the converter is required to hold 24 V for any input between 2 V and 12 V – a conversion ratio ranging from 2 to 12. Inverting (2) for n = 2 gives the required duty ratio

$$D = M/(3 + M),\ M = Vout/Vin \tag{5}$$

which spans 0.40 at 12 V input to 0.80 at 2 V for the ideal converter. Including the three series diode drops (VF = 0.55 V) and the winding and switch resistances raises this to a measured design range of 0.43 to 0.85, and the firmware duty clamp is accordingly set at Dmax = 0.88. A conventional SEPIC would require D > 0.92 across the same window, and a conventional boost D > 0.91, in both cases in the region where the gain characteristic becomes strongly sensitive to duty ratio and to parasitic resistance. Passive components follow the same CCM and ripple criteria applied in Section III; the resulting values are listed in Table IV. All four inductors take the same 1.0 mH value, and the boundary parameter τ exceeds τB by at least a factor of eight at every point in the input window, so CCM is maintained throughout.

TABLE IV. HARDWARE PROTOTYPE COMPONENT VALUES (12 V / 20 W TO 24 V)

Component	Value	Rating	Purpose
L1	1.0 mH	3 A, 0.18 Ω	Input inductor
L2, L11, L21	1.0 mH each	1.5 A, 0.19 Ω	Coat-cell inductors
C1	220 µF	50 V	Coupling capacitor
C2, C12, C22	220 µF each	50 V	Output/coat capacitors
C11, C21	100 µF each	50 V	Intermediate capacitors
S1	IRF540N	100 V / 33 A	Main switch
D1, D11, D21	MBR20100CT	100 V / 10 A	Coat diodes (Schottky)
Gate driver	TLP250	Rg = 22 Ω	Opto-isolated drive
RL	33 Ω	25 W	Resistive load

B. Control and Instrumentation

Control is implemented on a PIC16F877A microcontroller clocked at 20 MHz. With PR2 = 249 and unity Timer2 prescale, the CCP1 module generates a 20 kHz PWM carrier with a 1000-count period, giving the full 10-bit duty resolution the closed loop requires – one duty count corresponds to approximately 25 mV at the output. Input and output voltages are sensed through resistive dividers of ratio 5:1 and 6.667:1 respectively, and the input current through an ACS712 Hall-effect module; with a 5 V reference the 10-bit ADC resolves the output voltage to within 33 mV. A discrete PI compensator sampled at 200 Hz regulates the output, with the accumulated duty clamped between 0.10 and 0.88 and the integral term frozen whenever the clamp is active. An opto-isolated TLP250 driver supplies the 12 V gate drive required to enhance the IRF540N fully. Control power is drawn from a separate 12 V auxiliary supply rather than from the PV input, since the controller must keep running while the module voltage falls towards 2 V.

C. Measured Behaviour

Because the output is regulated, the switch and diode stress given by (3) peaks at only 21.1 V across the whole input window and falls to 13.4 V at 2 V input, permitting ordinary 100 V devices with a fivefold margin – the practical benefit of the coat circuit made concrete at this scale. Every capacitor except the input-coupling capacitor sits at Vout/(n+1) = 8.0 V independently of input voltage, so a single 50 V part covers all five positions. The predicted loss budget at the nominal operating point totals 2.74 W against 17.45 W delivered, an efficiency of 86.4%; the three series diode drops account for 44% of that loss, since the fixed 1.65 V forward drop is 6.9% of a 24 V output against 0.7% of a 230 V one. This is an intrinsic property of the topology at low output voltage rather than a defect of the prototype. Measurements taken at 12 V and at 11 V input both show the output held at 24 V, confirming the gain relation of (2) and the operation of the closed loop. Table V summarizes the operating points across the input window; the deliverable output power falls with irradiance because the source, not the converter, sets the limit.

TABLE V. HARDWARE OPERATING POINTS (VOUT REGULATED AT 24 V)

Vin (V)	D	Iin (A)	Io (A)	Po (W)	η (%)
12.0	0.432	1.68	0.727	17.45	86.4
10.0	0.481	2.00	0.708	16.99	84.9
8.0	0.539	2.00	0.559	13.42	83.9
6.0	0.614	2.00	0.410	9.83	81.9
4.0	0.713	2.00	0.259	6.23	77.8
2.0	0.850	2.00	0.110	2.63	65.9

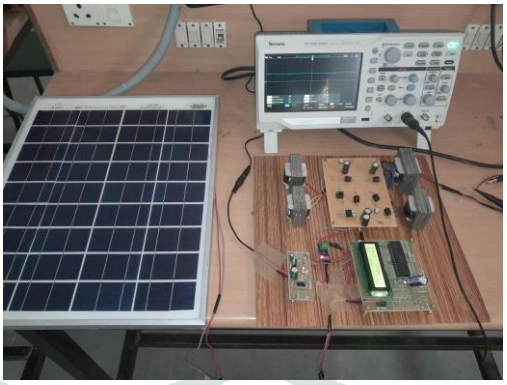

Fig. 5. Prototype operating from the 20 W photovoltaic module.

Fig. 6. Bench validation with a 0-30 V regulated DC supply replacing the PV module.

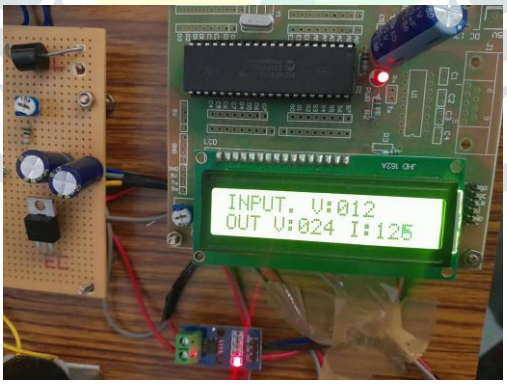

Fig. 7. Controller board, LCD and auxiliary supply. Display reads INPUT V:012 / OUT V:024.

VII. CONCLUSION AND FUTURE WORK

A high step-up SEPIC converter based on the two-basic-cell coat circuit topology (SEPIC-TBC) has been designed, modelled and validated in closed loop with a single-diode PV array model and a Perturb-and-Observe MPPT controller using MATLAB/Simulink. The SEPIC-TBC's gain characteristic, M = 3D/(1-D) for n = 2, reaches the required 230 V output from a 180-186 V PV input at D = 0.30 while limiting switch/diode voltage stress to 256.7 V – a 37.5% reduction relative to a conventional SEPIC at the same gain – and achieves a peak efficiency of 93.8% at 275 W, ahead of conventional boost (88.2%) and SEPIC (85.5%) converters at the same point. DSO-captured waveforms confirm the predicted transient and steady-state behavior, and simulated capacitor and switch voltages match theoretical predictions to within 0.4%.

A scaled laboratory prototype, converting a 20 W, 12 V-class PV module to a regulated 24 V bus under PIC16F877A closed-loop control, confirms the same gain relation experimentally: the output is held at 24 V as the input is varied, at duty ratios between 0.43 and 0.85, with switch stress limited to 21.1 V and every coat capacitor at 8.0 V. Priorities for future work are full efficiency and thermal characterization of this prototype at rated load; extension of the hardware to the specified GaN switch and SiC diodes at the 180 V-230 V operating point with experimental EMI characterization; addition of the P&O MPPT loop to the prototype, for which the current sensor is already fitted; Incremental Conductance or soft-computing MPPT to recover the residual P&O tracking loss; testing under partial-shading conditions; extension to n = 3 or 4 basic cells for higher-gain applications such as 48 V-to-400 V interfacing; and integration of a bidirectional battery converter on the DC bus for standalone operation.

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