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DESIGN METHODOLOGY AND PERFORMANCE SIMULATION OF A 16-BIT SAR ANALOG-TO-DIGITAL CONVERTER IN 90-nm CMOS

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Abstract : This paper presents the design and transient-level verification of a 16-bit Successive Approximation Register(SAR) Analog-to-Digital(ADC) using 90-nanometer CMOS technology in the Cadence Virtuoso design environment (GPDK090) using the Cadence Virtuoso design environment. The proposed ADC integrates a precharged bootstrapped sampling switch and a two-stage dynamic latch comparator, whose architectures are adapted from an existing 8-bit SAR ADC design, together with a newly designed 16-bit binary weighted bridge-capacitor Digital-to-Analog Converter (CDAC) that extends the reference 8-bit CDAC concept to higher resolution while limiting the total array capacitance and area. A custom successive-approximation control-logic block sequentially resolves the 16 bit output code from the most significant bit (D15) to the least significant bit (D0). Operating from a 1.2-V supply, the bootstrapped switch and the dynamic comparator individually consume power of 295.4 nW and 265.8 nW, respectively, while the complete 16-bit SAR ADC dissipates 460.9 µW power. Transient simulation results confirm correct bootstrapped gate-voltage tracking, proper regenerative comparator switching, and monotonic bit-cycling of the SAR logic across the full 16-bit conversion cycle, validating the functional correctness of the proposed architecture for low-power, high-resolution data-acquisition applications.

IndexTerms **- SAR ADC, Bootstrapped Switch, Bridge Capacitor CDAC, Dynamic Latch Comparator, Successive Approximation Logic, 90 nm CMOS, Low Power.**

I. INTRODUCTION

Analog-to-digital converters(ADCs) connect the analog world to digital processing systems by turning a sampled voltage into a numerical code. Successive Approximation Register (SAR) architectures are a common choice whenever a design needs moderate-to-high resolution together with low power and a small footprint. A SAR converter is typically built from four blocks, a sample-and-hold circuit, a comparator, a capacitive DAC, and a digital controller and it converts by running a binary search: on each clock cycle the comparator's decision fixes one more output bit. Because every bit relies on the previous decision, the accuracy and energy efficiency of the whole converter are tightly coupled to how well these four blocks work together.

Linearity is strongly shaped by the sampling switch: bootstrapping the switch keeps the sampling transistor's gate-to-source voltage roughly constant across the input swing, which flattens out the on-resistance and reduces the distortion it would otherwise cause. Dynamic-latch comparators fit SAR converters well for a related reason, they are clocked rather than continuously biased, so they draw current only when they are actually deciding. As resolution climbs, capacitor mismatch in the DAC becomes the dominant nonlinearity source, so the CDAC topology needs careful attention; calibration schemes and split or bridge-capacitor arrays are the usual ways to keep the capacitance and matching under control.

Building on this, the present work assembles a 16-bit SAR ADC around a precharged bootstrapped sampler and a dynamic-latch comparator carried over from the 90-nm 8-bit design in [2]. Its DAC is scaled up to 16 bits through a bridge-capacitor arrangement, and a purpose-built SAR controller drives the conversion from the MSB down to the LSB. The full converter is implemented and characterized at the transistor level in Cadence Virtuoso on the GPDK090 process.

Section II reviews the two reference designs, Section III lays out the proposed architecture block by block, Section IV presents and discusses the simulation results, and Section V closes with conclusions and directions for future work.

II. LITERATURE SURVEY

In [1], Ding et al. built a 180-nm, 16-bit SAR ADC that runs at 1 MS/s. Capacitor mismatch is corrected through foreground calibration based on a floating-capacitor technique, with the LSB capacitors organized in a round-robin scheme; the design also uses a precharged bootstrapped switch and a small custom capacitor within the CDAC. At 100 kS/s the reported SFDR is 108.9 dB, falling to 92.38 dB at the full 1-MS/s rate, and the converter draws 6.745 mW.

Reference [2] by Lakkannavar et al. describes an 8-bit SAR ADC built in the same 90-nm GPDK090 process and designed in Cadence Virtuoso. It uses a bootstrapped NMOS sampler, a two-stage dynamic-latch comparator, and a nine-unit-capacitor binary-weighted CDAC switched through transmission gates. Running at 0.9 V and 1 MHz, the comparator is reported to consume 0.2856 mW, and the simulated DAC output tracks the expected codes closely.

These two designs offer complementary starting points: [1] targets 16-bit resolution with mismatch calibration but at a coarser 180-nm node, while [2] stays at 8 bits but in the finer 90-nm process with low-power analog blocks. The present design borrows the bootstrapped switch and dynamic comparator from [2] and pushes the bridge-capacitor idea further to build a full 16-bit CDAC effectively pairing the 90-nm circuit blocks of [2] with a higher-resolution DAC structure.

III. PROPOSED 16-BIT SAR ADC ARCHITECTURE

Figure 1 shows the four blocks that make up the converter, the bootstrapped sampling switch, the dynamic-latch comparator, the 16-bit bridge-capacitor CDAC, and the SAR control logic. The bootstrap stage samples the input (a 100-kHz, 480-mV-amplitude sinusoid riding on a 600-mV offset in the testbench) onto the CDAC's top plate. The comparator then weighs the sampled voltage VDAC against the internal reference built up on the CDAC and passes its decision (OUTP, OUTN) to the SAR logic, which updates the code D[15:0] driving the CDAC switches. All blocks share a single 1.2-V supply (VDD = VREF = 1.2 V) and are implemented entirely in 90-nm CMOS.

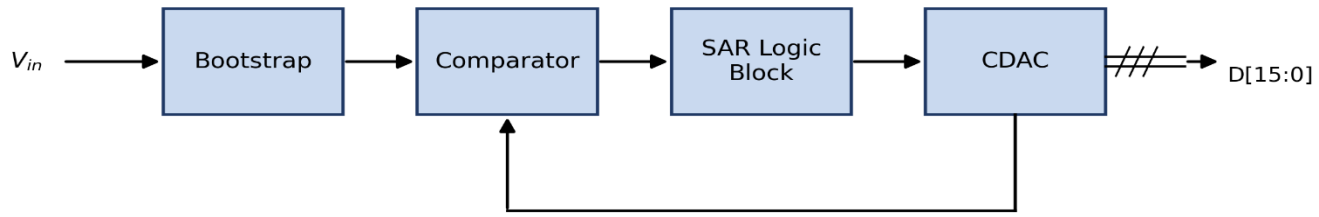

Fig. 1. Block-level Diagram of the proposed 16-bit SAR ADC

A. Bootstrapped Sampling Switch

A bootstrap capacitor C_b, precharged ahead of the sampling phase, supplies the elevated gate voltage the NMOS sampling device needs during sampling. During the preceding hold or conversion phase, $C_b$is charged from the supply rail; once sampling begins, that stored charge transfers to the gate node so the gate voltage tracks the input signal. This keeps the gate-to-source voltage nearly constant and limits how much the switch resistance varies with the input level. Auxiliary switches and inverters provide the precharge and discharge paths for both capacitors.

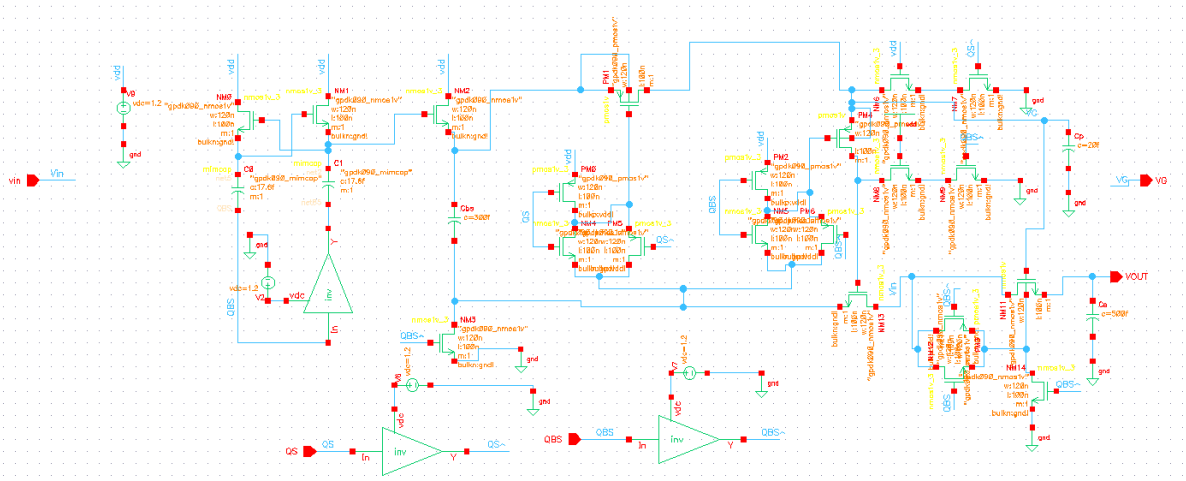

Fig. 2. Schematic of the proposed precharged bootstrapped sampling switch

The transient behavior in Figure 3 confirms this operation. During the sampling interval, the simulated gate voltage V_G rises roughly in step with the applied input, which is the expected bootstrap effect, and settles back to a controlled level during the complementary hold interval. The block's simulated average power is 295.4 nW.

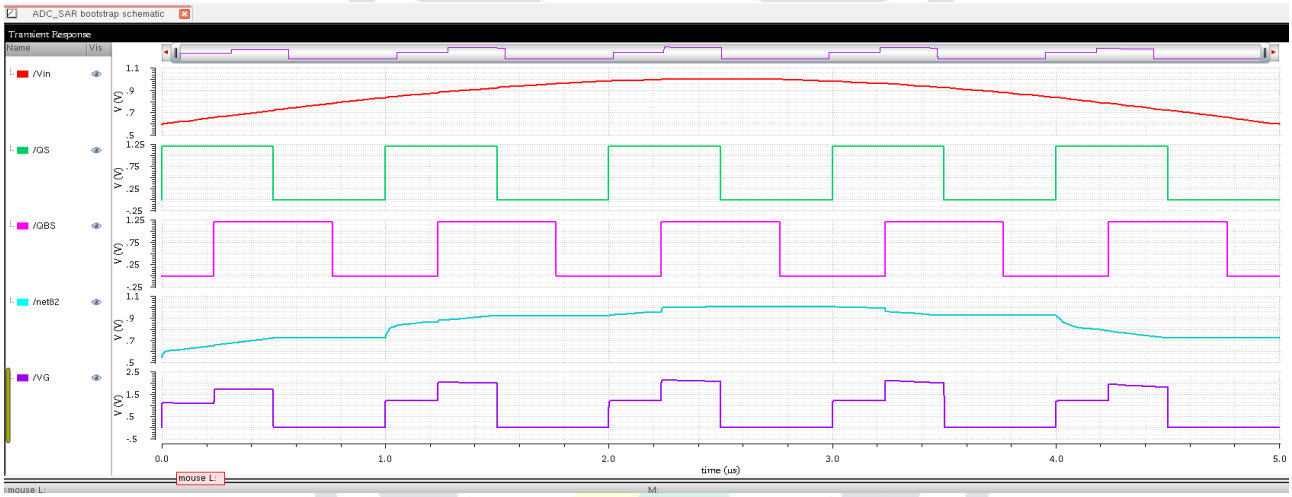

Fig. 3. Transient response of the bootstrapped switch (Vin, QS, QBS, VG).

B. Dynamic Latch Comparator

The comparator is a two-stage dynamic latch. Its first stage takes the differential inputs V_{in+} and V_{in-} and builds up a small voltage difference during evaluation, with reset transistors first pulling the internal nodes to known starting values before each comparison. That small difference then drives a second-stage regenerative latch , a pair of cross-coupled inverters which amplifies it to full, complementary logic-level outputs. A single clock signal toggles the comparator between its reset and evaluation states.

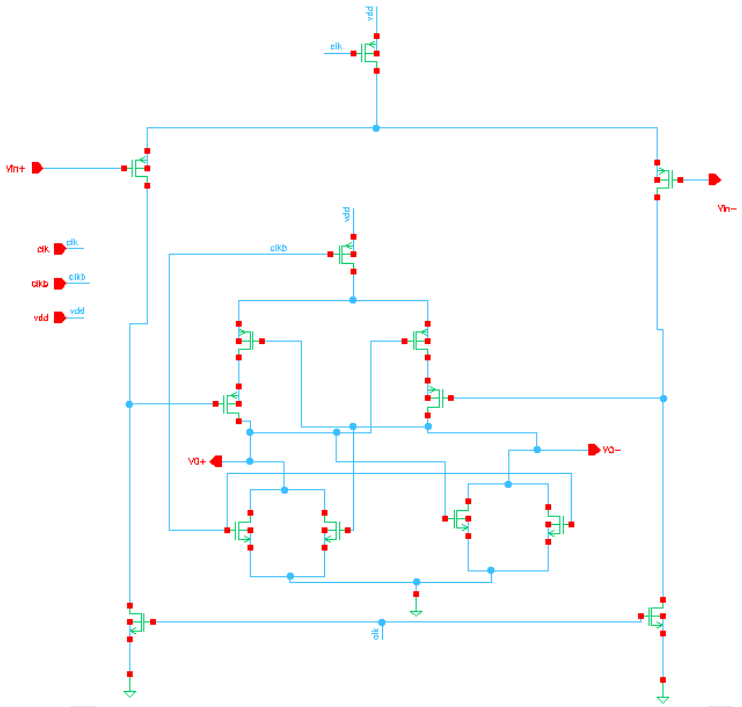

Fig. 4. Schematic of the dynamic latch comparator.

Figure 5 plots the resulting waveforms: the outputs swing in complementary fashion each time the clock triggers an evaluation, and the regenerative snap visible in the traces confirms the latch is making a clean differential decision. The comparator's average simulated power is 265.8 nW.

Fig. 5. Transient response of the dynamic latch comparator (Vin+, Vin-, Clk, Clkb, Vout).

C. 16-bit Bridge-Capacitor CDAC

The CDAC produces the trial voltage that each SAR decision is compared against. It is built from binary-weighted capacitor sections, each terminal switched to either the reference voltage or ground by a CMOS switch cell under the control of the SAR logic. Driving the PMOS and NMOS devices in each cell with complementary signals keeps charge injection and clock feedthrough from corrupting the switching operation.

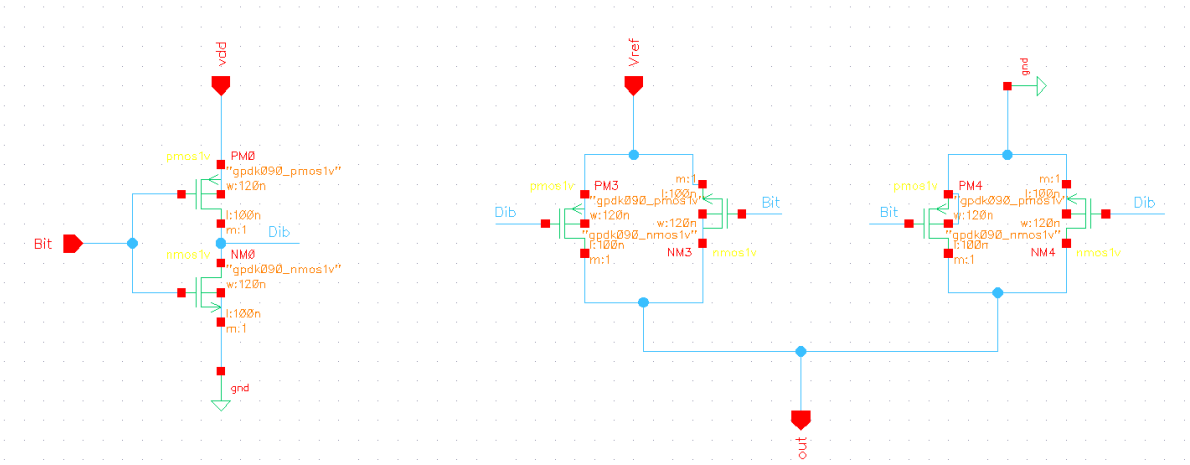

Fig. 6. Unit switch cell used in the 16-bit bridge-capacitor CDAC.

Rather than a single 16-bit binary-weighted array, the CDAC is split into two 8-bit banks MSB and LSB joined by a scaling bridge capacitor, as shown in Figure 7. This split keeps the total capacitance, and area, far below what a conventional 16-bit array would need, at the cost of having to size the bridge capacitor precisely enough to preserve the intended DAC transfer characteristics.

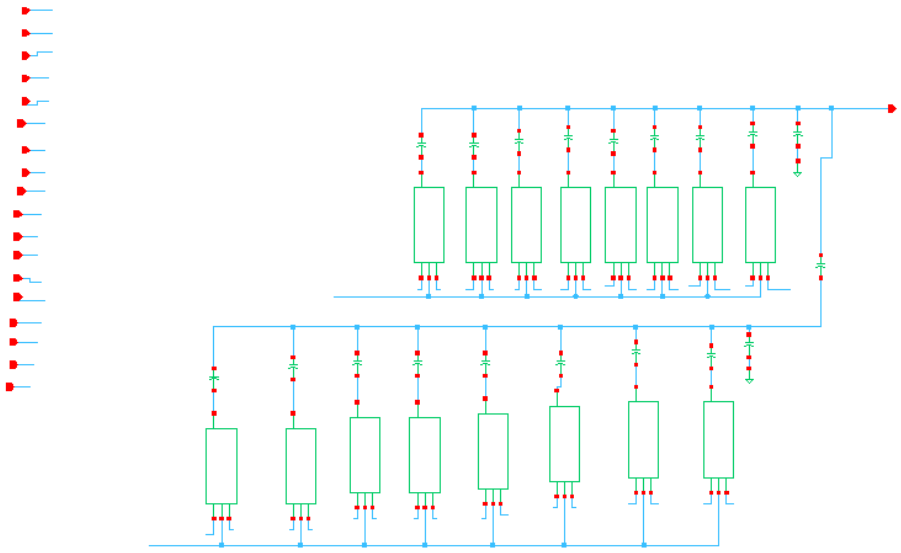

Fig. 7. Schematic of the 16-bit bridge-capacitor CDAC array.

D. SAR Control Logic

Conversion proceeds as a chain of 16 binary decisions. A reset clears the internal code register and starts the sequence at the MSB; on each subsequent clock edge, the comparator's output decides whether the bit under test stays set or is cleared, and control then moves to the next lower bit. Once all positions from D15 down to D0 have been decided, the controller raises an end-of-conversion flag and resets itself for the next cycle.

Algorithm 1. SAR successive-approximation control logic.

```
Algorithm SAR_Control_Logic
1. Initialize:
  code[i] <- 0 for i = 0 to 15
  bit_idx <- 15 ;  phase <- 0
2. On RESET (RST asserted):
  code[i] <- 0 for i = 0 to 15
  bit_idx <- 15 ;  phase <- 0
3. On every rising edge of CLK, if RST is not active:
  switch (phase):
   case 0 (Sampling phase):
     code[15] <- 1 ; bit_idx <- 15 ; phase <- 1
   case 1 (Bit-cycling / comparison phase):
     if (OUTP > OUTN): code[bit_idx] <- 1
     else:          code[bit_idx] <- 0
     if (bit_idx > 0): bit_idx <- bit_idx - 1 ;
                  code[bit_idx] <- 1
     else: phase <- 2
   case 2 (End of conversion):
     code[i] <- 0 for i = 0 to 15
     bit_idx <- 15 ; phase <- 0
4. Continuous output assignment:
  SAMPLE <- VDD if phase = 0 else 0
  EOC    <- VDD if phase = 2 else 0
  D[i]   <- VDD if code[i] = 1 else 0,  i = 0..15
End Algorithm
```

E. Complete 16-bit SAR ADC

Wiring the sampler, comparator, CDAC, and controller into a closed loop gives the complete converter. Once the input is sampled onto the CDAC, the controller works through the bits starting at D15: for each one, the CDAC sets a trial voltage, the comparator judges it against the sampled input, and the controller latches that decision into the corresponding output bit before moving to the next position. After sixteen such rounds, the resulting word $D[15:0]$represents the converted input.

IV. SIMULATION RESULTS AND DISCUSSION

The complete converter was simulated at the transistor level in Cadence Virtuoso, using the GPDK090 process and a 1.2-V supply. Figure 8 gives the transient response across a 20-µs window: once the sampling and clock signals trigger a conversion, the internal SAR nodes step through their decisions one after another, moving from the MSB toward the LSB exactly the bit-cycling pattern the design is meant to produce.

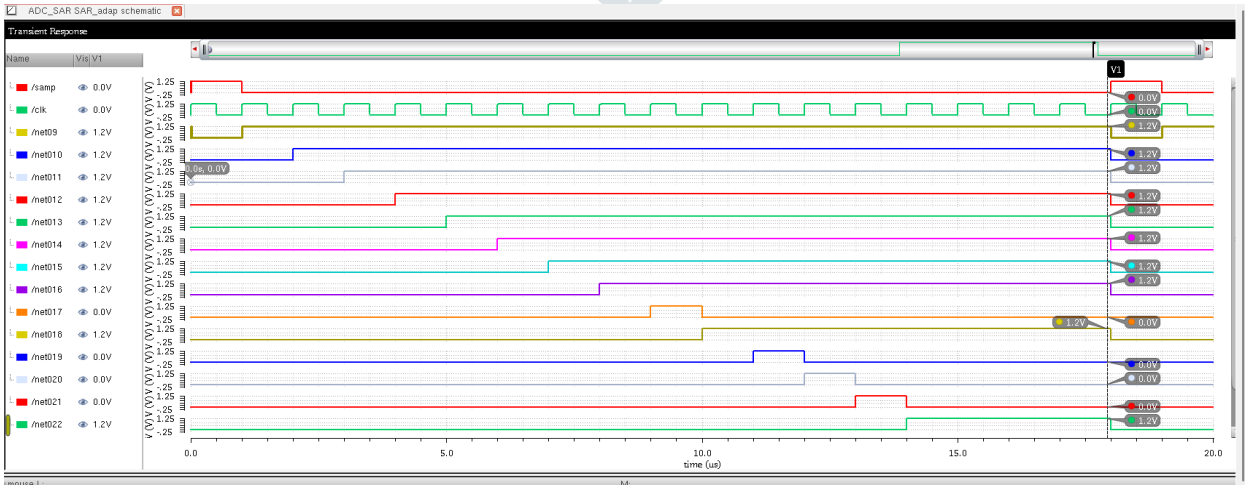

Fig. 8. Transient response of the complete 16-bit SAR ADC.

Table I summarizes the average power consumption of the individual sub-blocks and of the complete ADC.

Table I: Power consumption of the designed sub-blocks.

Block	Average Power
Bootstrapped sampling switch	295.4 nW
Dynamic latch comparator	265.8 nW
Complete 16-bit SAR ADC	460.9 µW

These simulated power figures are gathered in Table I. Both the bootstrapped switch and the comparator stay well below 1 µW on their own 295.4 nW and 265.8 nW respectively, but the complete ADC's 460.9-µW figure is much higher because it also captures the CDAC switching activity, SAR control circuitry, and the output-bit transitions that occur throughout a conversion.

Table II summarizes the comparison of the designed system to the previously discussed work done by other researchers.

Table II. Comparison of the proposed design with reference works.

Parameter	Proposed Design	Ding et al. [1]	Lakkannavar et al. [2]
Technology	90 nm	180 nm	90 nm
Resolution	16 bit	16 bit	8 bit
Supply Voltage	1.2 V	1.8 V	0.9 V
CDAC Architecture	Bridge capacitor (8+8)	Binary, non-bridge, custom 0.5-fF cap	Binary-weighted, 9 unit caps
Comparator Power	265.8 nW	Included in 6.34 mW total	0.2856 mW

Table II lines the proposed design up against [1] and [2]. It reaches 16-bit resolution in 90 nm with a bridge-capacitor CDAC, compared with [1]'s 180-nm process, which adds mismatch calibration, and [2]'s 8-bit, 90-nm implementation. Because the present design has no mismatch self-calibration, adding one is a natural next step for cutting down CDAC nonlinearity in future work.

V. CONCLUSION

This paper has presented a 16-bit SAR ADC, designed and functionally verified at the transistor level in Cadence Virtuoso on the 90-nm GPDK090 CMOS process. It combines a precharged bootstrapped sampling switch, a two-stage dynamic-latch comparator, a 16-bit bridge-capacitor CDAC, and a purpose-built SAR controller. Transient simulations show the sampler tracking correctly, the comparator regenerating cleanly, and the conversion proceeding in order from MSB to LSB. At 1.2 V, the switch and comparator average 295.4 nW and 265.8 nW individually, with the whole ADC drawing 460.9 µW results that confirm the architecture behaves as intended under simulation. Adding capacitor-mismatch calibration, running a full linearity characterization, and verifying the design post-layout are natural next steps for further evaluating the 16-bit converter.

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