JETIR.ORG ISSN: 2349-5162 | ESTD Year : 2014 | Monthly Issue
JOURNAL OF EMERGING TECHNOLOGIES AND INNOVATIVE RESEARCH (JETIR)
An International Scholarly Open Access, Peer-reviewed, Refereed Journal

DESIGN AND PERFORMANCE ANALYSIS OF AN OPTIMIZED ASPECT-RATIO 6T SRAM WITH SLEEP-TRANSISTOR BASED POWER GATING FOR STANDBY LEAKAGE POWER REDUCTION

[1]Chittidi Haritha Sai Lakshmi Annapurna, [2]Hari Krishna Kanneboina, [3]Avala Mallikarjuna Prasad

[1]PG Scholar, [2]Assistant Professor, [3]Professor

[1,2,3]Department of Electronics and Communication Engineering

[1,2,3]Jawaharlal Nehru Technological University, Kakinada, Andhra Pradesh, India

Abstract : As CMOS technology moves deeper into the sub-micron regime, SRAM the memory type that dominates on-chip storage in most System-on-Chip designs spends an increasing share of its power budget on standby leakage rather than active switching. This work takes an existing aspect-ratio-optimized 6T SRAM bit-cell, previously designed in 45 nm CMOS (GPDK045) at 1.2 V for a favourable combination of speed and leakage, and augments it with a single footer NMOS transistor placed between the cell's ground terminal and the true ground rail so the array can be power-gated during idle periods. Sized at a 600 nm width and a 45 nm channel length, this sleep device is turned fully ON whenever the cell is read or written and turned OFF once it returns to standby, breaking the sub-threshold leakage path while leaving the stored data node undisturbed. The complete cell, with and without the sleep transistor, was built and simulated in Cadence Virtuoso (GPDK045 nm) and characterized using both transient testing and 1000-run Monte Carlo analysis. Standby leakage power drops from 108.685 pW for the un-gated baseline to 20.9247 pW with the footer transistor in place, an approximately 80.7 % reduction, and this saving comes at almost no cost to active-mode behaviour: Write-1 delay actually improves, from 41.7843 ps to 36.4542 ps (12.8 % faster), write power falls from 6.9424 µW to 4.7611 µW (31.4 % lower), and Read-0/Read-1 delay together with read power shift by under 3.4 %. Taken together, these numbers indicate that a single, correctly sized footer sleep transistor is an inexpensive and effective way to cut SRAM standby leakage without sacrificing the speed or stability gained from aspect-ratio sizing.

Index Terms **-** 6T SRAM, leakage power, power gating, sleep transistor, low-power VLSI, Monte Carlo analysis, 45 nm CMOS.

I. INTRODUCTION

Wearable electronics, space-grade circuits, implantable medical devices and portable gadgets have all pushed energy efficiency to the top of the SoC design agenda [2]–[6]. Because SRAM typically occupies a large share of chip area and is instantiated thousands of times within a cache array, even a small per-cell leakage current multiplies into a sizeable fraction of overall chip power, an effect that is most pronounced while the memory sits idle between accesses. Shrinking supply voltages and transistor geometries make this worse, since sub-threshold leakage rises exponentially even as dynamic power falls meaning a cell optimized purely for speed and stability, with no attention paid to standby leakage, still leaves considerable power savings on the table.

Reference [1] recently proposed an iterative width-search algorithm for jointly sizing the pull-up, pull-down, access and peripheral (precharge/write-driver) transistors of a 6T SRAM cell, arriving at a 45 nm design with sub-picosecond read/write latency and leakage already lower than a conventionally sized cell. Standby power gating disconnecting the array from the supply or ground rail whenever it is idle attacks the same leakage problem from a different, largely independent angle, and can suppress leakage far more aggressively than sizing alone, without disturbing the transistor ratios that [1] tuned in the baseline design [7].

This paper builds on the aspect-ratio-optimized 6T SRAM cell of [1] by inserting one footer NMOS sleep transistor into the ground path of the memory cell. Fabricated at the same 45 nm node as the rest of the design and sized with a 600 nm width, this transistor is switched fully ON during active operation and fully OFF during standby under the control of a sleep-enable signal. Because the sleep device sits only in the shared ground-return branch, outside the cross-coupled inverter loop, it leaves the pull-up/pull-down/access ratio of the baseline design untouched, so read and write behaviour is preserved even as the leakage path is cut whenever the cell goes idle. The resulting design is validated in Cadence Virtuoso on the GPDK045 nm process through transient simulation and 1000-run Monte Carlo runs covering delay, average power and leakage power, and is benchmarked directly against the un-gated baseline.

The rest of the paper proceeds as follows. Section II surveys prior work on SRAM sizing and leakage suppression. Section III describes the baseline aspect-ratio-optimized 6T SRAM cell used as the starting point here. Section IV details the proposed footer sleep-transistor scheme. Section V lays out the simulation setup, and Section VI reports and interprets the results against the baseline. Section VII closes the paper, and Section VIII sketches directions for future work.

II. RELATED WORK

The SRAM design literature has approached the speed–stability–power trade-off from several complementary angles. One line of work formulates an algorithmic aspect-ratio estimation procedure that sizes the pull-up, pull-down, access and peripheral transistors of a 6T cell to jointly raise speed and leakage performance, validated through Cadence and Monte Carlo simulation [1]; however, that optimization targets a single design point and technology node, and does not pursue leakage reduction any further once the sizing itself is fixed.

A second line of work looks at leakage-reduction circuit techniques multi-threshold CMOS and power gating chief among them and reports substantial leakage savings in scaled SRAM arrays [6], [7], but usually in isolation from the sizing choices made elsewhere in the design, so the two aspects are seldom optimized jointly. A third strand documents growing leakage and variability as SRAM scales into deep sub-micron nodes without offering a specific remedy [3], [5]. Finally, statistical analyses of sub-threshold leakage current show it to be strongly sensitive to process and mismatch variation, which is why Monte Carlo-based validation is essential for any proposed leakage-reduction scheme [4].

Read together, this body of work suggests two things: transistor sizing alone can improve speed and, to a degree, leakage; and power gating remains a separate, well-established route to suppressing standby leakage more aggressively. The present work merges the two — it keeps the sizing methodology and transistor dimensions of [1] as the baseline, and adds a footer sleep-transistor power-gating stage aimed specifically at standby leakage, while confirming through simulation that the speed and power benefits of the original sizing survive the addition.

III. BASELINE ASPECT-RATIO-OPTIMIZED 6T SRAM

The baseline used throughout this work is the 45 nm, 1.2 V aspect-ratio-optimized 6T SRAM cell of [1], made up of three blocks: a precharge circuit that pulls the bit-line pair (BL, BLB) to VDD before each read, a write-driver circuit that forces the desired logic levels onto BL/BLB during a write, and the 6T cell itself two cross-coupled inverters (pull-up PMOS, pull-down NMOS) plus two NMOS access transistors switched by the word line. Its access (pass) transistors are intentionally made stronger than the pull-up devices to guarantee write-ability, while the precharge circuit's PMOS devices are kept near the minimum allowable width so they interfere as little as possible with the pull-down path and keep area and power low. The device dimensions that the sizing algorithm of [1] produced, reused unchanged here, are listed in Table I.

TABLE I. Transistor sizing of the baseline 6T SRAM adopted from [1] (45 nm technology).

MOSFET	Width (nm)	Length (nm)
NM1	720	45
NM2	720	45
NM3	920	45
NM4	920	45
NM5	910	45
NM6	910	45
NM7	910	45
NM8	910	45
PM1	120	45
PM2	120	45
PM3	120	45
PM4	120	45
PM5	120	45

With this sizing, [1] reports read access times of 11.17 ps / 9.97 ps (HIGH/LOW), write access times of 12.00 ps / 17.00 ps (HIGH/LOW), and a bare-cell leakage power of 1.64 pW. Once the precharge and write-driver circuitry is added, replicated and re-simulated here in the GPDK045 nm kit, the full non-gated design shows Read-0/Read-1 delays of 5.3636 ps / 5.6605 ps, Write-0/Write-1 delays of 17.6393 ps / 41.7843 ps, read/write power of 3.5637 µW / 6.9424 µW, and standby leakage of 108.685 pW; these numbers make up the “existing design” column used for comparison in Section VI. Device-level leakage-current studies such as [10] help frame the sub-threshold and junction leakage components discussed later in Section VI.

IV. PROPOSED FOOTER SLEEP-TRANSISTOR POWER GATING

In the baseline cell, standby leakage comes from sub-threshold conduction, gate-oxide tunneling and junction leakage acting together in the pull-up, pull-down and access devices, none of which switch off just because the memory is idle. Resizing these devices would upset the delay properties already tuned in [1], so instead this work cuts the leakage path directly: a single footer

NMOS transistor, SLEEP, is inserted between the cell's shared ground node (and, where the write driver shares that return, its ground connection too) and the true ground rail, as shown in Fig. 1. A sleep-enable signal drives the gate of SLEEP HIGH during active operation, so the device is fully ON and offers a low-resistance path to ground for normal reads and writes, and LOW during standby, so the device turns OFF and inserts a large sub-threshold resistance in series with the leakage path, collapsing leakage current by orders of magnitude.

Choosing the size of MSLEEP means balancing two opposing effects: a wider transistor lowers ON-state resistance, and with it the delay and IR-drop penalty during active operation, while a narrower transistor raises OFF-state resistance and therefore leakage suppression, at the expense of a bigger virtual-ground bounce and marginally slower access while the device turns on. Here, a 600 nm width with a 45 nm channel length matching the rest of the cell's technology node was chosen because it keeps ON resistance low enough that gated-cell read/write delay stays within a few percent of the ungated baseline, while its OFF resistance is still large enough to cut standby leakage by roughly fivefold, as Section VI shows.

Placing SLEEP in the single shared ground-return path, rather than duplicating it inside every pull-down branch, means only one extra transistor is needed per cell, so area and layout overhead stay minimal. Storage nodes Q and Q′ and the cross-coupled inverter ratios are untouched, so the sizing benefits already gained through aspect-ratio optimization in [1] should carry through to the gated design's active mode. Footer/header power gating is, of course, only one of several knobs used in the literature to trade speed, voltage margin and power scaled SRAM examples include self-collapsing write-assist circuits [11], read/write assist in tri-gate technology [12], dual write-driver-assist schemes for 7 nm FinFET SRAM [13], and pulsed PMOS trip-voltage-collapse schemes for 10 nm FinFET SRAM [14] but these all target active-mode margin rather than standby leakage, so the footer sleep-transistor approach proposed here could in principle be layered on top of any of them for a more aggressive low-power design. The single aspect ratio (W/L) = 600 nm / 45 nm for SLEEP.

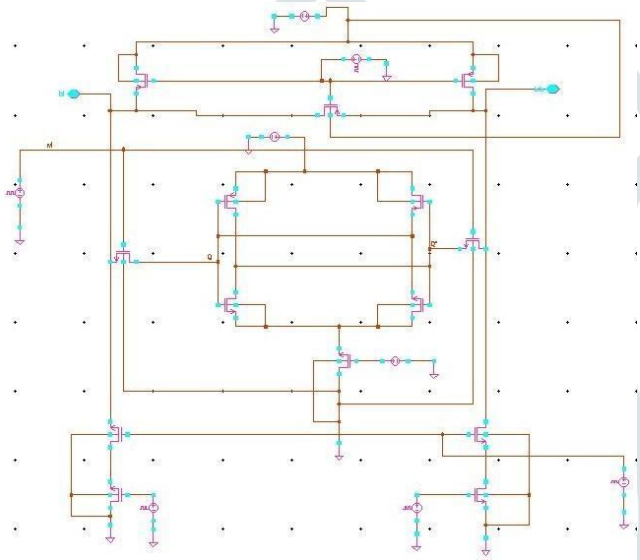

Fig. 1. Proposed 6T SRAM cell with footer NMOS sleep-transistor

V. SIMULATION METHODOLOGY

Both the baseline and proposed circuits were built and simulated in Cadence Virtuoso on the GPDK045 nm process design kit at a 1.2 V supply, matching the technology and bias point used in [1]. Transient simulations applied stimuli to the input, input′, write_sig and wl pins while monitoring the bit-line pair (bl, blb) and the internal storage nodes, confirming correct write-1, write-0, read-1, read-0 and hold behaviour once the sleep transistor was inserted into the ground path.

Simulations were run inside the Cadence Analog Design Environment (ADE-L) using the Spectre simulator with the BSIM device models from the GPDK045 nm PDK, at the typical-typical (TT) corner and 27 °C ambient the same corner used to characterize the baseline in [1]. Write-1/Write-0 and Read-1/Read-0 test vectors were built from piecewise-linear (VPWL) sources with 50 ps rise/fall edges on the input, input′, write_sig and wl pins, with enough settling time between operations that each access could be measured on its own. SLEEP's sleep-enable signal was held HIGH throughout the active-mode test benches (transient, delay, power) and pulled LOW in a separate standby test bench, so active and standby behaviour were each characterized with purpose-built benches rather than inferred from one combined run.

Manufacturing robustness was checked with 1000-run Monte Carlo simulations combining global process variation with local mismatch, covering four quantities Read-0/Read-1 delay, Write-0/Write-1 delay, average read/write power, and standby leakage power using the same statistical-validation approach applied to the baseline in [1]. Mean and standard deviation are reported for each quantity, and the means feed into the head-to-head comparison in Section VI.

Delay is measured as the interval between the 50 % VDD crossing of the relevant control edge (wl or write_sig) and the 50 % VDD crossing of the corresponding bit-line or storage-node response; read and write power come from integrating instantaneous supply current over the access window and dividing by its duration. Standby leakage power is obtained by holding the cell in the hold state (wl LOW, SLEEP OFF) and time-averaging supply voltage times steady-state supply current once transients have settled, so the reported value captures the combined sub-threshold, gate-oxide and junction leakage of the cell together with its precharge and write-driver circuits, not any single leakage mechanism in isolation. The 1000-run Monte Carlo analyses applied global and local mismatch variation to every transistor, SLEEP included, using the GPDK045 nm PDK's statistical models; a small number of runs that failed to converge to a valid measurement were dropped from the statistics, which is why the sample counts reported for individual metrics in Section VI fall a little short of 1000.

VI. RESULTS AND DISCUSSION

A. Transient Response

Fig. 2 plots the transient behaviour of the gated SRAM through successive write and read cycles. Each access is enabled by a HIGH pulse on the word line (wl); the internal nodes Q and Q′ latch the correct complementary values driven by the write driver, and the bit lines bl and blb settle to their expected precharged or discharged levels during reads. The extra nodes that make up the sleep-transistor bias network track the sleep-enable signal correctly throughout, showing that gating the ground path with SLEEP does not interfere with read or write functionality while the sleep transistor is held ON for active access.

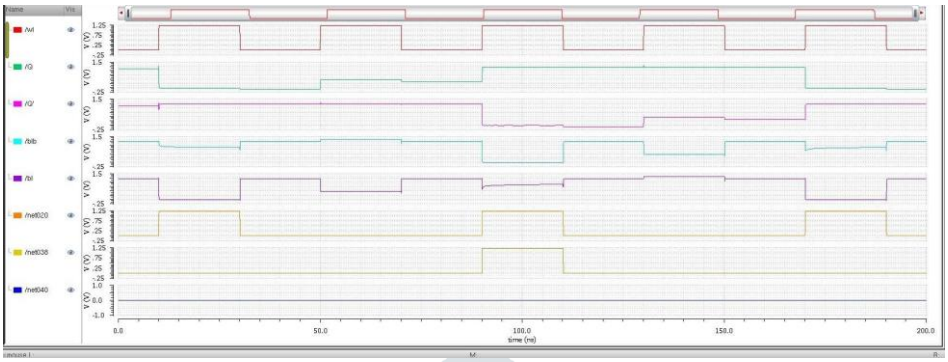

Fig. 2. Transient response of the proposed SRAM

B. Monte Carlo Delay Analysis

Figs. 3–6 represent the 1000-run Monte Carlo spread of Read-0, Read-1, Write-0 and Write-1 delay for the proposed design, with means of 5.5432 ps, 5.4630 ps, 16.9741 ps and 36.4542 ps respectively; each standard deviation is a small fraction of its mean (Table III), showing that adding the footer sleep transistor does not make delay unusually sensitive to process or mismatch variation. Write delay remains longer than read delay, as in the baseline, since a write must overpower both the access transistor and, where relevant, the precharge device, whereas read delay is set mainly by how quickly a small bit-line differential can be sensed.

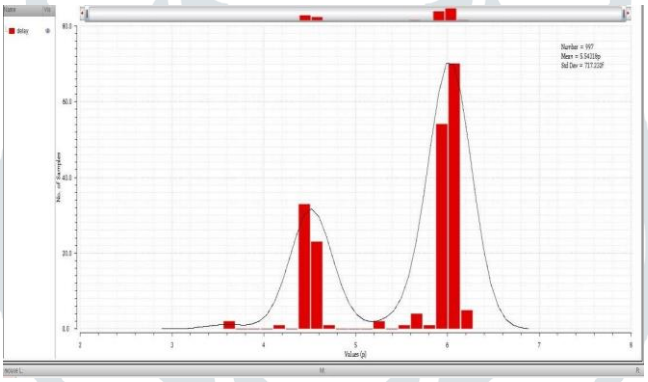

Fig. 3. Read-0 delay for the proposed SRAM.

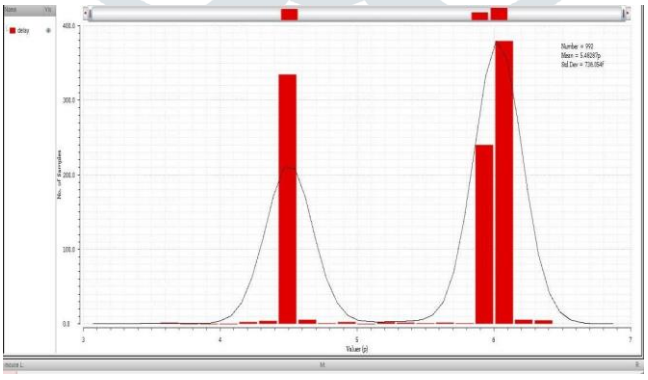

Fig. 4. Read-1 delay for the proposed SRAM.

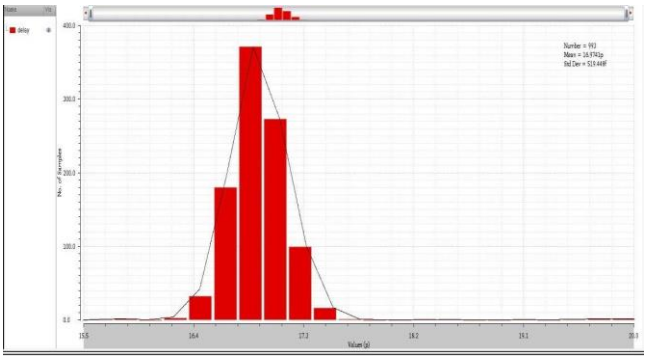

Fig. 5. Write-0 delay for the proposed SRAM.

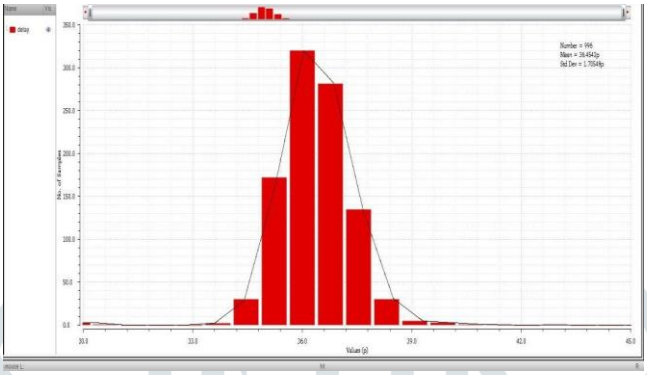

Fig. 6. Write-1 delay for the proposed SRAM.

C. Monte Carlo Average Power Analysis

Figs. 7 and 8 show the Monte Carlo spread of average read and write power for the proposed design, with means of 3.671 µW and 4.7611 µW respectively. Write power falls noticeably relative to the existing design because SLEEP, being fully ON during the write, contributes negligible series resistance, while the ground-referenced leakage that used to run continuously is now suppressed the moment the cell returns to standby after the operation finishes.

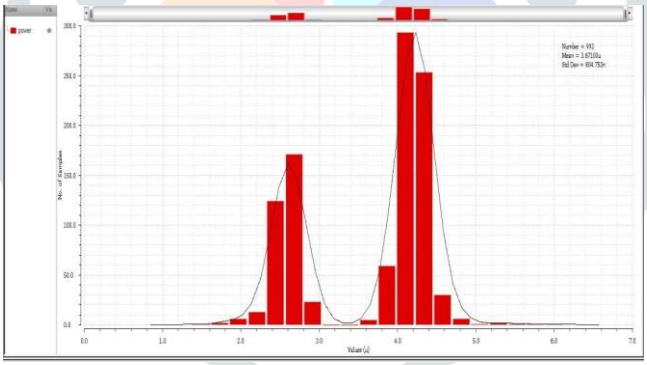

Fig. 7. Average read power for the proposed SRAM.

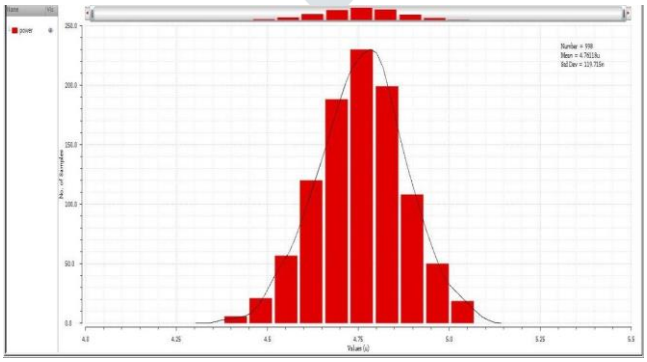

Fig. 8. Average write power for the proposed SRAM.

D. Leakage Power Analysis

Fig. 9 gives the Monte Carlo distribution of standby leakage power for the gated design, with a mean of 20.9247 pW and a standard deviation of 2.5953 pW across 996 valid runs roughly an 80.7 % drop from the 108.685 pW measured for the non-gated baseline under identical conditions, confirming that switching the footer NMOS OFF during standby is highly effective at shutting down the combined sub-threshold, gate and junction leakage of the cell, precharge and write-driver circuits.

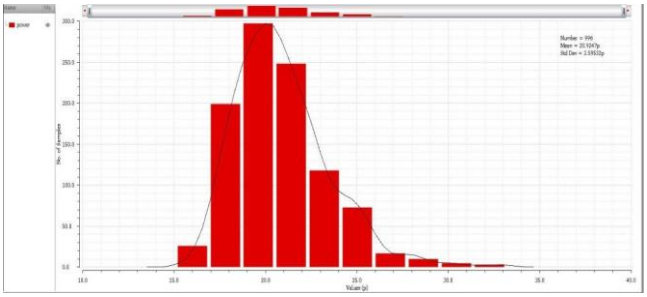

Fig. 9. Standby leakage power for the proposed SRAM design.

TABLE III. Monte Carlo (1000-run) summary for the proposed design.

Parameter	Mean	Std Dev
Read-0 delay	5.5432 p	717.2 f
Read-1 delay	5.4630 p	736.2 f
Write-0 delay	16.9741 p	513.4 f
Write-1 delay	36.4542 p	1.7155 p
Read power	3.6710 µ	804.8 n
Write power	4.7612 µ	119.7 n
Leakage power	20.9247 p	2.5953 p

E. Comparison with the Existing Design

Table IV lines up the proposed footer sleep-transistor design against the existing aspect-ratio-optimized baseline under matched simulation conditions. The headline result is an 80.75 % cut in standby leakage power (108.685 pW → 20.9247 pW). Active-mode metrics hold up well or even improve: Write-1 delay falls 12.76 % and write power falls 31.41 %, both because SLEEP, fully ON during writes, adds almost no series resistance while cutting off leakage between accesses; Write-0 and Read-1 delay drop slightly (−3.77 % and −3.14 %); Read-0 delay and read power rise only marginally (+3.35 % and +3.01 %), a modest and acceptable cost from the extra ON resistance and parasitic capacitance the footer device adds to the read discharge path. In short, a single well-sized footer sleep transistor delivers a large standby-leakage saving for only a few percent of change in active-mode delay and power, leaving the baseline's transistor sizing intact.

TABLE IV. Performance comparison between the existing design [1] and the proposed design.

Parameter	Existing [1]	Proposed	Δ (%)
Read-0 Delay (ps)	5.3636	5.5431	+3.35
Read-1 Delay (ps)	5.6605	5.4828	−3.14
Write-0 Delay (ps)	17.6393	16.9741	−3.77
Write-1 Delay (ps)	41.7843	36.4542	−12.76
Read Power (µW)	3.5637	3.6710	+3.01
Write Power (µW)	6.9424	4.7611	−31.41
Leakage Power (pW)	108.685	20.9247	−80.75

VII. CONCLUSION

This work added a footer NMOS sleep-transistor power-gating stage 600 nm wide, 45 nm channel length to an aspect-ratio-optimized 6T SRAM cell built in 45 nm CMOS at 1.2 V. Transient and 1000-run Monte Carlo simulation in Cadence Virtuoso (GPDK045 nm) show standby leakage power falling from 108.685 pW to 20.9247 pW, roughly an 80.7 % reduction, while read/write delay and active-mode power stay within a few percent of the non-gated design and in some cases (Write-1 delay, write power) actually improve. Footer sleep-transistor power gating therefore proves to be a simple, low-area-overhead complement to aspect-ratio-based sizing, well suited to building low-leakage, fast, stable SRAM for battery-powered, wearable and space-constrained SoCs.

VIII. FUTURE SCOPE

This study covers delay, average power and leakage power only; characterizing the data-retention behaviour of the gated cell particularly its retention voltage while SLEEP is OFF is a natural next step. Multi-threshold CMOS (MTCMOS) devices could be substituted for the sleep transistor to push leakage suppression further, and an adaptively or dynamically controlled sleep signal could help balance wake-up latency against leakage savings across varying workloads. Scaling the design and its power-gating

scheme up to a full cache array for AI, IoT and other low-power portable applications would also help quantify the benefit at the system level.

REFERENCES

[1] S. M. Mantrashetti, A. P. Chavan, P. Pawar, H. V. R. Aradhya, and O. S. Powar, "A Novel Algorithm for Aspect Ratio Estimation in SRAM Design to Achieve High SNM, High Speed, and Low Leakage Power," IEEE Access, vol. 13, pp. 9942–9954, 2025, doi: 10.1109/ACCESS.2025.3527333.

[2] B. Ebrahimi, M. Rostami, A. Afzali-Kusha, and M. Pedram, "Statistical design optimization of FinFET SRAM using back-gate voltage," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 19, no. 10, pp. 1911–1916, Oct. 2011.

[3] J. Kwon, I. J. Chang, I. Lee, H. Park, and J. Park, "Heterogeneous SRAM cell sizing for low-power H.264 applications," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 59, no. 10, pp. 2275–2284, Oct. 2012.

[4] J. P. Kulkarni and K. Roy, "Ultralow-voltage process-variation-tolerant Schmitt-trigger-based SRAM design," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 20, no. 2, pp. 319–332, Feb. 2012.

[5] R. Rao, A. Srivastava, D. Blaauw, and D. Sylvester, "Statistical analysis of subthreshold leakage current for VLSI circuits," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 12, no. 2, pp. 131–139, Feb. 2004.

[6] S. K. Gupta, A. Raychowdhury, and K. Roy, "Digital computation in subthreshold region for ultralow-power operation: A device–circuit–architecture co-design perspective," Proc. IEEE, vol. 98, no. 2, pp. 160–190, Feb. 2010.

[7] H. Jiao and V. Kursun, "Power gated SRAM circuits with data retention capability and high immunity to noise: A comparison for reliability in low leakage sleep mode," in Proc. Int. SoC Design Conf., Seoul, South Korea, Nov. 2010, pp. 5–8.

[8] A. Yan, Y. Chen, Y. Hu, J. Zhou, T. Ni, J. Cui, P. Girard, and X. Wen, "Novel speed-and-power-optimized SRAM cell designs with enhanced self-recoverability from single- and double-node upsets," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 67, no. 12, pp. 4684–4695, Dec. 2020.

[9] V. Gupta and M. Anis, "Statistical design of the 6T SRAM bit cell," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 57, no. 1, pp. 93–104, Jan. 2010.

[10] A. Islam and M. Hasan, "Leakage characterization of 10T SRAM cell," IEEE Trans. Electron Devices, vol. 59, no. 3, pp. 631–638, Mar. 2012.

[11] K. Cho, J. Park, K. Kim, T. W. Oh, and S.-O. Jung, "SRAM write assist circuit using cell supply voltage self-collapse with bit-line charge sharing for near-threshold operation," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 69, no. 3, pp. 1567–1571, Mar. 2022.

[12] E. Karl, Y. Wang, Y.-G. Ng, Z. Guo, F. Hamzaoglu, M. Meterelliyoz, J. Keane, U. Bhattacharya, K. Zhang, K. Mistry, and M. Bohr, "A 4.6 GHz 162 Mb SRAM design in 22 nm tri-gate CMOS technology with integrated read and write assist circuitry," IEEE J. Solid-State Circuits, vol. 48, no. 1, pp. 150–158, Jan. 2013.

[13] T. Song, J. Jung, W. Rim, H. Kim, Y. Kim, C. Park, J. Do, S. Park, S. Cho, H. Jung, B. Kwon, H.-S. Choi, J. Choi, and J. S. Yoon, "A 7 nm FinFET SRAM using EUV lithography with dual write-driver-assist circuitry for low-voltage applications," in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 2018, pp. 198–200.

[14] Z. Guo, D. Kim, S. Nalam, J. Wiedemer, X. Wang, and E. Karl, "A 23.6 Mb/mm² SRAM in 10 nm FinFET technology with pulsed PMOS TVC and stepped-WL for low-voltage applications," in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 2018, pp. 196–198.