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Design and Transient Analysis Of SAW Resonator-Based Oscillator Using BJT Featuring An Integrated 51.2dB Ripple Reduction Power Supply

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Abstract : Surface Acoustic Wave (SAW) resonators are mostly used in RF applications due to their compact physical structure, higher quality factor (greater than 12,000) compared to LC tanks and thus, we can get a better frequency-selectivity. Although they are a better option, their performance can be hindered by noise in the power supply causing supply-induced frequency pushing and amplitude-to-phase noise conversion. This study is done to design and simulate SAW resonator-based oscillators using low-noise and high frequency BJTs (BFR93A and BFP450) and the power supply and power supply filters which can help increase the performance of the oscillator. Here, the center nominal frequency of the oscillator is 315MHz and using Vanlong's SR315 and SQ315 resonators, we have created one-port and two-port oscillator circuits with the Equivalent Circuit Model for both resonators mentioned by Vanlong (Due to no available SAW resonators in NI Multisim simulation software).

To help prevent the RF signals from noise, a dedicated power supply and power supply filter are designed. The power supply is a DC-DC Synchronous Buck converter which converts 15V to 5V using TPS561208DDC integrated circuit (IC). This circuit is then cascaded with a third-order passive CLC -type low-pass filter (47µF – 180mH – 47µF) which is able to reduce switching voltage ripple and is able to compress input disturbances from 3.262 mV down to just 8.94 µV, thus, 51.2dB of voltage attenuation.

Altogether, this study tries to bring out an effective way for 315MHz signal generation with a special attention to noise suppression from the power supply side, which we found is studied less compared to other oscillator designs.

IndexTerms **- Surface Acoustic Wave (SAW) Resonator, 315 MHz Oscillator, One-Port Resonator, Two-Port Resonator, Bipolar Junction Transistor (BJT), Equivalent Circuit Model (ECM), Synchronous Buck Converter, -Type Low-Pass Filter, Power Supply Ripple Rejection, Phase Noise Mitigation.**

Introduction The Surface Acoustic Wave (SAW) resonator-based oscillators have become an important part of modern communication and high-frequency electronic systems due to their ability to provide high frequency stability, compact size, low phase noise, and improved signal quality [4], [6], [7]. These oscillators are widely used in wireless communication systems, RF transmitters and receivers, satellite communication, radar systems, sensor networks, and precision timing applications where accurate frequency generation is required [4], [6]. Among various oscillator configurations, the Pierce oscillator topology is commonly preferred because of its simple circuit structure, reliable operation, and compatibility with high-Q resonators such as SAW devices [10]. However, despite their advantages, practical SAW oscillators are affected by several limitations including phase noise, frequency drift, resonator losses, impedance mismatches, and power-supply-induced disturbances [1], [3], [11]. Variations in the power supply can alter the operating characteristics of the active device and introduce unwanted fluctuations that degrade oscillator performance through frequency pushing and amplitude-to-phase conversion effects [3], [11], [12]. Therefore, maintaining a stable and low-noise power supply becomes an important requirement for improving overall system performance [3]. The proposed work focuses on the design and analysis of a 100 MHz SAW oscillator using a BJT-based Pierce oscillator topology with emphasis on improving frequency stability and output signal quality [10], [11]. A power-supply noise reduction approach is incorporated through the use of a low-pass filtering technique to suppress unwanted noise and ripple components. The proposed system aims to reduce supply-induced disturbances and improve spectral purity while maintaining stable oscillator operation [3], [4]. The expected outcome of the work is a low-noise and highly stable oscillator suitable for RF and wireless communication applications [4], [6].

I. OSCILLATORS

2.1 Introduction

An oscillator is a steady AC waveform generator using DC power and a feedback system. It does not use any external input; instead, it uses internal circuit noise, such as flicker noise, thermal noise, etc. [1]. The output is sustained due to internal loop conditions [1]. Every oscillator satisfies 2 conditions for steady and sustained oscillations, which are called the necessary conditions of the Barkhausen criterion given by Heinrich Barkhausen [1], [2]. Barkhausen Criterion has the following 2 conditions –

1. The closed-loop gain, which is the product of the open-loop gain and the feedback factor of the amplifier used in the oscillator, should be unity for sustained oscillations [1], [2].

$$|A\beta|=1 \quad (1)$$

2. The total phase shift caused by the amplifier stage and the feedback stage should be equal to 0º or a multiple of 360º (2π).

$$\angle A\beta=0° \text{ or } n2\pi \text{ , } n \in Z \quad (2)$$

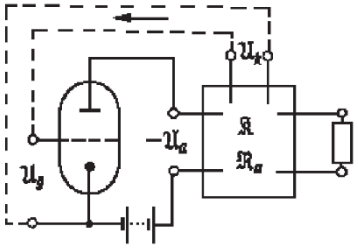

Bild 1. Allgemeines Schema einer Rückkopplung

(1) $\mathfrak{U}_a = -\mathfrak{V}\mathfrak{U}_g$; $\mathfrak{V} = -\frac{\mathfrak{U}_a}{\mathfrak{U}_g}$ = „*Verstärkungsfaktor*“

(2) $\mathfrak{R} = -\frac{\mathfrak{U}_k}{\mathfrak{U}_a}$ = „*Rückkopplungsfaktor*“

(3) $\mathfrak{R} = \frac{1}{\mathfrak{V}}$ oder $\mathfrak{R}\mathfrak{V} = 1$

(*Allgemeine Selbsterregungsformel.*)

Fig.1. Barkhausen’ s initial observations [2]

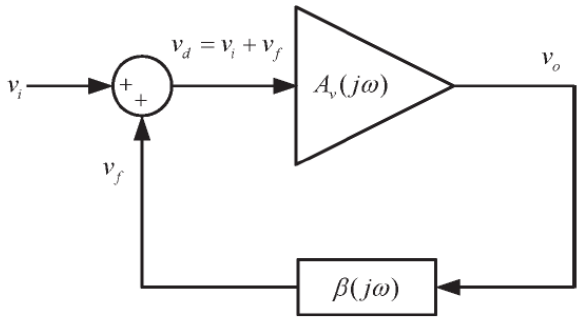

Fig.2. Basic feedback circuit [1]

3. SAW Resonator and Oscillator

Surface Acoustic Wave (SAW) resonator is a high-frequency passive device that uses mechanical resonance, that is, the resonance is achieved using the standing acoustic waves on the surface of a piezoelectric material [4]. This resonator is different from the others, like LC tank or crystal resonators, which use bulk vibrations [4]. The energy in SAW resonators is confined up to the depth of one wavelength of the substrate surface, as Rayleigh waves are the predominant mode of signal transmission [5]. Amplitude of Rayleigh waves decay exponentially as the wave moves into the bulk of the substrate, where the displacement components vary by an approximate formula,

$e^{-2\pi y/\lambda}$, where y is the depth[5]. (3)

The working principle of the SAW resonator is the inverse piezoelectric effect, where the electric signals are converted back into mechanical vibrations [4], [6]. The physical structure of a SAW resonator is fabricated on a thin piezoelectric substrate using photolithography, using which the metal electrodes, usually of gold or aluminum, are patterned [4], [6]. There are 3 main components IDTs, reflectors, and aperture, the first one being Interdigital Transducers (IDTs) that are the comb-shaped electrodes (with ‘fingers’) which determine the frequency of the SAW resonator. The center-to-center distance, which is called the pitch, is equal to $\frac{\lambda}{2}$, thus, it determines the wavelength (λ) of the SAW resonator, and therefore, its frequency [6]. When RF voltage is

applied to the IDTs, the periodic electric field causes the piezoelectric substrate to expand and contract [6]. This expansion and contraction cause Rayleigh waves [5], [6]. These waves travel along the surface until they hit the reflector gratings or Bragg mirrors [4], [6]. These reflectors are shorted or open-circuit metal strips that generally have a period of $\frac{\lambda}{2}$ to satisfy the Bragg condition [4], [6]. These reflect the signal back to the cavity [4], [6]. Standing waves are created only when these reflectors bounce the waves back and forth, and constructive interference occurs [4], [6]. The aperture here is the overlap length of IDT fingers [4], [6]. This influences the resonator's impedance and coupling strength [4], [6].

Frequency Determination:

Here, the resonant frequency is governed by the physical properties of IDTs and the properties of the substrate material [7]: $f_r = \frac{v}{\lambda}$ where, v is the phase velocity of the SAW in a specific material and λ is the wavelength defined by IDT finger spacing [7].

1 Port and 2 Port SAW resonator ECM

Most of the time, finding the correct SPICE model of a SAW resonator in a simulation environment is tough. To ease this, Equivalent Circuit Models (ECM) are devised. There are two types of SAW resonators based on the number of ports. A 1 Port SAW is where a single IDT acts as input and output too, and is placed in between 2 reflector gratings [7], [8]. So, it excites the acoustic wave and senses the reflected wave simultaneously [7], [8]. Thus, it acts like a passive two-terminal impedance [7], [8].

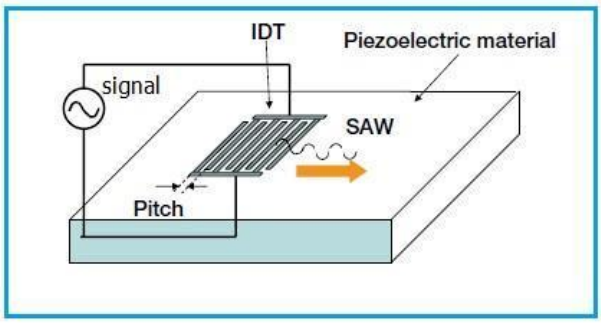

Fig.3. 1 Port SAW Resonator [8]

1 Port SAW ECM design considerations –

The electrical model for a 1-port SAW resonator is the Butterworth-Van Dyke (BVD) model, which has a static branch in parallel with the motional branch [7], [8]. The motional branch represents the mechanical resonance of the surface wave, where L (Motional Inductance) represents acoustic mass or inertia, C (Motional Capacitance) represents acoustic elasticity, and R (Motional Resistance) represents damping or acoustic and mechanical losses [7], [8]. The static branch represents parasitic or static capacitance C_o formed due to IDT electrodes [7], [8].

Resonant Frequency (f_r):

$$f_r = \frac{1}{2\pi\sqrt{LC}} = \frac{v}{\lambda} \quad (4)$$

Wavelength (λ):

$$\lambda = 2p \quad (5)$$

Static Capacitance (C_o):

$$C_o = N.W.C_{pair} \quad (6)$$

Where N is the number of finger pairs, W is the aperture and C_{pair} is the capacitance per finger pair unit.

Quality factor (Q_f): Is a dimensionless quantity which depicts the efficieny and sharpness of resonator as it's the ratio of peak energy stored to energy lost per cycle. A higher Q_f represents lower damping and narrower bandwidth (Δf) which is significant for oscillator stability and filter selectivity.

$$Q_f = \frac{2\pi f_r L}{R} = \frac{f_r}{\Delta f} \quad (7)$$

Motional Inductance (L):

$$L = \frac{Q_f R}{2\pi f_r} \quad (8)$$

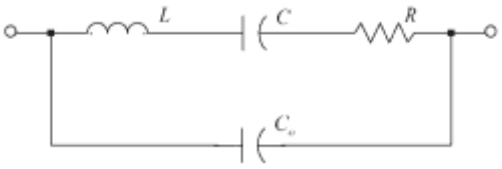

Fig.4. 1 Port SAW resonator ECM [1]

A 2 Port SAW uses two separate IDTs – one for input and the other one for output which are sandwiched between the two reflector gratings. The input IDT converts the electrical signal into mechanical wave, which resonates within the cavity formed by the gratings and is then picked up by the output IDT. Here the SAW resonator behaves like a transmission device or a very narrow band filter which is characterized by insertion loss and phase shift.

1 Port SAW is best suited for Colpitts oscillator and can be a bit nosy compared to 2 Port SAW [1]. Whereas, 2 Port SAW is best suited for Pierce oscillator and has better frequency stability and lower phase noise [1].

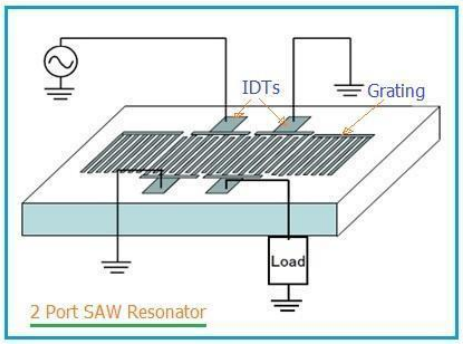

Fig.5. 2 Port SAW resonator [8]

2 Port SAW ECM design considerations –

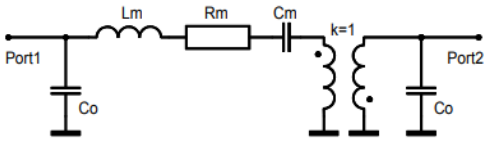

Fig.6. 2 Port SAW resonator ECM [10]

The concept is similar to 1-port SAW resonator but here there are two static capacitances and both will be equal if both IDTs are equal [10]. Here, an additional ideal transformer is added to represent the electromechanical energy conversion and provide 180º phase shift [10].

Resonant Frequency (f_r):

$$f_r = \frac{1}{2\pi\sqrt{LC}} = \frac{v}{\lambda} \quad (9)$$

Wavelength (λ):

$$\lambda = 2p \quad (10)$$

Static Capacitance (C_o):

$$C_o = N.W.\epsilon_0\epsilon_r \quad (11)$$

Where ϵ_0, ϵ_r are the permittivity constants of vacuum and substrate.

Motional Capacitance (C):

$$C = C_o.\frac{8k^2}{\pi^2} \quad (12)$$

Where k is the electromechanical coupling coefficient of the material.

Motional Inductance (L):

$$L = \frac{1}{(2\pi f_r)^2 C} \quad (13)$$

Quality Factor (Q_f):

$$Q_f = \frac{2\pi f_r L}{R} = \frac{1}{2\pi f_r CR} \quad (14)$$

The main advantages of using a SAW resonator over an LC tank or a quartz crystal is its HF range of oscillation, starting from 30MHz to several GHz, has greater frequency stability over time and varying environmental conditions, has a very high-quality factor and thus lower phase noise, and is very compact and lightweight as acoustic waves are 100000 times shorter than electromagnetic waves at the same frequency [1].

2.2 SAW Resonator-based Oscillator Using BJT

Research Gaps -

After reviewing numerous research papers, the following research gaps were identified: There is no specific 100 MHz SAW resonator-based oscillator with phase noise below -155 dBc/Hz at a 10kHz frequency offset. Most of the papers explain the impedance matching more than the actual circuit to be designed and made. Rarely have papers explained the power supply design for the oscillator with the oscillator design simultaneously.

Why BJT over MOSFET -

Here, the BJT is chosen over the MOSFET because it has superior phase noise performance due to lower flicker noise, which implies a much lower noise corner frequency and thus produces a cleaner signal with less jitter [11]. BJT has higher transconductance than comparable MOSFET for the same amount of bias current, thus this allows BJT to provide higher gain at higher frequencies, and also it is easier for the BJT to overcome insertion losses of the SAW resonator, ensuring reliable start-ups [11]. The parasitic capacitances of high-performance BJT are lower than those of a comparable MOSFET, which reduces the loading effect on the resonator and maintains a higher overall loaded Q factor [11].

Common Emitter (CE) configuration of BJT design

Basic formulae to design a CE amplifier at a specific frequency:

1. $V_{CEQ} = \frac{V_{CC}}{2}$ (15)
2. $I_C = \frac{V_{CC}}{10R_c}$ (16)
3. $P_Q = V_{CEQ}.I_C$ (17)
4. $I_E = I_B + I_C$ (18)
5. $I_C = \beta I_B$ (19)
6. $R_E = \frac{V_E}{I_E}$ (20)

7. $r_e = \frac{V_T}{I_E}$ (21)
8. $|A_V| = \frac{R_C || R_L}{r_e + R_{E1}}$ (22)
9. $V_{BE} = V_B - V_E$ (23)
10. $I_{div} = 10 I_B$ (24)
11. $R_1 + R_2 = \frac{V_{CC}}{I_{div}}$ (25)
12. $V_B = V_{CC} . \frac{R_2}{R_1 + R_2}$ (26)
13. $R_{in} = R_1 || R_2 || \beta (r_e + R_{E1})$ (27)
14. $C_{in} = \frac{1}{2\pi R_{in} f_L}$ (28)
15. $R_{out} = R_C || R_L$ (29)
16. $C_{out} = \frac{1}{2\pi R_{out} f_L}$ (30)
17. $R_E = R_{E1} + R_{E2}$ (31)
18. $C_E = \frac{1}{2\pi R_E f_L}$ (32)

II. Power Supply Filters

3.1 Introduction

Power-supply-induced noise is one of the significant factors affecting the performance of oscillator systems. Variations in supply voltage can introduce disturbances into the active device and resonator network, leading to frequency instability, increased phase noise, and degradation in output signal quality [3], [11]. Supply fluctuations may also produce frequency pushing and amplitude-to-phase conversion effects that adversely affect spectral purity [3]. Therefore, minimizing supply-induced disturbances becomes necessary for achieving stable and low-noise oscillator operation. To overcome these effects, a power supply filtering approach is incorporated into the proposed system.

3.2 Proposed Filter Design and Mathematical Analysis

To reduce unwanted ripple and noise components, a third-order π low-pass filter topology was selected due to its higher attenuation characteristics and improved suppression capability compared to lower-order filters. The proposed filter consists of two capacitors and one inductor arranged in a C-L-C configuration. The capacitors provide low impedance paths for AC noise components, while the inductor opposes rapid current variations and blocks unwanted disturbances. The cutoff frequency of the filter is determined by:

$f_c = 1/(2\pi\sqrt{(LC)})$

For the proposed design:

Input Voltage = 15 V

Output Voltage = 5 V

Injected noise signal = 10 mV AC

Target cutoff frequency = 50–60Hz. Selected component values:

C_1 = 100 µF

L = 100 mH

C_2 = 100 µF

The selected component values provide an approximate cutoff frequency of 55 Hz, allowing effective attenuation of unwanted supply disturbances while maintaining the required DC output.

3.3 Selection of Filter Topology

Different filter configurations provide different levels of attenuation and complexity [13]. First-order RC filters provide simple implementation but generally exhibit limited attenuation characteristics. LC filters improve selectivity and offer reduced power losses. However, higher-order π filters provide superior suppression performance because of their combined capacitive and inductive behavior [14].

The third-order π filter was selected for the proposed work because it provides improved attenuation of supply-induced disturbances while maintaining a relatively simple structure. The use of multiple reactive elements enhances filtering capability and improves voltage smoothening performance. This makes the π filter suitable for applications requiring stable and low-noise power supplies such as RF oscillator systems [13], [14].

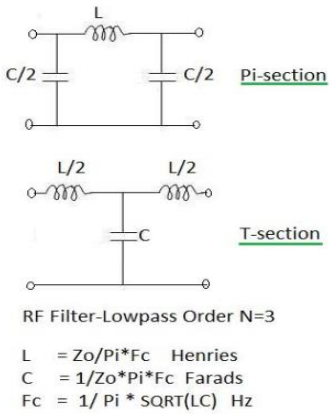

Fig.7. RF Low Pass Order of circuit is 3

This diagram illustrates commonly used passive low-pass filter configurations including π-section and T-section topologies. Among these configurations, the π filter structure was selected for the proposed work because it provides improved attenuation characteristics and better suppression of unwanted ripple components. The use of capacitive elements at both input and output stages along with an inductive element in the center improves filtering efficiency and enhances power-supply stability.

3.4 Circuit Implementation

The proposed power-supply noise reduction circuit is implemented using a third-order π low-pass filter configuration connected between the DC supply source and the oscillator circuitry. The primary objective of the filtering stage is to minimize unwanted AC ripple components and external disturbances before they reach the active oscillator components. Since supply fluctuations directly affect the operating point of transistors and other active elements, proper filtering becomes important for maintaining stable oscillator behavior.

The input to the proposed system consists of a 15V DC power source with an injected AC noise signal of approximately 10mV. This noise signal represents practical disturbances that may arise from switching devices, regulator circuits, electromagnetic interference, and external electronic components. If these disturbances are allowed to propagate directly into the oscillator circuitry, they can introduce amplitude fluctuations and frequency instability.

The third-order π filter consists of two capacitors and one inductor connected in a C-L-C configuration. The first capacitor, C_1, performs initial filtering by providing a low-impedance path for AC noise signals and diverting them toward ground. This process reduces the amount of unwanted disturbance entering the remaining circuit stages. The inductor L acts as the main filtering element and opposes sudden variations in current flow according to the principle of electromagnetic induction. Since the inductor presents higher impedance to AC components and lower impedance to DC components, ripple propagation through the circuit is significantly reduced. The second capacitor, C_2, performs secondary filtering by suppressing remaining disturbances and smoothing the voltage waveform.

After the filtering stage, a voltage regulator is introduced to convert the filtered 15V DC signal into a regulated 5V DC output suitable for oscillator operation. The voltage regulator maintains a stable output level even under minor supply variations and load fluctuations. The combined action of the π filter and voltage regulator creates a cleaner and more stable power source for the oscillator circuitry.

The selected component values for the proposed design are:
$C_1 = 100\mu F$
$L = 100mH$
$C_2 = 100\mu F$
Input Voltage = 15V
Output Voltage = 5V
Injected Noise Signal = 10mV AC
These component values are selected to achieve a cutoff frequency close to the desired operating range while providing efficient suppression of unwanted disturbances.

3.5 Expected Results and Performance Analysis

The performance of the proposed filtering technique is evaluated by analyzing the behavior of the supply signal before and after the implementation of the filtering stage. The primary objective is to determine the ability of the filter to suppress AC disturbances and improve the quality of the power delivered to the oscillator system.

At the input stage, the supply signal consists of a DC component combined with an unwanted AC ripple component. Due to the presence of this ripple signal, the waveform may contain fluctuations around the desired operating voltage. These fluctuations can alter the operating characteristics of the active device and contribute to phase-noise degradation and frequency instability within the oscillator system [16].

After passing through the third-order π filter, a significant reduction in the AC ripple component is expected. The output waveform is expected to become smoother with reduced voltage variations and lower noise content. Following the voltage regulation stage, the output should provide an approximately constant 5V DC signal with negligible ripple components.

Several performance parameters may be considered during analysis, including:
• Input ripple voltage
• Output ripple voltage

• Ripple attenuation percentage
• Voltage regulation performance
• Frequency stability improvement
• Reduction in supply-pushing effects
• Improvement in signal purity

The implementation of the proposed filtering technique is expected to improve overall oscillator performance by reducing unwanted disturbances that affect the active device and resonator network [16]. Improved filtering can reduce frequency variations and minimize noise propagation into the oscillator circuit. Furthermore, better supply quality is expected to contribute toward enhanced spectral purity and lower phase-noise characteristics.

The higher-order π filter structure also provides better attenuation characteristics compared to simple RC and LC filter configurations because of the combined action of multiple reactive components [13], [14]. This allows improved suppression of supply-induced disturbances and provides more reliable operation for RF and wireless communication systems.

3.6 Simulation Waveforms

The performance of the proposed filtering system can be analyzed using simulation waveforms obtained before and after implementation of the filtering stage. The following waveforms are considered:
• Input voltage waveform with injected noise
• Filter output waveform
• Regulated output voltage waveform
• Ripple comparison before and after filtering
• Frequency response of the proposed filter
The comparison of these waveforms helps evaluate the effectiveness of the proposed filtering approach in reducing supply-induced disturbances.

III. Simulation Results

4.1 Amplifier and Oscillator

1. Amplifier circuit -

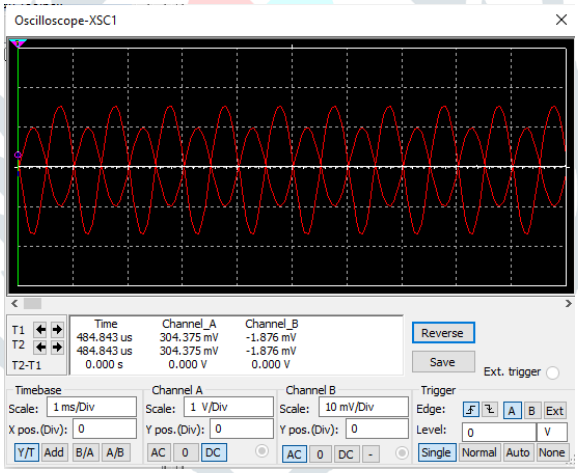

Fig. 8. Transient Analysis of CE BJT amplifier design

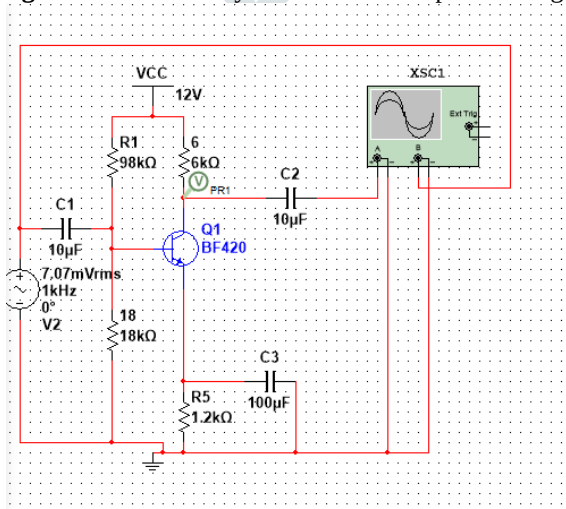

Fig. 9. Common Emitter (CE) BJT amplifier designed

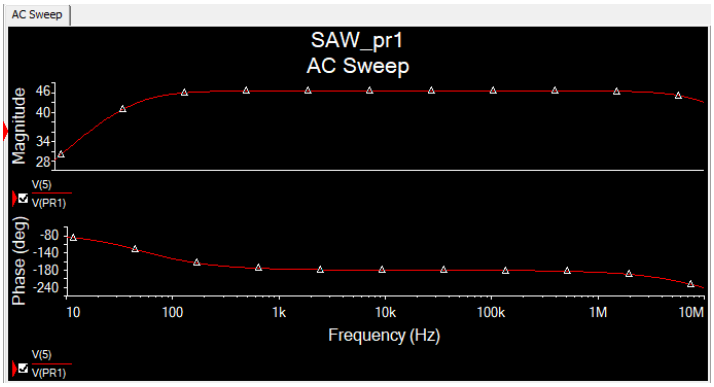

Fig. 10. AC Sweep Analysis of CE BJT amplifer

This is an amplifier circuit mainly used in oscillator circuits for amplification. So, to design an oscillator circuit, you first should get acquainted with design amplifier circuits and get to know their frequency selection criteria. This particular circuit uses BF420 Bipolar Junction Transistor (BJT) in its Common Emitter (CE) mode which uses a 12V DC supply. A 7.07mV RMS sinusoidal signal with a frequency of 1kHz was given to the circuit which portrayed the real-world noise. From the transient analysis of the circuit, we can infer the amplification of the input signal and 180° phase inversion which is a characteristic of Common Emitter amplifiers. The bypass capacitors used at the input and the output help to transfer only the AC signals and maintain the DC bias. To be designed at 1kHz means that the circuit can easily allow the noise of 1kHz frequency to be amplified with a larger gain and suppress the noise at other frequencies. But as observed from the frequency response, the magnitude response remains 46dB across the flat portion of a large frequency range as we aren't using a perfect frequency selector, that is, a resonator. The 7.07mV signal is getting amplified to approximately 1.6V sinusoidal signal thus, having a voltage gain of 226.3. The selectivity can be changed by selecting the correct value for f_L.

2. 1-Port SAW resonator circuit –

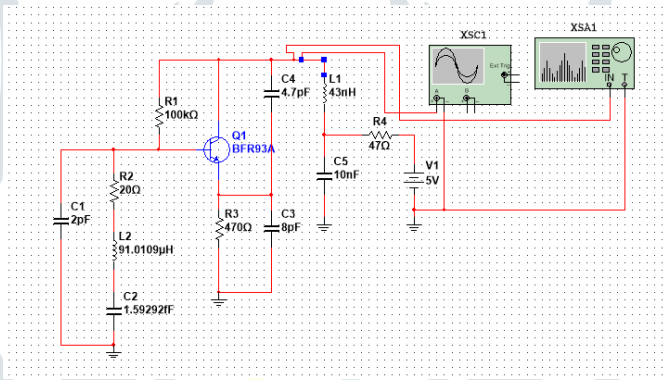

Fig. 11. 1-Port SAW Resonator Circuit designed

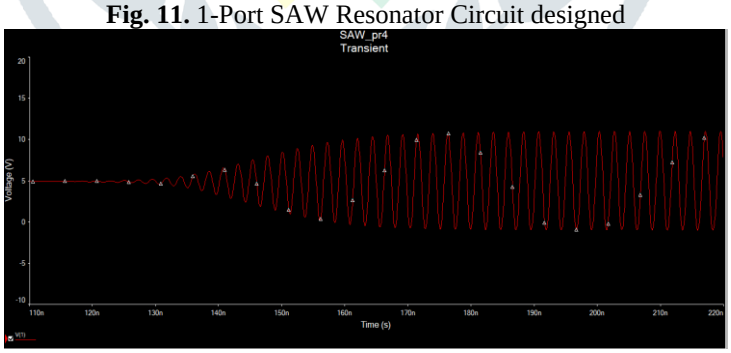

Fig. 12. 1-Port SAW Resonator Circuit Transient Analysis

This is a BFR93A transistor based 1-Port SAW resonator Oscillator circuit with a 5V DC power supply and of frequency 315MHz. It consists of an Equivalent Circuit Model (ECM) of the 1-Port SAW resonator due to the unavailability of a proper SAW resonator component on NI Multisim. The ECM consists of 20Ω motional resistance, 91.0109µH motional inductance, 1.59292fF motional capacitance and 2 pF static capacitance. For additional prevention, we added a Radio Frequency Choke (RFC) to prevent the hindrance of the DC bias of the amplifier. As discussed in previous sections, the oscillations as observed, gradually builds up and stabilizes from the initial response thus highlighting the active amplifier stage is compensating for the losses in the resonant network. The resonant frequency calculated from the motional branch using $f_s=1/(2\sqrt{(L_mC_m)})$ formula is 418MHz and for the LC network formed due to the RFC is 354MHz. Although the frequencies are way different than the desired, these are not the actual oscillation frequencies as it relies on the feedback network, transistor parasitics, impedance matching and loading conditions and thus, we get a 315MHz signal in the end.

3. 2-Port SAW resonator circuit –

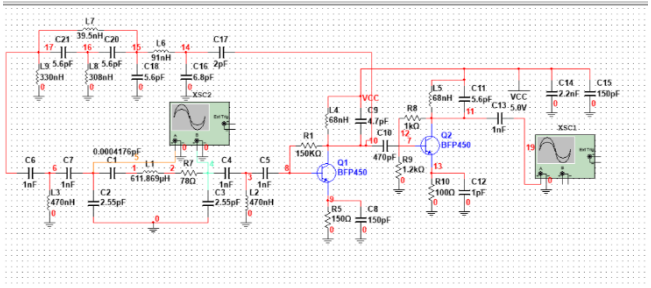

Fig. 13. 2-Port SAW Resonator Circuit designed

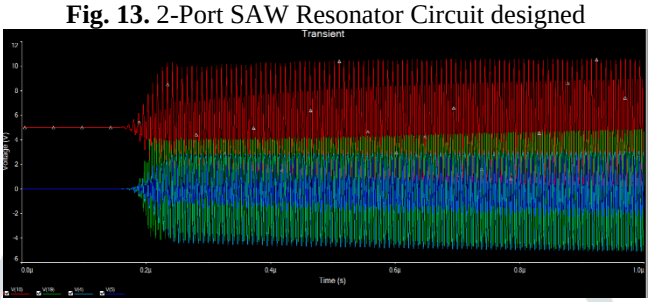

Fig. 14. 2-Port SAW Resonator Circuit Transient Analysis

This is a 2-Port SAW Resonator based oscillator working at 315MHz frequency and uses 2 amplifier stages having BFP450 as the required transistors. The supply given here is again 5V DC for biasing of the amplifier circuit. Here also we have used the SAW resonator equivalent circuit model having motional resistance of 78Ω, motional inductance of 611.869µH, motional capacitance of 0.0004176pF and static capacitance of 2.55pF. Apart from this there are additional inductors and capacitors added to the circuit with different purposes like impedance matching to get the desired oscillations. The transient analysis of this circuit shows how oscillations build up by 0.18µs and comes to a stable amplitude. The series resonant frequency calculated comes out to be 314.85MHz, close to the nominal frequency (315MHz). This circuit also incorporates a Voltage-controlled oscillator (VCO) circuit for better frequency control using the reactive elements. As well as, the circuit has 2 C-L-C impedance matching networks connected before and after the SAW ECM circuit for impedance matching and ease the signal transferring through the feedback path with low losses. Thus, by observing the waveform, we can infer that the active amplifier stages are able to provide the required energy to compensate for losses in the resonant network.

4.2 Power Supply Filters

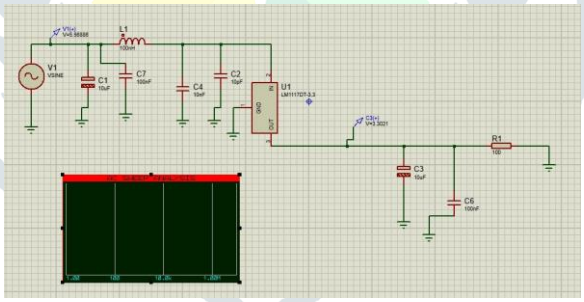

Fig. 15. C-L-C Power Supply filter designed

The proposed power-supply noise reduction circuit was implemented and analyzed using simulation tools. The above circuit shows the designed π-filter integrated with a voltage regulation stage to suppress unwanted disturbances and improve supply stability.

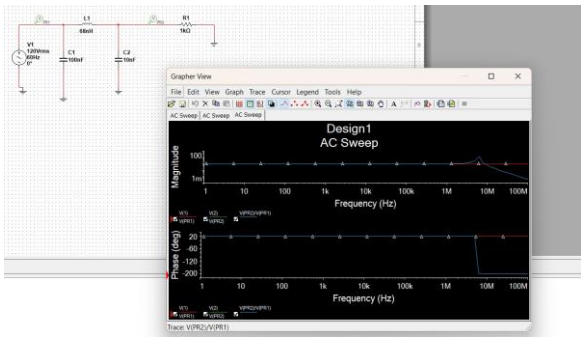

Fig. 16. C-L-C Power Supply Filter AC Sweep

This presents the AC sweep response of the filter, illustrating its attenuation characteristics over different frequencies. The results indicate effective suppression of unwanted noise components, resulting in improved power quality and more stable operation of the oscillator system.

IV. Power Supply Design and Analysis

Phase noise and frequency stability in SAW oscillator-based RF systems are highly sensitive to power supply noise, ripple, and load transient response. A dedicated 5 V regulated supply, derived from a 15 V nominal input, powers the BJT amplifier and associated circuitry. This section presents the complete design methodology of a synchronous step-down (buck) DC-DC converter employing the Texas Instruments TPS561208DDC [13], covering topology selection, analytical design equations, component sizing, and WEBENCH/TINA-TI simulation-based performance verification

5.1 Converter Topology and IC Selection

A non-isolated synchronous buck topology is adopted for its superior efficiency, compact component count, and low output ripple at the required 3:1 voltage conversion ratio. The TPS561208DDC is a 1 A, 4.5–17V input synchronous step-down converter in a 6-pin SOT-23 package [13]. It employs Texas Instruments' D-CAP2™ adaptive on-time PWM control, providing fast transient response and inherent stability with low-ESR ceramic capacitors without external frequency compensation [13]. Key parameters include: $R_{DS(on)}$, H = 140mΩ, $R_{DS(on)}$, L = 84mΩ, nominal switching frequency f_{sw} = 580kHz, internal soft-start = 1.0ms, and VREF = 0.768V. The device operates exclusively in CCM across its full load range, eliminating mode-transition-induced spectral interference on the supply rail [13].

5.2 Circuit Implementation

The converter is designed per the TPS561208 reference application circuit [13], with component values optimised using TI WEBENCH Power Designer. The TINA-TI SPICE simulation schematic is shown in Fig. 17, with all principal measurement nodes annotated. Both the WEBENCH and TINA-TI circuits share identical values: L1 = 4.7µH (DCR = 80mΩ), C_{out} = 47µF (ESR = 2.143mΩ), C_{in} = 2 × 10 µF (ESR = 5.463mΩ each), C_{bst} = 100nF, R_{fbt} = 56.2kΩ, and R_{fbb} = 10kΩ.

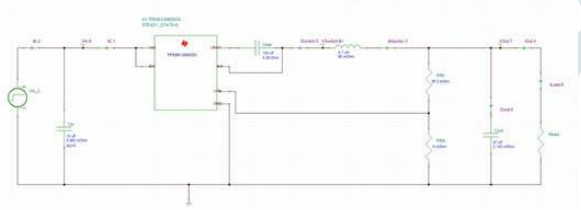

Fig. 17. TINA-TI transient simulation schematic of the TPS561208DDC buck converter. Configured for V_{in} = 15V, V_{out} = 5V, I_{out} = 1A. All measurement nodes labelled [13].

5.3 Duty Cycle and Switching Frequency

In steady-state CCM, the voltage conversion ratio equals the duty cycle D:

$$D = Vout / Vin = 5.0 / 15.0 = 0.333 \ (33.3\%) \qquad (33)$$

D-CAP2 implements an adaptive on-time architecture maintaining quasi-fixed switching frequency across the input range [13]. WEBENCH computation at V_{in} = 15.6V yields D = 33.22% and f_{sw} = 538.95kHz. Figure 18 shows the WEBENCH-simulated duty cycle versus output current across three input voltages. The monotonic positive slope reflects additional on-time needed to compensate resistive drops across $R_{DS(on)}$ and inductor DCR as load increases.

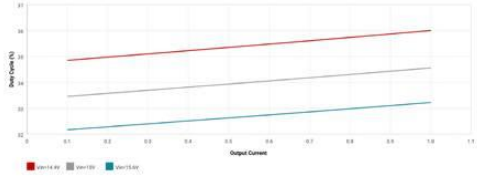

Fig. 18. WEBENCH-simulated duty cycle (%) vs. output current (A) for Vin = 14.4V (red), 15V (grey), and 15.6V (teal). Duty cycle rises from ≈ 32% to ≈ 36% across the 0–1A load range [13].

5.4 Output Voltage Setting

Output voltage is programmed via a resistor divider to the VFB pin (VREF = 0.768 V) [13]:

$$V_{out} = VREF \times (1 + R_{fbt} / R_{fbb}) \qquad (34)$$

Substituting R_{fbt} = 56.2kΩ and R_{fbb} = 10kΩ gives V_{out} = 0.768 × 6.62 = 5.084 V — a 1.6% deviation from the 5.0V target, within the 4.23% tolerance budget for 2% IC feedback and 1% resistor tolerances [13]. Both steady-state simulations confirm $V_{out,avg}$ = 5.14V.

5.5 Output Inductor Sizing

Peak-to-peak inductor ripple current in CCM [13]:

$$\Delta IL = (V_{out} / V_{in,max}) \times (V_{in,max} - V_{out}) / (L \times f_{sw}) \qquad (35)$$

With L = 4.7 µH, $V_{in,max}$ = 15.6V, V_{out} = 5V, and f_{sw} = 538.95kHz: ΔI_L = 1.36A. Peak switch current $I_{L,peak}$ = 1.0 + 0.68 = 1.68 A, below the 2A output current load limit [13]. RMS current $I_{L,rms} = \sqrt{(1.0^2 + 1.36^2/12)} \approx 1.07$A gives $P_L = 1.07^2 \times 80mΩ \approx 91.5$mW (WEBENCH: 92.34mW).

5.6 Output Capacitor and Ripple Analysis

Peak-to-peak output voltage ripple for a low-ESR ceramic capacitor:

$$\Delta V_{out} \approx \Delta I_L \times (ESR + 1 / (8 \times C_{out} \times f_{sw})) \quad (36)$$

With C_{out} = 47µF (ESR = 2.143mΩ), ΔI_L = 1.36A: ΔV_{out} ≈ 9.6mV analytically; WEBENCH reports 19.06mV. Steady-state TINA-TI simulation (Fig. 18) confirms ΔV_{out} = 16.20mV at $V_{out,avg}$ = 5.14V and f_{sw} = 590.20kHz — all within the 30mV design limit. Output capacitor RMS current $I_{Co,rms}$ = 392.7mA gives $P_{d,\,Cout}$ = 330.48µW [13].

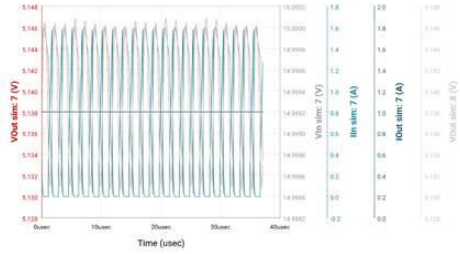

Fig. 18. TINA-TI steady-state simulation: V_{out} oscillates between 5.130V and 5.148V, yielding ΔV_{out} = 16.20mV peak-to-peak at $V_{out,avg}$ = 5.14V and f_{sw} = 590.20kHz [13].

5.7 Input Capacitor Selection

Two 10µF / 25V ceramic capacitors in parallel give $C_{in,eff}$ = 20µF. Input ripple current:

$$I_{Cin,rms} = I_{out} \times \sqrt{(D \times (1 - D))} = 1.0 \times \sqrt{(0.333 \times 0.667)} \approx 471mA \quad (37)$$

WEBENCH reports $I_{Cin,rms}$ = 522.56mA (including inductor ripple), well within each capacitor's 2.37A rating, with $P_{d,Cin}$ = 745.9µW. A 100nF bootstrap capacitor (C_{bst}) between VBST and SW is mandatory for high-side gate drive biasing [13].

5.8 Thermal Analysis and Power Budget

IC power dissipation is modelled as [13]:

$$P_{IC} = I_{out}^2 \times (R_{DS(on),H} \times D + R_{DS(on),L} \times (1-D)) + P_{sw} \quad (38)$$

WEBENCH reports P_{IC} = 249.12mW, P_L = 92.34mW, $P_{d,Cout}$ = 330.48µW, and $P_{d,Cin}$ = 745.9µW, giving P_{total} = 342.9mW. Junction temperature:

$$T_j = T_a + P_{IC} \times \theta_{JA,eff} = 30 + 249.12 \times 10^{-3} \times 60 = 44.95°C \quad (39)$$

At 44.95°C — 80°C below the 125°C rated maximum and 115°C below the 160°C thermal shutdown threshold — the design supports continuous operation at ambient temperatures up to ≈ 80°C without derating [13].

5.9 Efficiency Analysis

Full-load conversion efficiency:

$$\eta = P_{out} / P_{in} = 5.0 / (5.0 + 0.343) = 93.58\% \quad (40)$$

Figure 19 presents the WEBENCH efficiency curves across Vin = 14.4V, 15V, and 15.6V. Peak efficiency of ≈ 94–95% is achieved at 0.5–0.6A partial load. The three curves overlap closely, confirming less than 1 percentage point variation across the input voltage range — important for RF supplies subject to upstream transients.

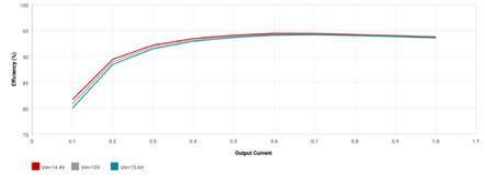

Fig. 19. WEBENCH efficiency (%) vs. output current (A) for V_{in} = 14.4V (red), 15V (grey), and 15.6V (teal). Full-load efficiency is 93.58% at V_{in} = 15.6V; peak ≈ 94–95% at partial load [13].

5.10 Soft-Start and Startup Behavior

The integrated 1.0ms soft-start linearly ramps the internal reference on EN assertion, preventing inrush current and inductor saturation [13]. Figure 20 shows the TINA-TI startup simulation: V_{out} rises monotonically from 0V and achieves 90% of its 5.14V regulated value within 0.94ms, with no overshoot or oscillation. Peak inductor current during startup is 1.72A — below the 2.0A OCL (Output Current Load) limit [13].

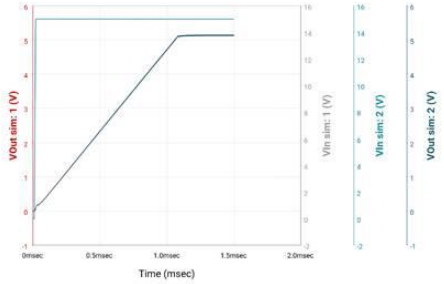

Fig. 20. TINA-TI startup simulation: V_{out} ramps from 0V to steady-state ≈ 5.14V. Output settles within 0.94ms with no overshoot, confirming correct D-CAP2 soft-start operation [13].

5.11 Load Transient Response

Load transient performance (Fig. 21) for a 1.0A to 0.1A step with 10µs transition edges shows symmetrical overshoot/undershoot of 70mV (1.36% of V_{out}) with a 20µs recovery time. D-CAP2 re-asserts the on-pulse within one switching cycle of detecting a feedback error [13], comparing favourably with conventional voltage-mode PWM controllers that typically require several cycles. This is well within the ±5% (±250mV) transient specification.

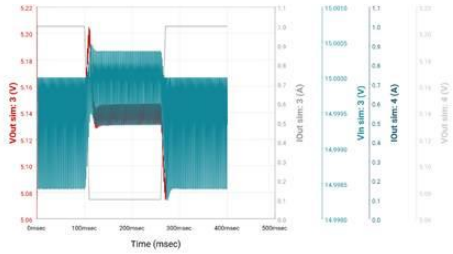

Fig. 21. TINA-TI load transient simulation: V_{out} exhibits 70 mV overshoot/undershoot for a 1.0A to 0.1A step, recovering to regulation within 20µs. $V_{out,avg}$ = 5.14V [13].

5.12 Input Transient Response

Figure 22 shows the output response to a V_{in} step between 14.4V and 15.6V under a fixed 1A resistive load. Output voltage deviation is below 20mV (0.39%) across the 1.2V (8%) input step, with recovery within 50µs — a line rejection ratio exceeding 26dB. This level of power supply rejection is adequate for the BJT amplifier and oscillator stages, where supply-induced noise directly sets the phase noise floor.

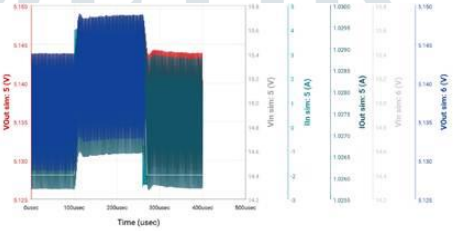

Fig. 22. TINA-TI input transient simulation: Vout deviation < 20mV for a 1.2V V_{in} step (14.4V to 15.6V), recovering within 50µs. Load current remains stable at 1.028A [13]

Table. 1. Power supply bill of materials – TPS561208DDC buck converter

Component	Part / Value	Specification	Qty
U1 – TPS561208DDC	IC – Sync. Buck	V_{in}: 4.5–17V, V_{out}: 0.76–7V, 1A, 580kHz	1
L1 – Output Inductor	NIC NPI43C4R7MTRF	4.7µH, DCR = 80mΩ	1
C_{out} – Output Cap.	TDK C3216X5R1C476M160AB	47µF, ESR = 2.143mΩ, 16V, X5R	1
C_{in} – Input Cap.	Taiyo Yuden MSAST21GBB5106MTNA01	10µF, ESR = 5.463mΩ, 25V, X5R	2
C_{bst} – Bootstrap Cap.	AVX 08053C104KAT2A	100nF, ESR = 280mΩ, 25V, X7R	1
R_{fbt} – Upper Feedback R	Yageo RC0201FR-0756K2L	56.2kΩ, 1%, 50mW	1
R_{fbb} – Lower Feedback R	Yageo RC0201FR-0710KL	10kΩ, 1%, 50mW	1

Table. 2. Simulated performance summary – 15V to 5V synchronous buck converter

Parameter	Simulated Value	Design Target / Spec.
Input Voltage (V_{in})	14.4 – 15.6V	4.5 – 17V
Output Voltage ($V_{out,avg}$)	5.14V	5.0V nominal
Switching Frequency	538.95kHz (calc.) / 590.2kHz (sim.)	580kHz nominal
Duty Cycle	33.22%	$V_{out}/V_{in,nom}$ ≈ 33.3%

Conduction Mode	CCM	CCM (full load)
Peak-to-Peak V_{out} Ripple	16.20mV (sim.) / 19.06mV (calc.)	< 30mV
Peak-to-Peak ΔI_L	1.24A (sim.) / 1.36A (calc.)	< 1.50A
Peak Switch Current	1.68A	< 2.0A (OCL)
Load Transient Overshoot	70mV (0.1A to 1.0A step)	±250mV (±5% V_{out})
Transient Settle Time	0.02ms (20µs)	< 1.0ms
Efficiency η (full load)	93.58%	> 90% at 1A
Total Power Dissipation	342.9mW	< 500mW
IC Junction Temperature T_j	44.95°C	< 125°C ($T_{J,max}$)
Startup Time	0.94ms	≈ 1.0ms (internal SS)
Input Cap. RMS Current	522.56mA	< 2.37A per capacitor
Output Cap. RMS Current	392.7mA	< rated I_{RMS}

sim. = TINA-TI steady-state simulation. All values at T_a = 30°C, Vin = 15.6V, I_{out} = 1.0A unless stated.

All simulated parameters satisfy design targets with substantial margin. Output voltage ripple (16.20mV) and transient deviation (70mV) remain within the budgets established by the oscillator supply sensitivity analysis. The IC junction temperature of 44.95°C — 80°C below the rated maximum — confirms long-term thermal reliability under continuous full-load operation.

V. Conclusion

In conclusion, the proposed work emphasizes that to create a perfectly working oscillator, the designer should not only focus on the resonator design but also one the active amplifier designs and the power supply conditioning. The research signifies the different ways of creating low-noise SAW resonator-based oscillators and their associated feedback networks. The addition of VCO and C-L-C impedance matching network highlight the careful consideration of reactive network design for stable oscillations. These oscillators are used in many applications from local oscillator to RF transmitter / receiver mixer (or clock distribution network), depending on the system architecture. Future work may involve Printed Circuit Board (PCB) development, design validation of the circuits and low-noise perfections.

References

A. References

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B. Figure References

Fig.1. – [2]
Fig.2. – [1]
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