DESIGN OF LOW POWER 2:1 MULTIPLEXER WITH MT-CMOS TECHNIQUE

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ABSTRACT - Multiplexer with less number of transistors is designed, that will give high speed response and low power consumption. In many applications Multiplexer is used as a universal element, that will collect the data from many sources and transmits to a single destination. In low power techniques, one of the efficient technique is MT-CMOS.In MT-CMOS technique the leakage power is effectively reduced. The operating modes of MT-CMOS are low threshold mode and high threshold mode. The Speed performance is increased by Low threshold mode and the leakage power is reduced by the high threshold mode. By operating sleep bar transistors and sleep transistors with high threshold voltages, the leakage power in MTCMOS circuits can be reduced. When sleep bar input is ON and sleep input is OFF, the current flow in the low threshold voltage main circuit is zero. When sleep bar is OFF and sleep is ON then the circuit works in normal Mode. MT-CMOS technique has low power dissipation 0.011890nwatts compared to traditional 2:1 Multiplexer 1.0308nwatts. Mentor Graphics 130nm technology is used in the design of this circuit.

Keywords: Threshold Voltage, MT-CMOS (Multi Threshold Voltage), Multiplexer, Low Power, 130nm Technology.

INTRODUCTION

In this present mobilized world the basic requirement from the consumers is devices with low power consumption, which in turn became the principal theme in today's electronic industry. This resulted in a major paradigm shift in the designing with power dissipation as important consideration as performance and area. In most of the digital modules like CPUs, graphics controllers, PLDs, in telecommunications and in computer networks multiplexers are used as basic building blocks and these multiplexers as also the building blocks of switch logic, where the circuits are implemented as combination of switches. Hence in this paper we present the design of a low power dissipative D – Flip-Flop based 2:1 multiplexer.

CMOS TECHNIQUE

In CMOS (complementary metal oxide semiconductor) design, Both the NMOS and PMOS networks are complementary to each other. During 40 years CMOS devices are continuously scaled for achieving lower power consumption, high density and performance. The power consumption is kept under control by scaling down the supply voltage (VDD).To achieve improved performance and high drive current, subsequently the transistor threshold voltage (Vth) has been scaled down. Due to scaling of the threshold voltage, the sub threshold leakage current is increased.

Dynamic Power consumption and static Power consumption are components of Power consumption in CMOS circuits. Switching of the transistors causes Dynamic power consumption. Irrespective of the transistor switching, the static power consumption is present. At 0.18µ technology and above Dynamic power consumption is dominant factor and it is more than 90% of the total chip power. Therefore Frequency scaling and voltage scaling techniques are concentrated on dynamic power reduction. static power consumption is become challenge with decrease of feature size from 0.18µ technology to 0.09µ and 0.065µ technologies.

MT-CMOS TECHNIQUE

Multi Threshold Complementary Metal Oxide Semiconductor can be simply called MT-CMOS. The Multi-threshold CMOS chip technology provides optimized power and delay by having transistors with multiple threshold voltages (V_{th}). The threshold voltage of a MOSFET is the gate voltage where an inversion layer forms at the interface between the substrate and the insulating layer of the transistor. In order to minimize clock periods on critical delay paths ,the faster switching Low V_{th} devices are useful. the static leakage power is high in low V_{th} devices.The static leakage power can be reduced by using High V_{th} devices without causing a delay.

One method of creating devices with multiple threshold voltages is to apply different bias voltages (Vb) to the base or bulk terminal of the transistors. Other methods involve adjusting the gate oxide thickness, gate oxide dielectric constant (material type), or dopant concentration in the channel region beneath the gate oxide.

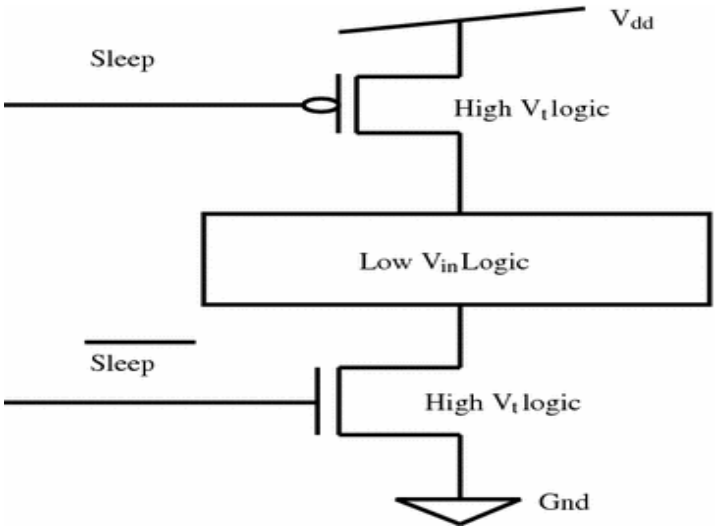


Fig.1. MTCMOS model

Figure.2 Conventional 2:1 Multiplexer schematic

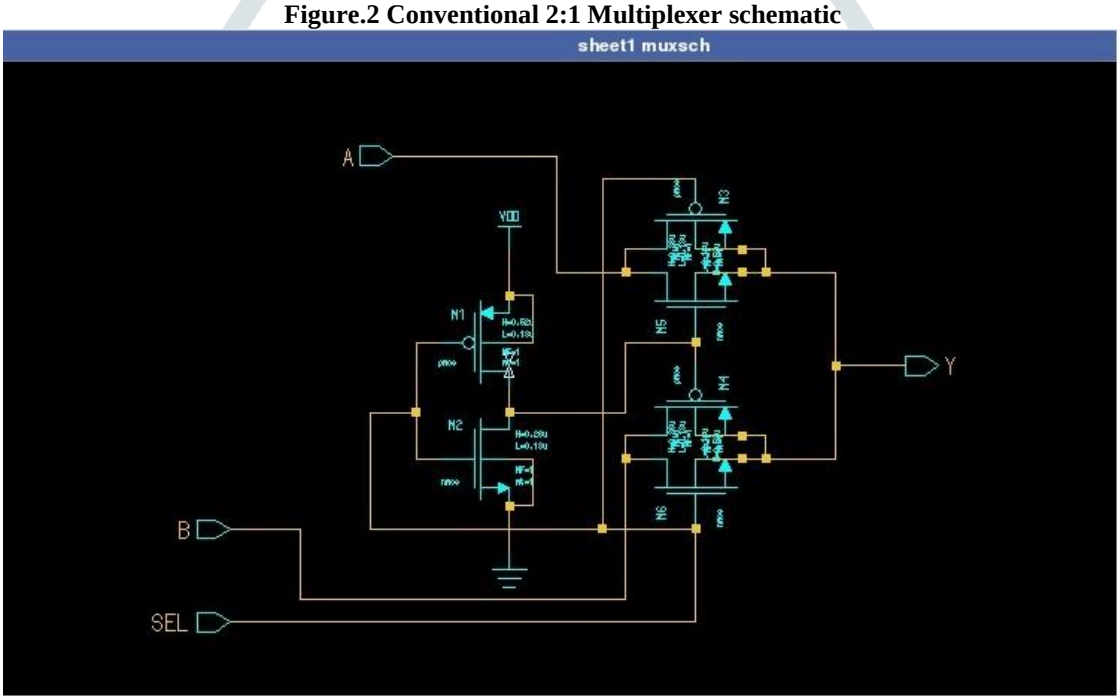
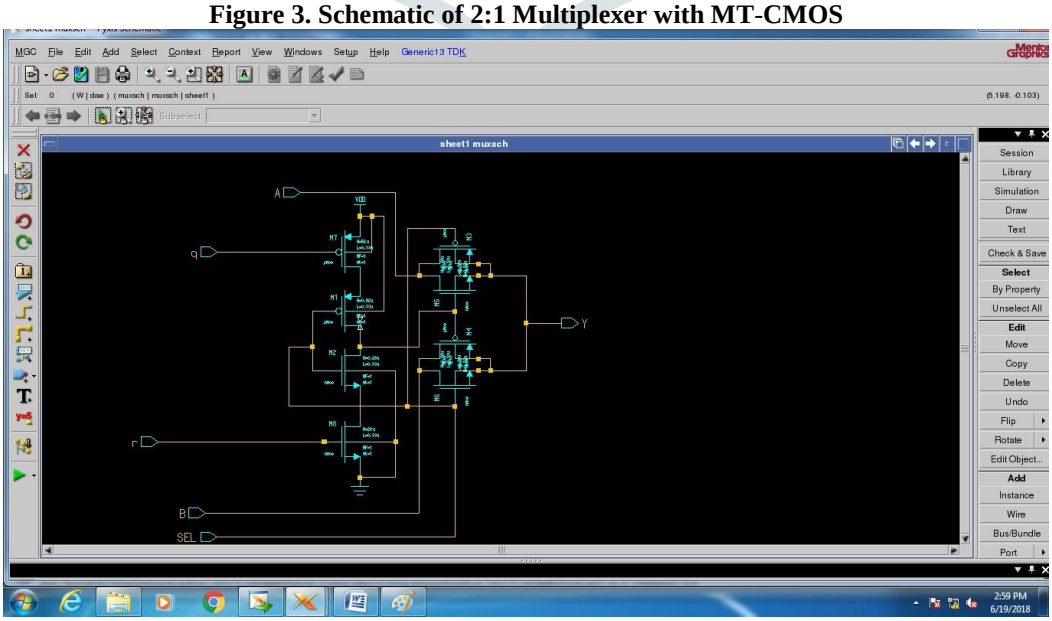


Figure 3. Schematic of 2:1 Multiplexer with MT-CMOS



RESULTS

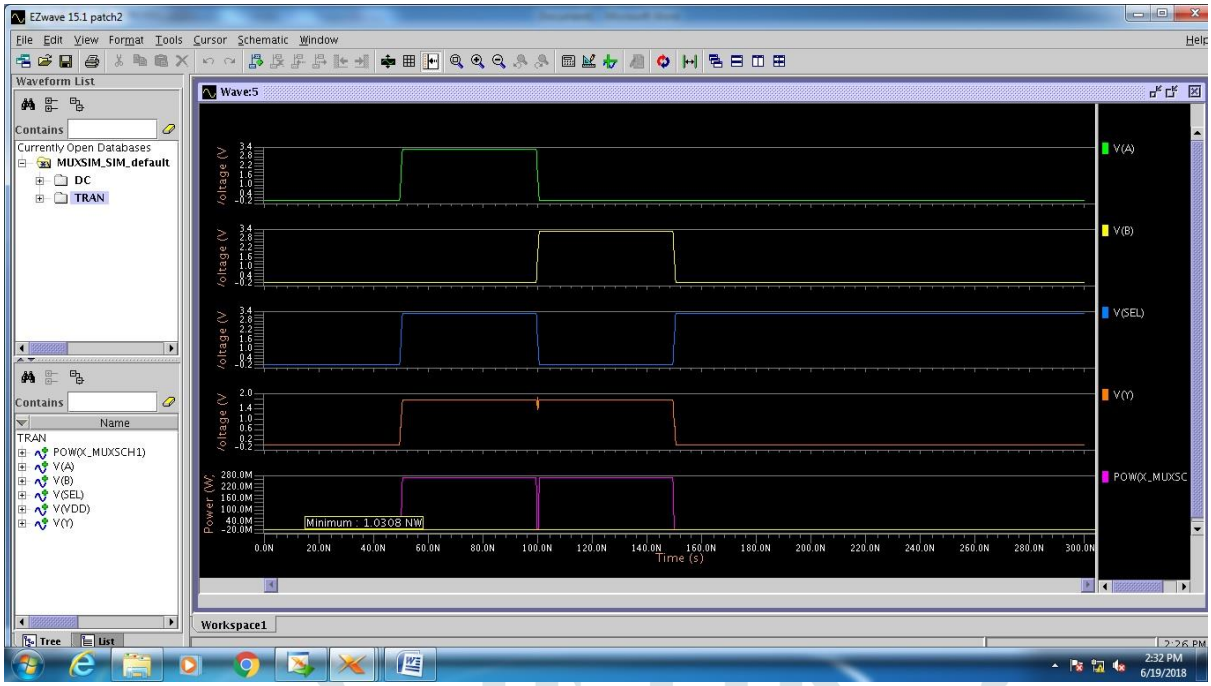


Fig 4 Conventional 2:1 Multiplexer Output waveforms

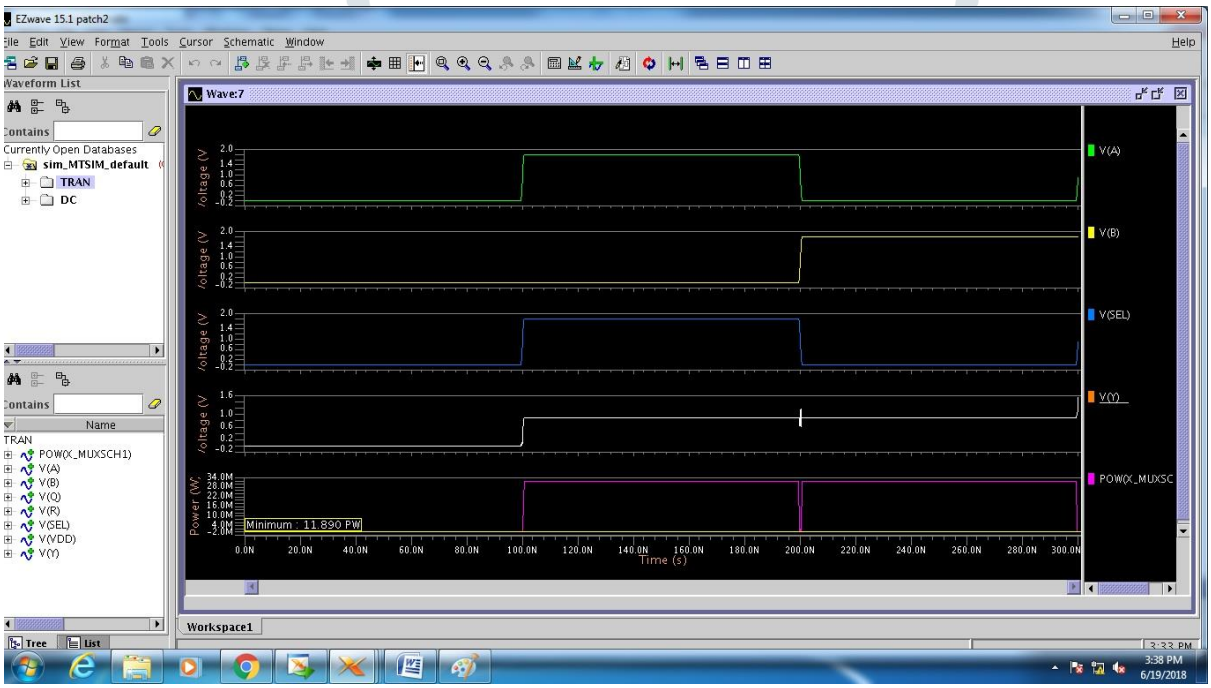


Fig 5. Output waveforms of 2:1 Multiplexer with MT-CMOS

Table 1. Power dissipation (Leakage power)

Power dissipation In Nano Watts	MUX without MT-CMOS technique	MUX with MT-CMOS technique
	1.0308	0.011890

CONCLUSION

The author of my base paper was implemented the same circuit on 130nm technology and succeeded at leakage power reduction. I have implemented the same circuit on 130nm technology by varying channel length and reducing power supply to 1.8v. My results are better than the existed results. If it is possible to access advanced technologies like 90nm, 45nm etc we can reduce the leakage power more and more and also we can reduce the power supply. Many FPGA vendors use the multiplexer as a basic block FPGA's so it is going to be very useful.

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