Design and Implementation of 2-4 Mixed-Logic Line Decoders for unsupervised learning

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Abstract*—Recent advancement in CMOS technology involve materials progress which led to new design structures and new design techniques in nanoscale circuits. The 90nm design rules uses CMOS circuits and materials for metal interconnects, allow the design of basic circuits with low power consumption, low delay and less transistor numbers. In this paper, mixed-logic implementation of 2-4 line decoders, combining pass transistors, static CMOS and transmission gates. Comparative spice simulations show that the circuits present a significant improvement in power and delay, outperforming CMOS in almost all cases. Unsupervised learning is used for decoding which can be further used in many applications.

Index Terms—***Line decoder, mixed-logic, pass transistor logic, transmission gate logics, unsupervised learning.***

I. Introduction

Static CMOS circuits are widely used for majority of logic gates in integrated circuits [1]. They consist of complementary N-type metal oxide semiconductor (nMOS) pulldown and P-type metal oxide semiconductor (pMOS) pullup networks, which presents good performance. CMOS logic is characterized by robustness against voltage scaling and transistor sizing and thus reliable operation at low voltages and small transistor sizes [2]. Input signals are connected to the transistor gates only, reducing design complexity and facilitation of cell-based logic synthesis and design.

Pass transistor logic (PTL) was developed in 1990s, when various design styles were introduced aiming to provide an alternative to CMOS logic. Inputs are applied to both the gates and source/drain diffusion terminals of transistor. They are implemented with either individual nMOS/pMOS pass transistors or parallel pairs of nMOS and pMOS called Transmission gates [3].

Line decoders are the fundamental circuits which are widely used in peripheral circuitry of memory arrays. This develops a mixed-logic methodology for their implementation, for improved performance compared to single-style design.

II. Overview of Line Decoder Circuits

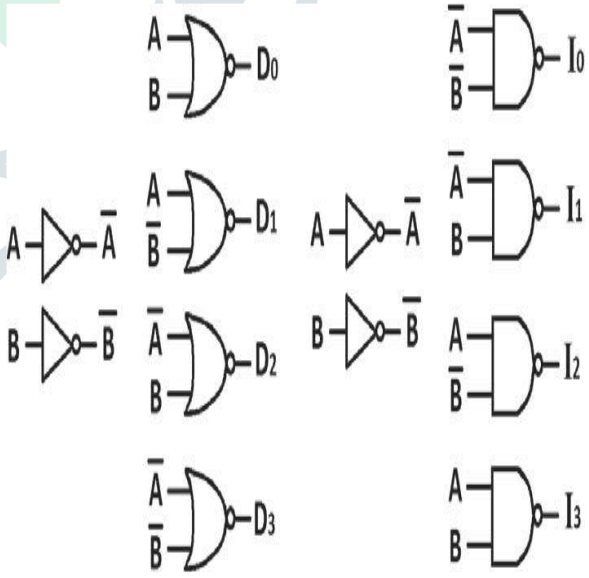
In digital systems, discrete quantities of information are represented by binary codes. An *n*-bit binary code can represent up to 2^n distinct elements of coded data. A decoder is a combinational circuit that converts binary information from *n* input lines to a maximum of 2^n unique output lines or fewer if the *n*-bit coded information has unused combinations. The circuits examined here are n-to-m line decoders, which generate the m = 2^n minterms of *n* input variables [5].

A. 2-4 Line Decoder

A 2-4 decoder has 2 inputs A and B and generates the 4 outputs D0-3.Based on the input combination, one of the four output is selected and set as 0, and the remaining are set as 1.A 2-4 decoder can be designed by using 2 inverters and 4 NOR gates, both yielding a total of 20 transistors and this can be shown in Fig. 1(a).The truth table of the 2-4 decoder is shown in Table I.

B. Inverting 2-4 Line Decoder

An inverting 2-4 decoder has 2 inputs A and B and generates the complementary outputs of I0-3. Based on the input combination one of the output is selected and set as 1 and the remaining are set as 0. An inverting 2-4 decoder can be designed by using 2 inverters and 4 NAND gates, both yielding a total of 20 transistors and this can be shown in Fig. 1(b). The truth table of the inverting 2-4 decoder is shown in Table II.



(a) (b)

Fig. 1. 20-transistor 2-4 line decoders implemented with CMOS logic. (a) Non inverting NOR-based decoder.
(b) Inverting NAND-based decoder

TABLE I

TRUTH TABLE OF THE 2-4 DECODER

A	B	D_0	D_1	D_2	D_3
0	0	**1**	0	0	0
0	1	0	**1**	0	0
1	0	0	0	**1**	0
1	1	0	0	0	**1**

TABLE II

TRUTH TABLE OF THE INVERTING 2-4 DECODER

A	B	I_0	I_1	I_2	I_3
0	0	**0**	1	1	1
0	1	1	**0**	1	1
1	0	1	1	**0**	1
1	1	1	1	1	**0**

The schematic diagram of CMOS based NOR/NAND gate is shown in the Fig. 2(a) and Fig. 2(b)

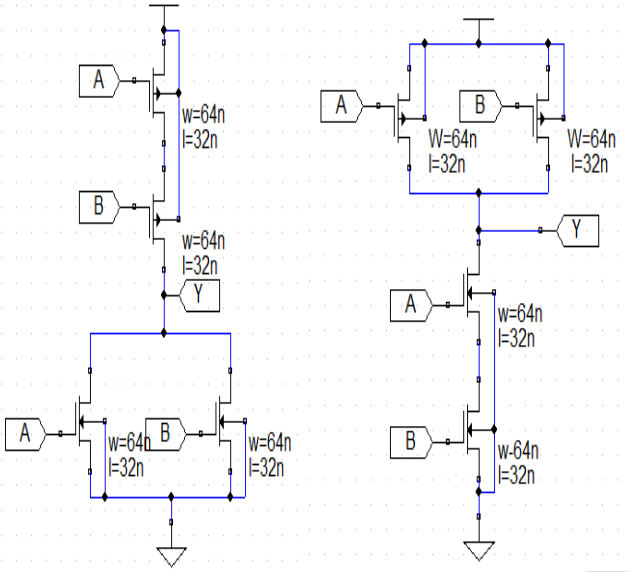


Fig. 3. Schematic view of (a) NOR gate (b) NAND gate

III. PROPOSED SYSTEM

A. 14- Transistor 2-4 Low-Power Topology

A 14-transistor 2-4 low power can be designed by using either TGL or DVL gates would require 5 PMOS and 9 NMOS, whereas, 14 transistor inverting decoder would require 5 NMOS and 9 PMOS, yielding a total of 14 transistors each. The new 14 transistor 2-4 decoders are shown in Fig 3(a) and Fig 3(b).

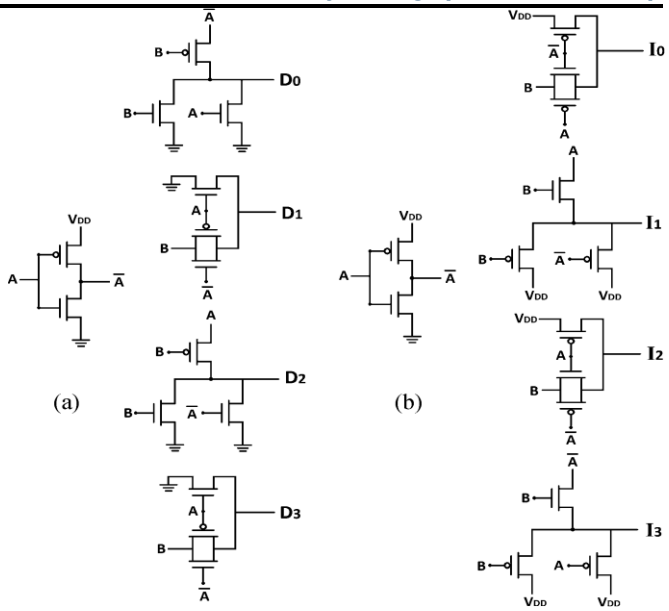


Fig. 3. 14-transistor 2-4 line decoders. (a) 2-4 LP. (b) 2-4 LPI.

The D0 and D2 can be designed with DVL gates where A is used as the propagating signal and D1 and D3 can be designed with TGL gates in this B is used as the propagating signal, whereas in inverting I0 and I2 can be designed with TGL gates in this B as the propagating signal and I1 and I3 can be designed with DVL gates where B is used as propagating signal. The new two topologies are LP and LPI whereas LP stands as Low power and I as Inverter.

B. 15 transistor 2-4 High performance decoder

The low-power topology presented above have a drawback in the case of D0 and I3 regarding worst case delay which comes from the use of complementary A used as the propagating signal. D0can be designed with CMOS NOR gate and I3 with CMOS NAND gate. The 2-4 HP can be designed by using 9nMOS and 6pMOS whereas 2-4HPI can be designed by using 6nMOS and 9pMOS, yielding a total of 15 transistors each. The 2-4HP and 2-4HPI decoders are shown in Fig 4(a) and (b) respectively. So, in 15 transistors topology there is an improvement in delay compare than 2-4 low power topology but slightly increase in power dissipation.

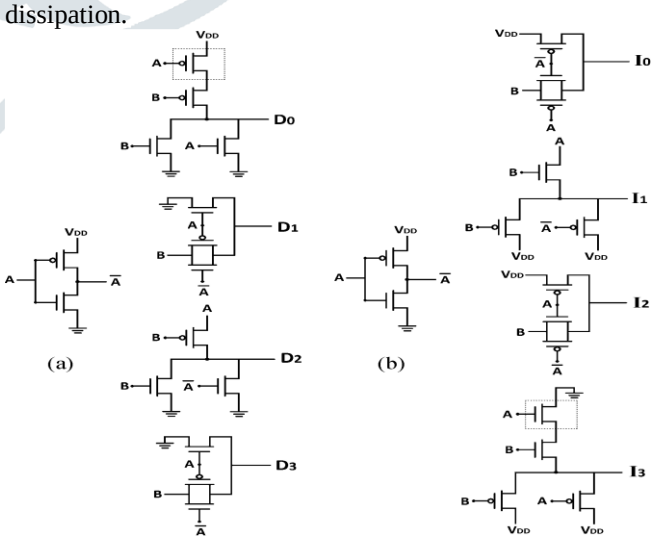


Fig. 5. 15-transistor 2-4 line decoders (a) 2-HP. (b) 2-4 HPI

IV. UNSUPERVISED LEARNING

In unsupervised learning, the training set/data consists of unlabeled inputs, that is, of inputs without any assigned desired output. For instance, in Fig. 6, the inputs are again points in the two-dimensional plane, but no indication is

provided by the data about the corresponding desired output. Unsupervised learning generally aims at discovering properties of the mechanism generating the data. In the example of Fig. 6 [7], the goal of unsupervised learning is to cluster together 2 input points that are close to each other, hence assigning a label – the cluster index – to each input point (clusters are delimited by dashed lines). Applications include clustering of documents with similar topics. It is emphasized that clustering is only one of the learning tasks that fall under the category of unsupervised learning.

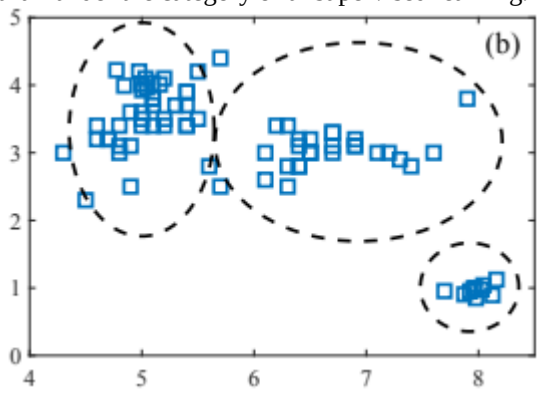


Fig. 6. Unsupervised learning

The performance of the decoders can be improved by applying machine learning techniques.

For example, Machine learning for neural decoding

Neural decoding uses activity recorded from the brain to make predictions about variables in the outside world. In the general framework for decoding, there are *N* neurons whose spiking activity is recorded for a period of time, *T* as in Fig. 7(a) [8]. The focus is on output variables that are continuous (velocity, position) rather than discrete.

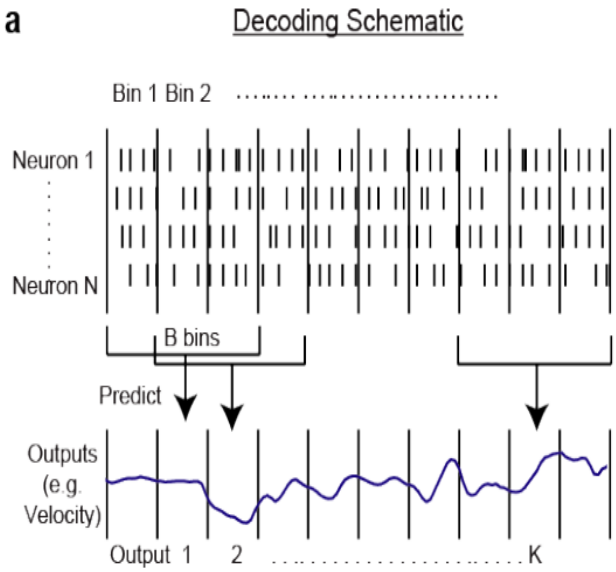


Fig. 7(a) General framework for decoding

V. SIMULATIONS

This section performs with the simulation of single style design and mixed style design of 2-4 Line Decoders. The circuits are implemented using a 32 nm predictive technology model for low-power applications (PTM LP) [6], incorporating high-k/metal gate and stress effect. SPICE simulation is done using Tanner EDA Tools, results are shown and its analysis is identified.

A. Simulation Setup

All circuits are simulated with varying frequency (0.5, 1.0, 2.0 GHz) and voltage (0.8, 1.0, 1.2 V), for a total of 9 simulations at a temperature of 25° C and the average power/delay is calculated and presented in each case. All inputs are buffered with balanced inverters (Lon = Lap = 32 nm, Wn = 64 nm, Wp = 128 nm) and all outputs are loaded with a capacitance of 0.2 fF, as shown in Fig. 8.1.

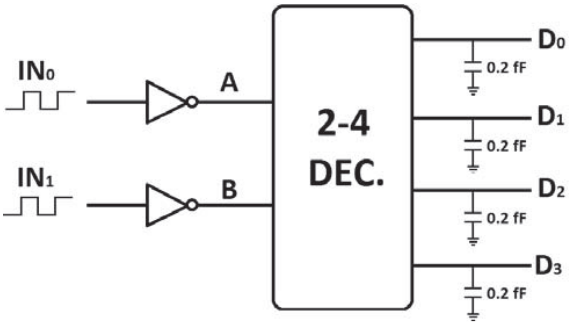
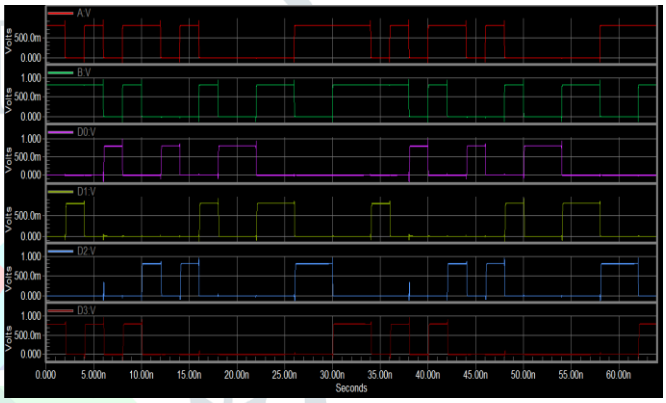
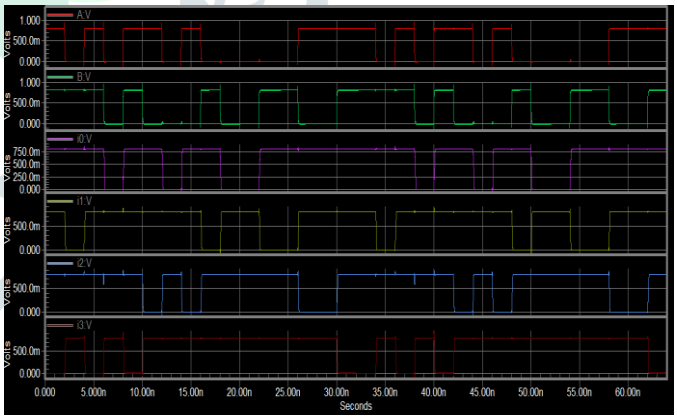


Fig. 8.1. Simulation setup regarding input/output loading conditions of 2–4 Decoders

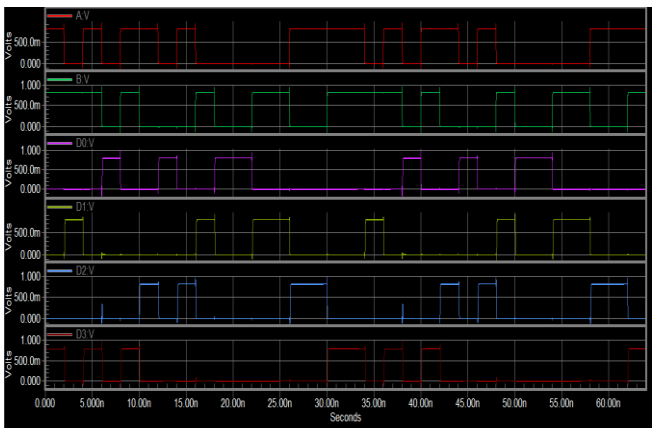
B. Results for proposed 2-4 decoders



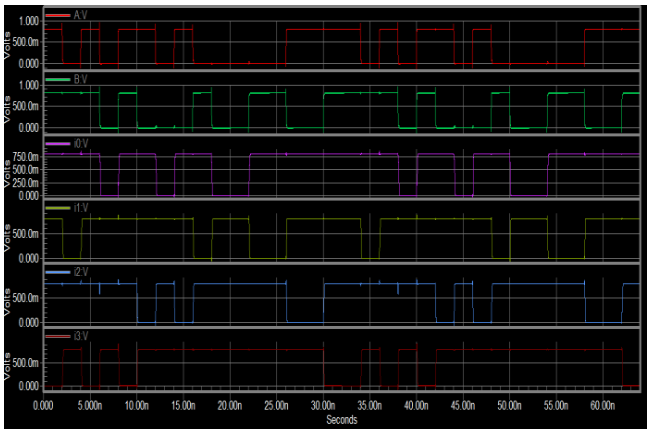
(a)



(b)



(c)



(d)

Fig. 8.2. Input/output waveforms of the proposed 2-4 decoders for all input transitions. (a) 2-4LP. (b) 2-4LPI. (c) 2-4HPI. (d) 2-4HPI

TABLE III

POWER DISSIPATION RESULTS (IN NANOWATTS)

2-4 DEC.	500MHZ			1GHZ			2GHZ		
	0.8	1	1.2	0.8	1	1.2	0.8	1	1.2
CMOS	263	415	620	529	857	1274	1011	1747	2511
2-4LP	257	356	557	456	769	1139	962	1565	2326
2-4HP	237	384	574	496	776	1159	972	1563	2356
CMOS INV	259	419	623	615	849	1282	1055	1758	2593
2-4LPI	234	379	559	475	763	1135	948	1546	2265
2-4HPI	239	375	557	436	754	1138	957	1550	2332

TABLE IV

PDP RESULTS (IN ELECTRONVOLTS)

2-4 DEC.	500MHZ			1GHZ			2GHZ		
	0.8	1	1.2	0.8	1	1.2	0.8	1	1.2
CMOS	172	135	125	329	257	249	698	474	516
2-4LP	157	87	113	329	210	237	656	405	535
2-4HP	157	115	117	328	210	232	656	434	470
CMOS INV	158	111	129	336	263	269	682	541	541
2-4LPI	163	111	117	333	203	226	686	422	459
2-4HPI	159	109	115	311	206	271	629	429	472

TABLE V

PROPOGATION DELAY RESULTS (IN PICOSECONDS)

2-4 DEC	0.8V	1.0V	1.2V
CMOS	96	46	29
2-4 LP	111	45	35
2-4 HP	108	43	36
CMOS INV	102	42	32
2-4 LPI	119	49	31
2-4 HPI	105	48	32

VI. CONCLUSION

This paper has introduced an efficient mixed-logic design for decoder circuits, by combining TGL, PTL and static CMOS. By using this methodology, four new 2-4 line decoders are developed, namely 2-4LP, 2-4LPI, 2-4 HP and 2-4HPI, which offers reduced transistor count and improved power-delay performance in comparison with CMOS decoders.

A variety of spice simulations were performed which make them mostly suitable for applications where area and power minimization is of primary concern. When applied to unsupervised learning, they can be used as building blocks in the design of larger multiplexers and other combinational circuits of varying performance requirements.

This reduced transistor count and low-power characteristics can benefit both bulk CMOS and SOI designs as well.

REFERENCES

[1] N. H. E. Weste and D. M. Harris, “CMOS VLSI Design, a Circuits and Systems Perspective,” 4th ed., 2011: Addison-Wesley.

[2] R. Zimmermann and W. Fichtner, "Low-Power Logic Styles: CMOS Versus Pass-Transistor Logic", IEEE Journal of Solid State Circuits, vol. 32, no. 7, pp.1079 -1090, 1997.

[3] K. Yano, et al., "A 3.8-ns CMOS 16x16-b multiplier using complementary pass-transistor logic," IEEE J. Solid-State Circuits, vol. 25, pp.388 - 393, 1990.

[4] M. Suzuki, et al., "A 1.5ns 32b CMOS ALU in double pass-transistor logic," Proc. 1993 IEEE Int. Solid-State Circuits Conf., pp.90 -91 1993.

[5] X. Wu, "Theory of transmission switches and its application to design of CMOS digital circuits," International J. Circuit Theory and Application, vol. 20, no. 4, pp.349 -356, 1992.

[6] Available at: http://ptm.asu.edu/

[7] Osvaldo Simeone, “A Very Brief Introduction to Machine Learning With Applications to Communication Systems.

[8] Joshua I. Glaser, Raeed H. Chowdhury, Matthew G. Perich, Lee E. Miller, and Konrad P. Kording, Machine Learning for neural decoding.