Design and performance evaluation of low power & high speed hybrid 1-bit full adder for extensive PDP reduction using PTL

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Abstract : Modern VLSI techniques focus heavily on propagation of high speed and low power consumption. In this research paper, we present a hybrid 1-bit full adder using pass transistor logic design which employs both static CMOS logic and Pass Transistor Logic (PTL). We have compared our work against other state of art designs, for power consumption, speed and area constraints. We designed all the full-adders in cadence CMOS technology. At 1.8V power supply, the average power consumed by our design is 2.33µW, at 100MHz and the propagation delay 0.19 ns. It reduces transistor count and due to this power consumption reduces and hence Power delay product reduces.

Index Terms **– Pass transistor logic, High speed, Low power, Power delay product**

I. INTRODUCTION

Presently in electronics industry low power has come up as a prime theme. The requirement for low power has become a major factor as essential as area and performance . In all digital circuits full adder is used as a vital building block so, definitely, improving the performance will improve the overall design performance. In arithmetic and logical functions, the vast use of this operation has attracted many researchers to present various types of unique logic styles for designing 1-bit Full Adder cell. Power consumption, speed, and area are the three most important parameters of VLSI system. Designing low power VLSI systems have become an essential goal because of the rapid increasing technology in the field of communication and computing during the recent years. By using less number of transistors in order to implement any logic function has become profitable in reduction of parasitic capacitance and chip area, resulting into low power consumption or high speed by means of exponential relationship between number of transistors and area. Hence, low-power circuits plays a major role in VLSI design.

VLSI is dominated by CMOS technology and like other logic families, it also has its limitations that have been combated and improved over the years.

For example process technology has shrunk rapidly from 180 nm in 1999 to 60 nm in 2008 and is now 45nm., and attempts being made to reduce it further (32 nm) while the initial shrinkage now increases due to the additional benefits of higher packing density and a larger feature size that would mean more transistors on a chip.

As number of transistors increases the power dissipation increases as well as the noise. If the heat generated per unit area is to be considered, the chips are already close to the jet engine nozzle. At the same time, the voltage scaling of threshold voltages beyond a certain point posses series limitations in providing low dynamic power dissipation with increased complexity. The number of metal layers and interconnections, whether global or local also tend to become messy as such nano levels.

Full adder is the fundamental unit of computational blocks of almost every DSP-VLSI architecture. Several high end blocks such as parallel adders, ALU, MAC units etc. have a Full-adder in their core building blocks. DSP operations are frequently performed in various video-processing, linear filtering operations etc. Thus, enhancement in the performance of the 1-bit adder block shall imply enhancement in the performance of the entire system .The one bit full adder is capable of performing addition of three 1-bit inputs and producing result of 1 bit sum and 1 bit carry for the next stage.

To accommodate the growing demands, we propose a new power efficient Hybrid full adder using 14 transistors that produces very promising results, in terms of power consumption, propagation delay and transistor count.

We have compared our proposed 1-bit Hybrid Full Adder using pass transistor logic with other conventional and state of art Full Adder architectures. We have considered Number of Transistors used in design, Power Consumption and Propagation delay as the criteria for comparison**.**

II. LITERATURE SURVEY

Static CMOS logic is the most primitive design style for realizing a Full-adder. In Static CMOS logic, the Output node is either connected to VDD or VSS leading to decreased static power dissipation. Static realization of the Full-adder benefits from better noise margin and lower power consumption, compared to the dynamic counterpart. The implementation has also shown reliable output at lower voltage levels. The problem with static CMOS implementation, however, remains that for N fan in gate,2N transistor numbers are required, thus increasing the area on the chip. The common static CMOS implementation[1] of Full adder consists of 28 transistors & is commonly called **28T Static** Full Adder.

The next alternative to realize Full-adder is using dynamic logic style. Dynamic logic relies on the sequence of pre-charge and evaluation phases of the clock input. Dynamic Full adder is advantaged by increased speed. The speed-up can be accorded to the reduced number of transistors to implement the design. Lesser transistors would imply lesser load capacitance, which ultimately increases the speed of operation . However, Dynamic realization of Full-adder suffers from Leakage power consumption, noise and clock-skew issues. A common dynamic Full-adder has been realized using 16 transistors and is called 16T dynamic Full Adder[7].

The Full adder design in static CMOS with complementary PMOS and NMOS .This adder is based on regular CMOS structure (pull-up and pull-down network), which uses both NMOS and PMOS transistors. In a structure formed by two complementary networks, these transistors are arranged.

In Static CMOS ,only strong 0 must be passed by the NMOS Transistors and only strong 1 passes the PMOS .So the output is always strongly driven and the levels never decay . This is called a fully restored logic gate Pull-up network is complement of pull-down.
Full-adders based on domino logic[2] has been realized using 3 transistor implementations of the XOR and XNOR functions. However, a direct path between VDD and Ground leads to power losses. The domino logic full-adder is an improvement over in this regard. Also, the transistor count has been optimized. In domino logic, higher speed of operation is possible due to reduced number of intermediate transitions. Despite the issue of charge sharing, Domino logic Full-adder cell finds applications in high performance circuits.
The full adder for extensive PDP reduction [15] has been realized using three multiplexers .It has been done in order to reduce the number of transistors. The multiplexers acts as a building blocks of this architecture. The multiplexers have been realized by switch Restoring pass transistor logic. Realization of 2 X 1 MUX using SRPL logic involves 4 transistors and each NOT gate requires another 2 transistors. Therefore , the total number of transistors required for hybrid full adder for extensive PDP reduction is 20 transistors.

III. PROPOSED ARCHITECTURE

The proposed hybrid 1-bit full adder consists of 2 XOR gates , one multiplexer and inverters .Proposed Full adder architecture is designed as hybrid topology ,a combination of Static CMOS and Pass Transistor logic(PTL).While designing the full adder with pass transistor logic ,our main objective was aimed at reducing the number of transistors and hence reducing power consumption and delay experienced. Our proposed architecture is based on a different approach containing XOR gates as basic building blocks. The proposed 1 bit full adder with pass transistor logic consist of 14 transistors. In the previous existing method the 20 transistors are required. Due to 14 transistors the power consumption and propagation delay will be reduced.

Pass transistor logic(PTL) describes several logic families that are used to design integrated circuits. It reduces the number of transistors used to create different logic gates by eliminating redundant transistors. Transistors are used as switches for passing logic levels between circuit nodes instead of as switches directly connected to supply voltages .This reduces the number of active devices, but has the drawback of decreasing the voltage difference between high and low logic levels at each stage.

The pass transistor is controlled by a periodic clock signal and acts as an access switch to either charge or charge the parasitic capacitance C_x, depending on the V_{in} input signal. Thus ,two possible operations when the clock signal is active(CK=1) are the transfer of logic "1"(loading capacitance C_x to a high level of logic) and the transfer of logic "0"(loading capacitance C_x to a low level of logic).In either case, the output of the NMOS inverter with depletion load obviously assumes a low or high level of logic , depending upon the V_x voltage.
The Boolean expressions for the outputs of a 1-bit full adder are:
Sum=a ^ b ^ c (where x=b^c=b'c+bc')
=a ^ x
And
Carry =abc + a'bc + ab'c + abc'

= (a + a').bc + ab'c + abc'

= bc + ab'c+abc'

= (bb'+ bc + c'b' + c'c).b + ab'c + abc'

= ((b'c + bc')'.b + a.(b'c +bc')

= x'b + xa (where x = b ^c = b'c + bc').

Based on the above equations, we realize the full adder circuit using two XOR gates and multiplexer. It is important that inputs are considered in the same order for proper realization of truth table of a single bit full adder. This has been done in order to reduce the number of transistors .Pass transistor logic often requires fewer number of devices to implement the logic functions as compared to CMOS.

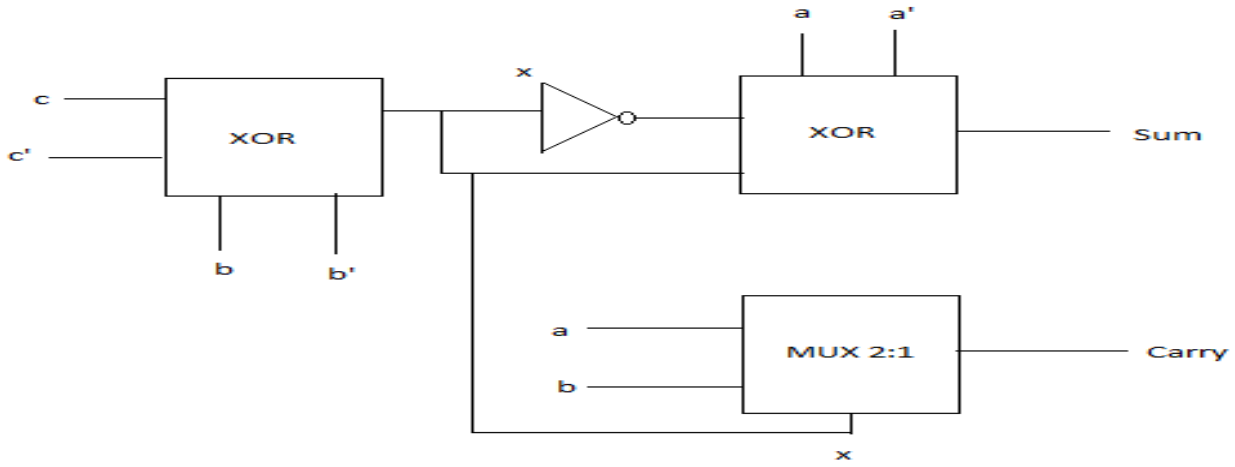

Figure: Block diagram of proposed hybrid 1-bit full adder using PTL

The block diagram of proposed method is shown above. It consists of XOR gates and multiplexer. Each XOR gate requires 2 transistors, multiplexer requires another 2 transistors. Each inverter requires 2 transistors. So there are 4 inverters in the circuit and it requires a total of 8 transistors. Therefore, the total numbers of transistors required is 14.So the wire length reduces and area consumption reduces. Due to this Power delay product also reduces(power delay product means product of power consumption and propagation delay).

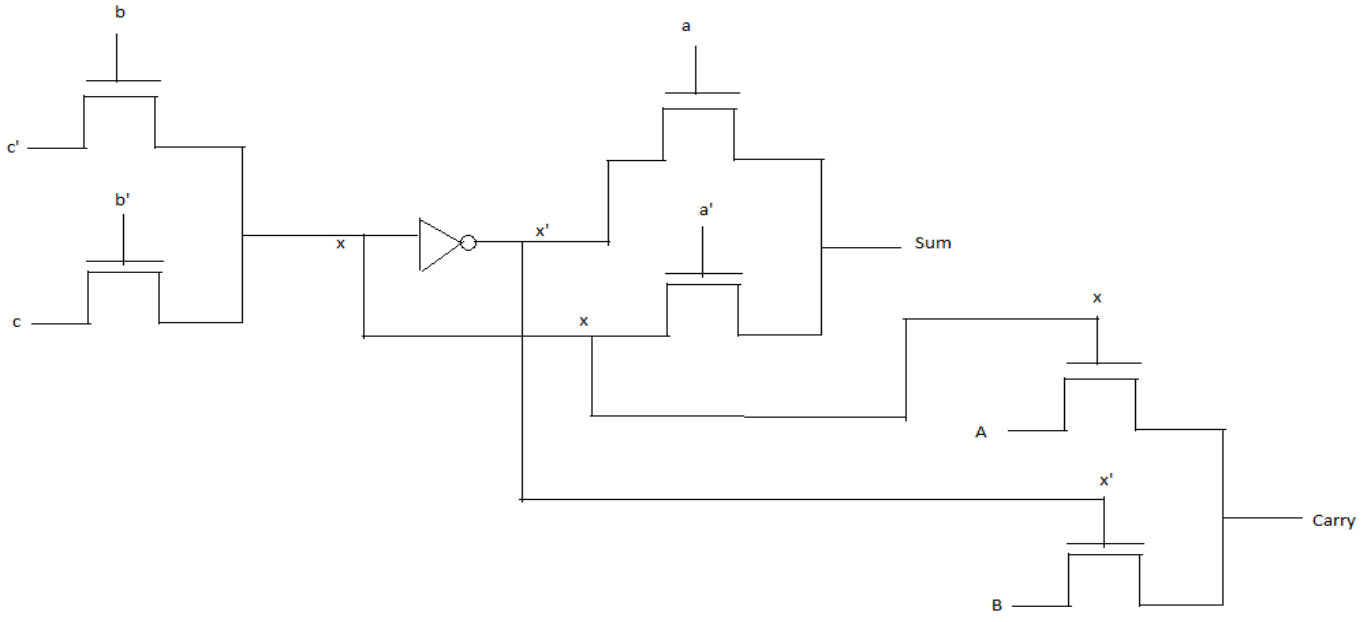

Figure: Internal structure of proposed hybrid 1-bit full adder using PTL

If a= 0,b= 0 and c= 0; the output sum becomes “0” and carry becomes “0”. The operation of above circuit yields the output of full adder circuit.

Similarly for remaining inputs we get sum and carry using two XOR gates and multiplexer. The output is similar to full adder circuit.

The schematic of the proposed architecture is shown in figure. We designed the circuit with the help of Cadence tool. The proposed architecture is implemented using 180nm technology.

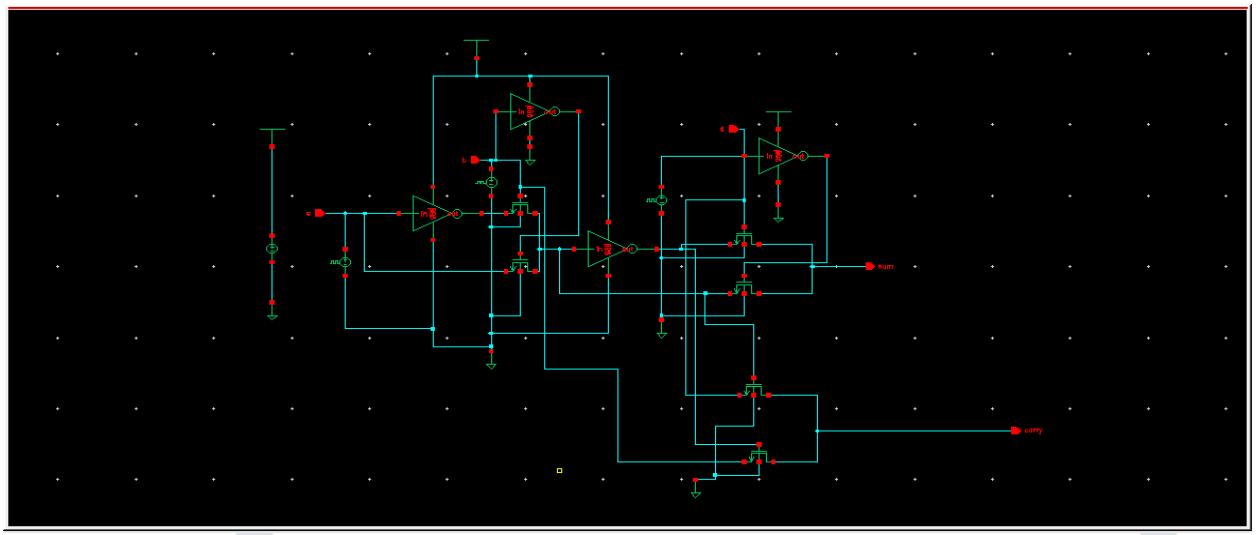

Figure: Schematic of proposed hybrid 1-bit full adder using PTL

IV. Simulation results:

We have performed simulations on Cadence tool using 180 nm technology. In this tool we simulate the design for n45 nm ,90 nm and 180 nm technology.
The results have been obtained for power consumption, propagation delay and power delay product(PDP).we are comparing the results with Static CMOS adder[],Domino based full adder[],Dual voltage logic full adder[],hybrid full adder[],hybrid CMOS full adder and hybrid 1-bit full adder[].All the power consumption calculations have been carried out at 100 MHz.
The voltage vs time output waveforms for the proposed hybrid 1-bit full adder using PTL is shown in figure.

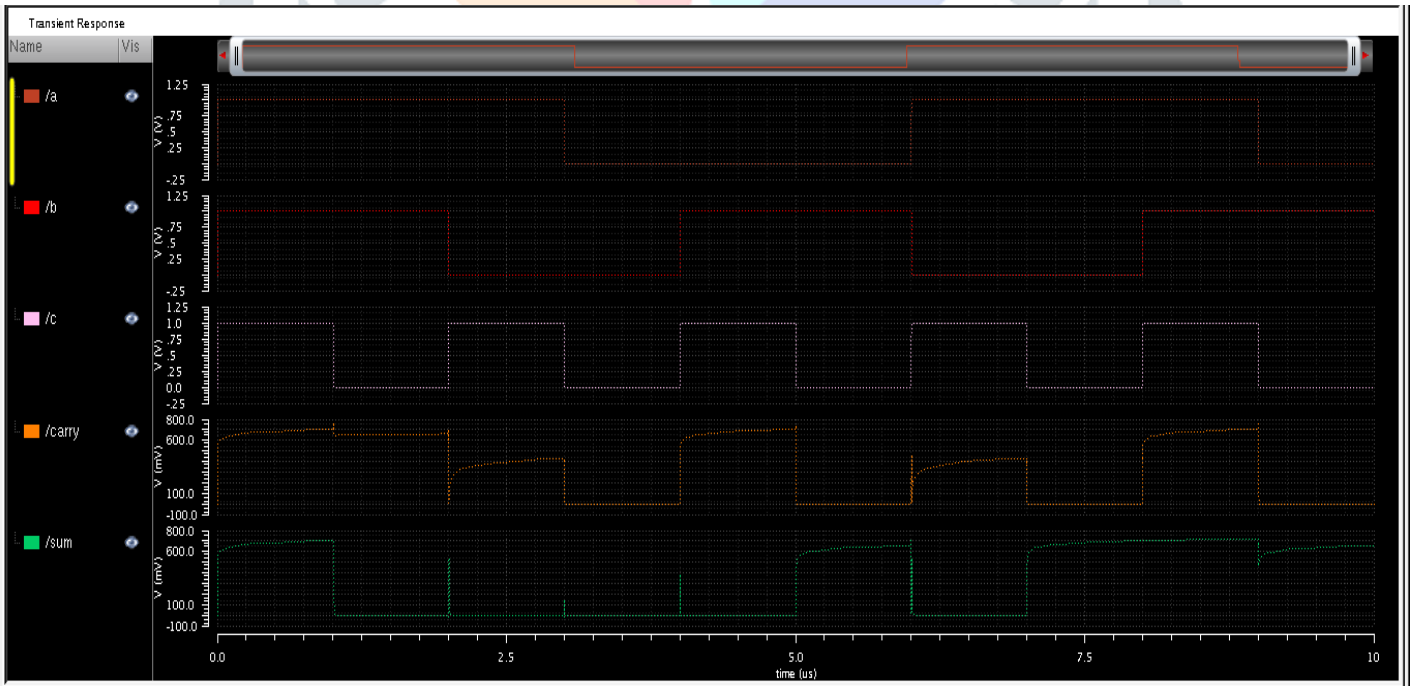

Figure :Simulated waveforms for proposed hybrid 1-bit full adder using PTL

VDD	1.0 V	1.8 V
Power consumption(in µW),100 MHz		
Static CMOS logic [1]	2.31	8.25
Domino logic [2]	1.73	7.72
Hybrid logic [3]	1.48	6.73
Dual voltage logic [4]	1.53	6.39
Hybrid logic CMOS [5]	1.23	4.50
Existing hybrid 1-bit full adder [15]	0.98	3.69
Proposed hybrid 1-bit full adder	0.7	2.33

Table 1: power consumption comparison for 1-bit full adder structures using PTL

VDD	1.0 V	1.8 V
Propagation delay(in ns)		
Static CMOS logic [1]	0.77	0.56
Domino logic [2]	0.72	0.49
Hybrid logic [3]	0.69	0.41
Dual voltage logic [4]	0.58	0.36
Hybrid logic CMOS [5]	0.46	0.23
Existing hybrid 1-bit full adder [15]	0.44	0.21
Proposed hybrid 1-bit full adder	0.37	0.19

Table 2:Propagation delay comparison for hybrid 1-bit full adder structures using PTL

VDD	1.0 V	1.8 V
Power delay product(PDP)		
Static CMOS logic [1]	1.78	4.62
Domino logic [2]	1.25	3.78
Hybrid logic [3]	1.36	2.37
Dual voltage logic [4]	1.25	1.99
Hybrid logic CMOS [5]	0.84	0.92
Existing hybrid 1-bit full adder [15]	0.43	0.77
Proposed hybrid 1-bit full adder	0.26	0.45

Table 3: Power delay product (PDP) comparison for hybrid 1-bit full adder using PTL

V. Conclusion:

In this paper, we have designed and analyze hybrid 1-bit full adder using pass transistor logic. we have simulated our design on cadence tool. The simulations have been carried out for 180nm technology at different voltage levels. Results obtained from the simulation shows that as the supply voltage is lowered the power consumption reduces ,however the propagation delay increases. While decreases in power consumption is desirable, but increase in propagation delay is a worry. thus the power delay product can be considered as Figure of merit and the standard for comparison of various 1-bit full adder circuits.

We have compared our results with other recently proposed 1-bit full adder circuits and found that with our efficient design style , there is an improvement in Power delay product(PDP) .This indicates that the proposed hybrid 1-bit full adder has better performance as compared with the previously proposed full adder circuits. We conclude that our proposed hybrid 1-bit full adder is a good choice in future.

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